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I - XI
ANNUAL INTERNATIONAL
MICROELECTRONICS OLYMPIAD OF ARMENIA
TESTS AND PROBLEMS

2016

CONTENT

Dear young engineers and students!

It's my special pleasure to introduce this very actual and useful problem and test book that consists of all problems and tests along with their solutions and answers used during these 11 years - since the First Armenian Microelectronics Olympiad to the Eleventh Annual International Microelectronics Olympiad of Armenia.

I highly welcome the idea of having such a problem and test book for the Annual International Microelectronics Olympiad of Armenia. Therefore I appreciate the immense work accomplished by the Olympiad Program Committee President Prof. Vazgen Melikyan and the members of the Program Committee. The impressive results of all the Olympiads have proven that the book serves as an essential source for acquiring problem solution skills for the participants, thus contributing greatly in the preparation stage. The soft version of the book is posted on the Olympiad website and is shared with all the participating countries: Argentina, Armenia, Belarus, Brazil, Chile, China, Colombia, Egypt, Georgia, Germany, Hong Kong, India, Iran, Israel, Jordan, Malaysia, Nagorno Karabakh, Peru, Philippines, Russia, Saudi Arabia, Serbia, Switzerland, Turkey, UAE, UK, Ukraine, Uruguay, USA and Vietnam.

This book serves not only as a repository of the problems and tests but also helps students to enhance the knowledge in microelectronics and similar engineering disciplines and develop solution skills. The great value of this problem book is that it can also serve as a resource for the trainings of the specialists in Microelectronics area.

I wish good luck to all Olympiad participants and hope this book will help them to be well prepared for the 12th Annual International Microelectronics Olympiad of Armenia.

With best wishes,
Armen Baldryan
President of Unicomp CJSC
President of Org. Committee of Annual International Microelectronics Olympiad of Armenia

PREFACE

During the last nine years the First (September 22-25, 2006), the Second (September 18-25, 2007), the Third (September 16-29, 2008), the Fourth (September 15-30, 2009), the Fifth (September 28-October 28, 2010), the Sixth (September 30-October 11, 2011), the Seventh(September 18 - October 4, 2012), the Eighth(April 26-October 15, 2013), the Ninth (June 3 - October 16, 2014) the tenth (May 6 - October 12, 2015) and the eleventh (September 27 - October 18, 2016) Microelectronics Olympiads of Armenia (http://www.synopsys.com/Company/Locations/Armenia/ EducationalPrograms/Microelectronics Olympiad) took place. The goals of these Olympiads are to: stimulate the further development of microelectronics in Armenia and participant countries, discover young, talented resources, increase interest towards microelectronics among them, and understand the level of knowledge in the field of microelectronics among young specialists to make necessary adjustments to educational programs.

The Olympiads are held in two stages. The first stage, which entailed a test involving a number of basic tasks, is held simultaneously in the local places in participating countries. The top contestants advance to the second stage, which takes place in Armenia and involves a challenging contest and complex engineering tasks requiring advanced solutions. The set of the test questions and problems of I-XI Annual Microelectronics Olympiads of Armenia along with their solutions are included in this book. You can also find at: (http://www.synopsys.com/Company/Locations/Armenia/EducationalPrograms/MicroelectronicsOlympiad). Test questions and problems are related to VLSI Design and EDA areas and are classified according to their basic sections: Digital integrated circuits, Analog integrated circuits, RF integrated circuits, Semiconductor physics and electronic devices, Semiconductor technology, Numerical methods and optimization, Discrete mathematics and theory of combinations, Object-oriented programming, Nanoelectronics.

The problem book, first of all, is for participants of the Annual International Microelectronics Olympiad of Armenia of the coming years. I hope it will contribute to the increase of knowledge level of potential participants in the Olympiad. At the same time, it can also be useful for other students, Masters, PhDs and engineers of the above mentioned areas.

The problem book also contains similar test questions and problems that are the variations of the corresponding type of tests and problems given to the participants during the Olympiads.

The problem book, in its future publications, will be extended with the test questions and problems of upcoming Olympiads.

You can send your remarks to microelectronics_olympiad@synopsys.com.

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Tests and problems

1. DIGITAL INTEGRATED CIRCUITS

a) Test questions

1a1. There is a tri-state buffer where internal delays can be ignored. Right after z state is set, the output voltage level will be:

A. VDD/2 where VDD is supply voltage
B. High or low, depending on the state before z state is set
C. Indefinite
D. High
E. Low

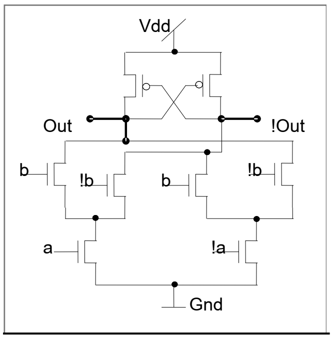
1a2. In CMOS ICs, PMOS transistor is usually configured as:

A. No potential is given to substrate
B. Substrate is connected to source
C. *Substrate is connected to drain*
D. The highest potential is given to substrate
E. The lowest potential is given to substrate

1a3. There is a JK flip-flop. Mark the prohibited input combination.

A. J=1, K=1
B. J=1, K=0
C. J=0, K=1
D. J=0, K=0
E. No prohibited combination

1a4. What logic function is implemented by the presented circuit?



A. AND
B. XOR-XNOR
C. AND-NAND
D. OR-NOR
E. MUX-MUXI

1a5. Which is the Canonical Disjunctive Normal Form (CDNF) of the function described by the following truth table?

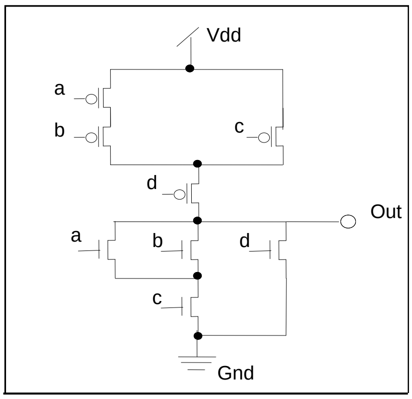
a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

A. y=!a&b&!c+!a&b&c+a&b&!c+a&b&c
B. y=!a&!b&!c+!a&!b&c+a&!b&!c+a&!b&c
C. y=(a+b+c)&(a+b+!c)&(!a+b+c)&(!a+b+!c)
D. y=(!a+!b+!c)&(!a+!b+c)&(a+!b+!c)&(a+!b+c)
E. y=(a+!b+c)&(a+!b+!c)&(!a+!b+c)&(!a+!b+!c)

1a6. Threshold voltage of a MOS transistor is called the voltage which is necessary to be applied between the gate and the source:

A. For 1uA current flow through drain
B. Of the transistor for current flow through drain which is 10 times more than leakage current of transistor
C. Of the transistor for average concentration of charge carriers that maintain transistor's conductance be equal to average concentration of majority charge carriers in substrate in channel formation place
D. Of the transistor for average concentration of charge carriers that maintain transistor's conductance be equal to average concentration of minority charge carriers in substrate in channel formation place
E. Of the transistor for the transistor to be saturated

1a7. What formula describes the circuit?



A. Out = !((!a+!b)&!c+!d)

B. Out = !((a+b)&c+d)

C. Out = !((a&b+c)&d)

D. Out = ((!a+!b)&!c+!d)

E. Out = !((!a&!b+!c)&!d)

1a8. Which statement is correct?

A. The operation of charge-coupled devices' (CCD) is based on processes occurring in bipolar transistors

B. CCD frequency internal limit is influenced by thermo generation of charge carriers

C. CCD frequency parameters do not depend on the degree of semiconductor's surface energetic levels

D. CCD frequency properties do not depend on the type of a semiconductor

E. CCDs are static devices

1a9. Which of the shown answers more contributes to the successful solution of placement issue of a cell?

A. Maximum distance between high frequency circuits

B. Maximum distance between low frequency circuits

C. Maximum proximity of more related cells

D. A. and C. together

E. B. and C. together

1a10. One of the rules of concurrent modeling is

A. Lc(γ) list defined for an external output line composes the set of testable faults which can be found by the given input set (vector)

B. Single stuck-at fault (SSF) model assume that there is only one fault in tested logic circuit

C. Two types of stuck-at logic faults - stuck-at-1 fault (SA1 or s@1) and stuck-at-0 fault (SA0 or s@0)

D. Lc(γ) list defined for an external output line composes the set of testable faults which can be found by an output set (vector)

E. None

1a11. In state-of-the-art integrated circuits the minimum width of interconnect transmission lines is limited by

A. Resolution of the lithography process

B. Mutual agreement of customer and manufacturer

C. Desire of designer

D. Technological method to get thin layers

E. Phenomena of electromigration

1a12. The increase of logic circuit organization's parallelism mostly leads to

A. The increase of performance

B. The increase of the number of primary outputs

C. The decrease of the number of logic cells

D. A. and B. together

E. B. and C. together

1a13. The f(x_1, x_2, x_3) function takes 1 value on 0, 3, 5, 6 combinations. What class does the given function belong to?

A. Constant 0

B. Constant 1

C. Linear and selfdual

D. Selfdual

E. Monotone

1a14. The operation of a Gunn diode is based on:

A. The effect of semiconductor inversion in strong electrical field

B. The appearance of negative differential impedance in strong electrical field

C. The tunnel effect in strong electrical field

D. The rectifying properties of p-n junction

E. The contact effects between metal and semiconductor

1a15. Which of the answers more contributes to the increase of fan-out?

A. Increase of cells' input resistance

B. Increase of cells' output resistance

C. Decrease of cells' output resistance

D. A. and B. together

E. A. and C. together

1a16. Which of the following statements is wrong for synchronous FSM?

A. Memory element competition, static and dynamic risks in combinational circuits are dangerous

B. The abstract presentation of the automaton is used to design a circuit

C. Synchronization of asynchronous input signals are required with clock signals

D. All FFs trigger at the same clock signal

E. The wrong answer is missing

1a17. The common emitter configuration compared with the common base configuration:

A. Increases frequency properties

B. Increases the collector junction's resistance

C. Increases collector junction's breakdown voltage

D. Increases the current gain

E. Decreases the thermal component of collector current

1a18. Which of following methods of interconnect designing more contributes to speed increase?

A. Increase of interconnect layers
B. Decrease of total length of interconnects
C. Decrease of length of signal processing critical path
D. B. and C. together
E. A. and C. together

1a19. Among the following principles, which is wrong for concurrent simulation?

A. Classification of vectors according to quality, move of low quality vectors in the beginning of simulation, elimination of detected faults – it increases simulation speed, reduces simulation time
B. Any subset of faults is simulated, extrapolation of fault coverage is executed according to obtained results
C. IC simulation, estimation of vectors' quality - 01 or 10 toggle node number, toggle coverage
D. For the given vector there is strict correlation between detectable fault number and 01, 10 toggle number
E. None

1a20. There is an inverter which has a passive capacitive load. If supply voltage increases,

A. Rise will increase, fall will decrease
B. Fall will increase, rise will decrease
C. Output transition time will decrease
D. Output transition time will increase, as during switching the load must be charged by larger ΔU voltage
E. Output transition time will remain the same, as ΔU will increase, but charging current will also increase

1a21. The transfer characteristic of MOS transistor is *the dependence of:*

A. Drain voltage on gate-source voltage
B. Drain voltage on drain-source voltage
C. Drain current on drain-source voltage
D. Drain current on gate-source voltage
E. Gate current on gate-source voltage

1a22. Latch-up phenomena is proper to

A. ECL circuits
B. Only CMOS circuits
C. N-MOS and CMOS circuits
D. P-MOS and CMOS circuits
E. All bipolar circuits

1a23. Which one is a prohibited input combination for RS latch?

A . R=0, S=1
B. R=1, S=0
C. R=0, S=0
D. R=1, S=1
E. There is no prohibited combination

1a24. Define in which state will Johnson's 6 bit counter go, after the 10th pulse is applied. Initial state is 000111.

A. 011110
B. 001011
C. 101010
D. 011010
E. The correct answer is missing

1a25. How many pins does the bipolar transistor have?

A. 1- emitter,
B. 2- emitter and base,
C. 2- base and collector,
D. 2- emitter and collector;
E. 3- emitter, base and collector,

1a26. What semiconductor material is mostly used in integrated circuits?

A. Ge
B. Si
C. GaAs
D. Fe
E. Zn

1a27. From the following statements which is wrong for DRAM?

A. Usually one MOS transistor is used to keep 1 bit in memory
B. FF is as a memory cell
C. Address inputs are multiplexed
D. DRAMs are considered energy dependent
E. The wrong answer is missing

1a28. In logic design level the following is designed:

A. A stand alone device which is divided up to such multibit blocks as registers, counters, etc.
B. A stand alone logic gate or FF, which consists of electronic components – transistors, diodes, etc.
C. A stand alone semiconductor component, e.g. a transistor
D. A digital device the components of which are separate logic gates and FFs
E. A general system which consists of RAM memory device, datapath devices, etc.

1a29. In component level of the design the following is designed:

A. A separate semiconductor device, e.g. a transistor
B. A separate device, which is being disassembled until diverse components, such as registers, calculators, etc.
C. A separate logic gate or FF which consists of electronic components – transistors, diodes, etc.

D. A general system which consists of operative memory device, numerical device, etc.

E. A digital device which consists of separate logic gates and FFs

1a30. In order to prevent latch-up in CMOS circuits it is necessary to:

A. Increase the parasitic capacitances between the buses of output buffer's parasitic bipolar transistors

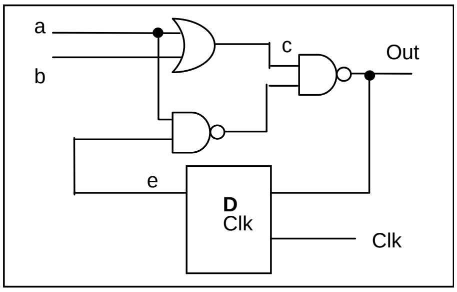
B. Increase the gain of parasitic bipolar transistors

C. Put the drains of n and p transistors as close as possible

D. Put n+ guard ring around n+ source/drain

E. Put p+ guard ring around n+ source/drain and put n+ guard ring around p+ source/drain

1a31. Identify the synchronous model of the following circuit (TP-delays, TF-transition time, "p"-previous state of a flip-flop).



A. c=a & b,
d=!(a | e),
Out=!(c & d),
e=posedge(Clk ? Out: 'p'), TP=0.1n,

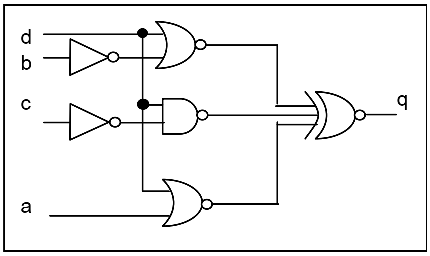
B. c=a | b
d=!(a | e),
Out=!(c & d),
e=posedge(Clk) ? Out: 'p'

C. c=a & b,
b=!(a | e),
Out=!(c & d),
e=!(posedge(Clk)? Out: 'p'), TF=0.1n

D. c=a & b, TP=0.1n,
d=!(a | e), TP=0.1n,
Out=!(c & d), TP=0.1n,
e=posedge(Clk) ? Out: 'p', TP=0.1n,

E. c=a & b, TP=0.1n,
d=a | e, TP=0.1n,
Out=c & d, TP=0.1n,
e=!(posedge(Clk)? Out: 'p'), TP=0.1n,

1a32. In case of which switching the occurrence of dynamic hazard exists in the following circuit?



A. a=0-1, b=1,
c=0, d=1

B. a=0, b=0-1,
c=0, d=0

C. a=0, b=1,
c=0, d=0-1

D. a=1, b=0,
c=1, d=0-1

E. a=0-1, b=0,
c=1, d=0

1a33. In digital circuits, PMOS transistor's

A. Delays do not depend on the supply voltage

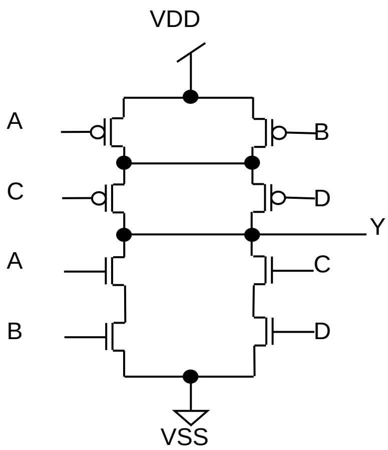
B. Threshold voltage is proportional to the delay of transistor

C. Delays do not depend on temperature

D. The highest potential is usually applied to substrate

E. Dynamic power dissipation depends only on transistor resistance

1a34. For the following circuit mention the input which will have the maximum input-to-output delay.



A. A

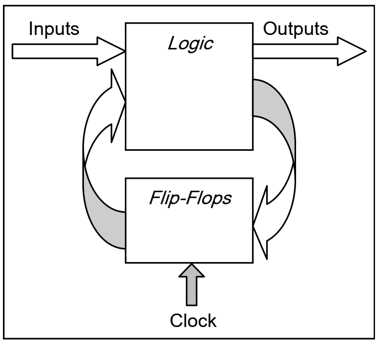
B. C

C. D

D. B

E. All are equal

1a35. In the following digital system, where setup time of FF is T_{SU}, delay T_{CLKQ}, and delay of logic part T_{LOGIC}, the highest clock frequency will be

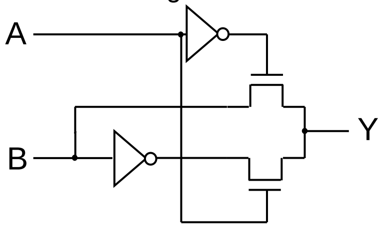


A. $f=1 / T_{LOGIC}$
B. $f=1 / (T_{LOGIC}+T_{SU})$
C. $f=1 / (T_{LOGIC}+T_{CLKQ}+T_{SU})$
D. $f= T_{LOGIC}+T_{CLKQ}+T_{SU}$
E. $f=1 / (T_{LOGIC}+2*T_{CLKQ}+T_{SU})$

1a36. Which is the sum of the following two signed hexadecimal numbers if the addition is performed by saturation adder 81H + FEH?
A. *7FH*
B. *FFH*
C. *00H*
D. *80H*
E. *77H*

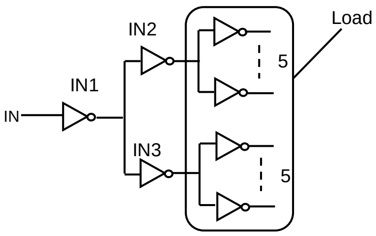
1a37. Which of the following is the binary representation of 3.25 decimal number in 4bit, 4bit fixed point format?
A. *01110101*
B. *10001010*
C. *00110100*
D. *00111010*
E. *01111001*

1a38. XOR logic circuit is presented. Which is the disadvantage of the circuit?



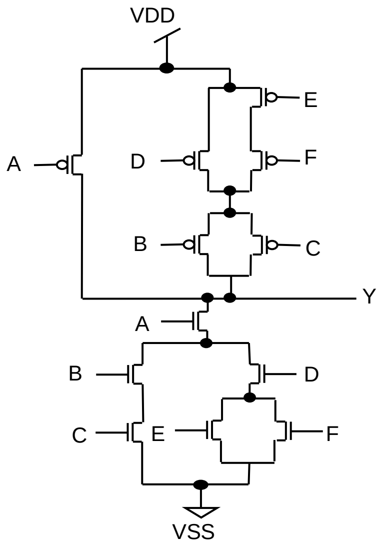
A. *Input capacitances are large*
B. *Delays are large*
C. *Output 1 level is degraded*
D. *Output 0 level is degraded*
E. *Power consumption is large*

1a39. Buffer circuit composed by I1, I2, I3 identical inverters is shown. The I2 and I3 are loaded by 5 similar inverters. What expression is the average delay of the buffer defined by?



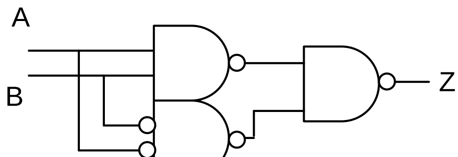
A. $(R_p+R_n)\cdot(2\cdot C_{out}+7\cdot C_{in})$
B. $(R_p+R_n)\cdot(5\cdot C_{out}+7\cdot C_{in})$
C. $(R_p+R_n)\cdot(C_{out}+7\cdot C_{in})$
D. $2\cdot(R_p+R_n)\cdot(2\cdot C_{out}+7\cdot C_{in})$
E. $(R_p+R_n)\cdot(2\cdot C_{out}+5\cdot C_{in})$

1a40. What logic function is realized in the circuit?



A. $A\cdot(B\cdot C+D\cdot(E+F))$
B. $A\cdot(B+C+D\cdot(E+F))$
C. $A+B\cdot C+D\cdot(E+F)$
D. $\overline{A\cdot(B\cdot C+D\cdot(E+F))}$
E. $\overline{A+B\cdot C+D\cdot(E+F)}$

1a41. What formula does the given circuit describe?



A. *Z=A&B+(!A&!B)*
B. *Z=(!A&B)+(!B&A)*
C. *Z=!A&B*
D. *Z=A&(!B)*
E. *Z=A+!B*

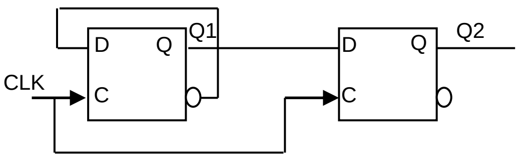
1a42. Saturation condition of a NMOS transistor looks like:
A. $V_{DS}\le V_{GS}-V_{THN}$
B. $V_{DS}\ge V_{GS}-V_{SB}$
C. $V_{GS}\ge V_{DS}-V_{THN}$
D. $V_{DS}\ge V_{GS}-V_{THN}$
E. $V_{DS}\ge V_{GS}+V_{THN}$

1a43. Conjunctive Normal Form (CNF) of the function in the following truth table has the following view:

a	b	c	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

A. (!a+!b+!c)& (!a+b+c)& (!a+b+c)& (!a+!b+c)
B. (a+!b+!c)& (!a+b+c)& (!a+b+c)& (!a+!b+!c)
C. (!a+!b+c)& (!a+!b+c)& (!a+b+c)& (!a+!b+c)
D. (a+b+c)& (!a+b+c)& (!a+b+!c)& (!a+!b+c)
E. !a&!b&!c+ !a&b&!c+ a&!b&!c+ a&b&c

1a44. In what state will the below shown automaton go, after applying four pulses if the initial state is Q1Q2=1x?

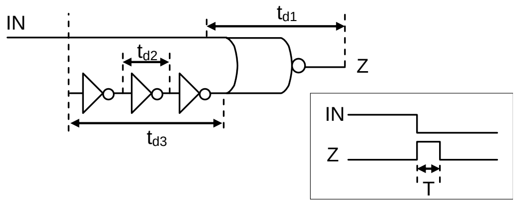


A. 01
B. 10
C. 00
D. 11
E. x1

1a45 In digital circuits, for an NMOS transistor
A. The lowest potential is usually given to substrate
B. Delays do not depend on the supply voltage
C. Threshold voltage is proportional to the delay of transistor
D. Delays do not depend on temperature
E. Dynamic power dissipation depends only on transistor resistance

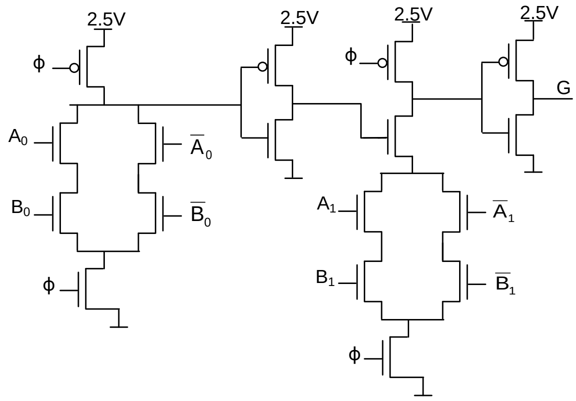
1a46. Which is the sum of the following two signed hexadecimal numbers if the addition is performed by saturation adder 12H + 70H?
A. 7FH
B. FFH
C. 00H
D. 80H
E. 82H

1a47. T duration of the short pulse, obtained on the output of the given circuit, is mainly defined by?



A. td1
B. td3
C. td2
D. td1 + td2
E. td1 + td3 delays

1a48. If A and B are interpreted as two-bit binary words A = {A1, A0} and B = {B1, B0}, what interpretation can be applied to output G?

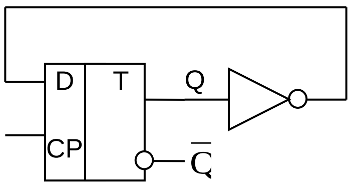


A. Scalar product: G=(A0&B0)+(A1&B1)
B. Modulo-2 sum:
G=(A0⊕B0) ⊕ (A1⊕B1)
C. Equality:
G=(A = = B)
D. Non-equality
G=(A != B)
E. Logic sum
G=A0+B0+A1+B1

1a49. Considering that NOR2 cell's inputs are independent and equally distributed, which is the probability of output switching?
A. 0.25
B. 0.375
C. 0.5
D. 0.75
E. 0.875

1a50. Assuming $k_n=2k_p$, in what case will the resistances from the output of NOR2 cell to VDD and VSS be equal?
A. $W_p=W_n$
B. $W_p=2W_n$
C. $W_p=4W_n$
D. $W_p=6W_n$
E. $W_p=8W_n$

1a51. The figure shows the circuit of a frequency divider.
What expression gives the minimum period of clock pulses?

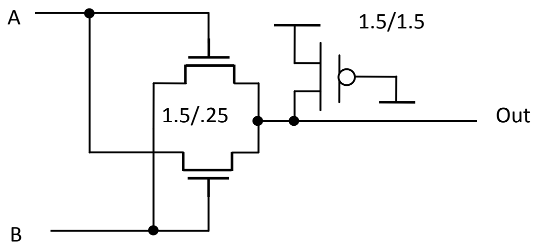


A. $T_{min}=t_{su}+t_{c2q}+t_{pinv}$
B. $T_{min}= t_{c2q}+t_{pinv}$
C. $T_{min}=t_{su}+t_{hd}+t_{c2q}+t_{pinv}$
D. $T_{min}= t_{hd}+t_{c2q}+t_{pinv}$
E. $T_{min}= t_{su}+t_{hd}+t_{pinv}$

1a52. How many digits does the thermometer code have which is obtained after modifying 4-bit binary code?
A. 16
B. 4
C. 15
D. 8
E. 32

1a53. For the same size inverter what version has minimum leakage current?
A. PMOS low-vt, NMOS high-vt
B. PMOS standard-vt, NMOS high-vt
C. PMOS high-vt, NMOS standard-vt
D. PMOS high-vt, NMOS low-vt
E. PMOS low-vt, NMOS standard-vt

1a54. What logic function does the circuit implement?



A. OUT=A+B
B. OUT=A&B
C. OUT=!A+!B
D. OUT=!A&!B
E. OUT=A⊕!B

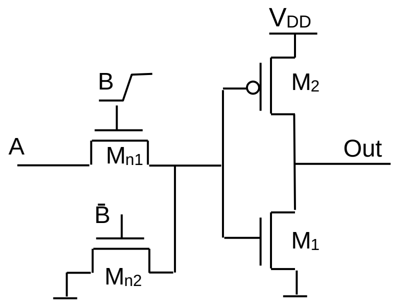
1a55. Which is the basic consequence of MOS transistor's degradation due to warm carriers?
A. The increase of threshold voltage
B. The decrease of threshold voltage
C. The increase of channel resistance
D. The decrease of channel resistance
E. The decrease of drain-package disruption voltage

1a56. Assuming $k_n=rk_p$, in what case will the resistances from the output of 3NAND cell to VDD and VSS be equal?
A. $W_p/W_n=r$
B. $W_p/W_n=r/9$
C $W_p/W_n=r/6$
D. $W_p/W_n=r/3$
E. $W_p/W_n=2r/3$

1a57. Which one of the given expressions is wrong?
A. A⊕!B = !A⊕B
B. 1⊕!B⊕A = B⊕A
C. A⊕B =! A⊕!B
D. A⊕!B = !A⊕!B
E. !A⊕B = !(A⊕B)

1a58. What is the minimum number of transistors in a pass gate implemented 1:4 multiplexer, assuming that normal and complemented select variables are available:
A. 16
B. 12
C. 8
D. 6
E. 4

1a59. What function does the circuit implement?

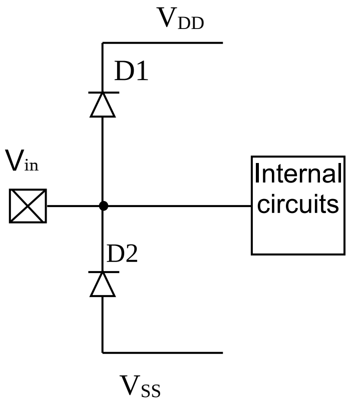


A. OUT=A+B
B. OUT=A&B
C. OUT=!A+!B
D. OUT=!A&!B
E. OUT=A⊕!B

1a60. C capacitance is connected to the end of interconnect line with L length, line parameters are c [F/m], r [Ohm/m]. By what formula is the signal delay time in the line given?
A. 0.7rc
B. 0.7Lr(C+c)
C. 0.7Lr(C+Lc/2)
D. 0.7Lr(C+Lc)
E. 0.7Lr(C/2+Lc/2)

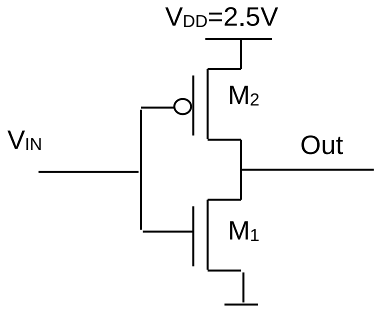
1a61. By increasing the metal line length of interconnect in IC, the delay increases
A. Linearly
B. By square law
C. By 3/2 law
D. By 2/3 law
E. By cubic law

1a62. Assuming that a p-n junction forward bias voltage is V_{pn}, what is the input voltage maximum safe margin?



A. $V_{SS} \le V_{in} \le V_{DD}$
B. $V_{SS}-V_{pn} \le V_{in} \le V_{DD}-V_{pn}$
C. $V_{SS}+V_{pn} \le V_{in} \le V_{DD}+V_{pn}$
D. $V_{SS}-V_{pn} \le V_{in} \le V_{DD}+V_{pn}$
E. $V_{SS}+V_{pn} \le V_{in} \le V_{DD}-V_{pn}$

1a63. Which answer is true if $V_{IN}=V_{DD}$?



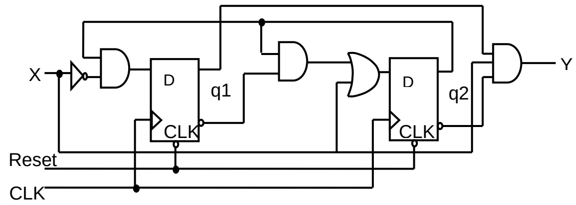
A. M1-saturated, M2-linear
B. M1-linear, M2-linear
C. M1- linear, M2- saturated
D. M1-saturated, M2-saturated
E. None

1a64. In what case is the short connection current missing in a CMOS inverter?
A. $V_{tp}=V_{tn}$
B. $V_{tp}+V_{tn}=0$
C. $V_{tp}+V_{tn}<VDD$
D. $|V_{tp}|+V_{tn}<VDD$
E. $|V_{tp}|+V_{tn}<VDD/2$

1a65. What equation describes JK flip-flop function?
A. Q+=Q&J + !Q&K
B. Q+=!Q&J + Q&K
C. Q+=!Q&J + Q&!K
D. Q+=Q&!J + !Q&K
E. Q+=Q&J + !Q&!K

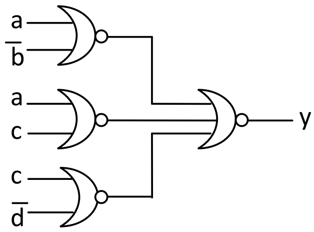
1a66. At passing from one technology to the other, transistors are scaled by S <1 coefficient due to which the gate capacitance of a transistor with minimal sizes, depending on S:
A. Increases linearly
B. Decreases linearly
C. Increases by square law
D. Decreases by square law
E. Does not change

1a67. Given a circuit of synchronous FSM, detector of an input sequence, perform FSM analysis.



Determine which input sequence the given FSM detects. The end of the previous word may be the beginning of the next one.
A. 0110
B. 1001
C. 0100
D. 1101
E. The correct answer is missing

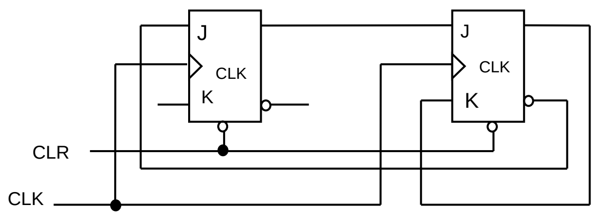
1a68. Given a circuit in NOR basis. What function does the given circuit implement?



A. $\bar{a} \cdot b + \bar{a} \cdot \bar{c} + \bar{c} \cdot d$
B. $a \cdot c + \bar{b} \cdot c + a \cdot \bar{d}$
C. $b \cdot c \cdot \bar{d} + \bar{a} \cdot b + c \cdot d$
D. $\bar{a} \cdot b \cdot \bar{d} + a \cdot \bar{b} + c \cdot d$
E. The correct answer is missing

1a69. What is the difference of electrical “short” or “long” interconnects at most characterized by?
A. Interconnect width
B. Signal power
C. Signal edge increase
D. Current power
E. A. and B. together

1a70. Analyze an FSM circuit, built on JK-flip-flops.
Which of the listed functions realizes the given circuit?



A. It is a modulo-4 binary up counter
B. It is a modulo-3 binary up counter

C. It is a modulo-4 binary down counter
D. It is a modulo-3 binary down counter
E. The correct answer is missing

1a71. In case of the shown element base, what is the order of power reduction of the circuit? a) bipolar; b) CMOS; c) N-MOS

A. a - c - b
B. b - c -a
C. a - b - c
D. b - a - c
E. c - b - a

1a72. It is required to construct 64:1 multiplexer using 8:1 multiplexer. How many 8:1 multiplexers are needed?

A. 8 MUX 8:1
B. 9 MUX 8:1
C. 10 MUX 4:1
D. 11 MUX 8:1
E. The correct answer is missing

1a73. Which of the below listed criteria of organizing interconnects more contributes to the increase of performance?

A. Increase of the number of interconnects layers
B. Similarity of interconnects length
C. Increase of the number of vias
D. Reduction of critical path of signal processing
E. A. and B. together

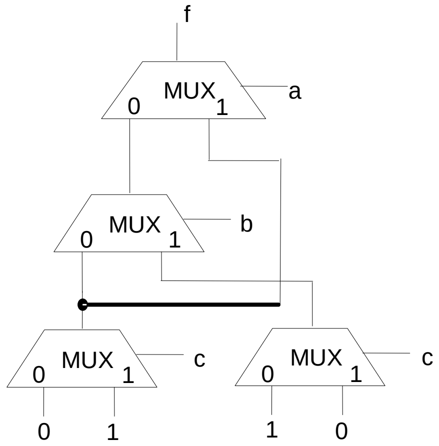
1a74. The logic of which circuit presented by VHDL code is senseless or wrong?

A.
```
process (clock)
  begin
    Y <= A and B;
  end process;
```
B.
```
process (A)
  begin
    A <= A + 1;
  end process;
```
C.
```
process (A)
  begin
    Y <= A + 1;
  end process;
```
D.
```
process (A, B)
  begin
    Y <= A and B;
  end process;
```
E.
```
process (reset_n, clock)
  begin
    if (reset_n = '0') then
      Y <= 0;
    elsif (clock'EVENT and clock = '1')
then
      Y <= A and B;
    end if;
  end process;
```

1a75. Given F(x1,x2,x3) = x1⊕ x2⊕ x2·x3 function. Which of the given expressions corresponds to the given function?

A. $F = x1\cdot \overline{x2} + x1\cdot x3 + \overline{x1}\cdot x2\cdot \overline{x3}$
B. $F = x1\cdot x2 + \overline{x1}\cdot x3 + \overline{x1}\cdot x2\cdot \overline{x3}$
C. $F = \overline{x1}\cdot \overline{x2} + x1\cdot x2 + x2\cdot \overline{x3}$
D. $F = x1\cdot \overline{x2} + x2\cdot x3 + x1\cdot \overline{x3}\cdot x2$
E. $F = x1\cdot \overline{x2} + x1\cdot x2 + x2\cdot \overline{x3}$

1a76. Which of the functions below is realized in the given circuit on multiplexer?

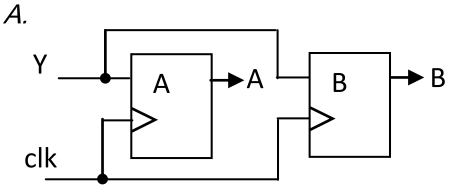


A. $b\cdot c + a\cdot c + \overline{a}\cdot b\cdot \overline{c}$
B. $a\cdot b + b\,\overline{c} + a\,\overline{c}$
C. $a\cdot \overline{b} + a\cdot b\cdot c + \overline{b}\cdot c$
D. $a\cdot b + a\cdot b\cdot c + \overline{b}\cdot c$
E. $b\cdot c + a\cdot c + b\cdot c$

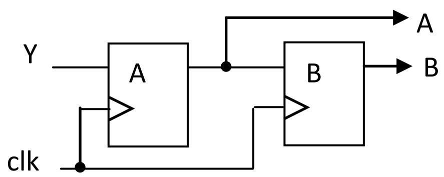
1a77. Which circuit does the use of the following assignment correspond to?

```
always @(posedge clk)
begin
    A<=Y;
   B<=A;
end
```

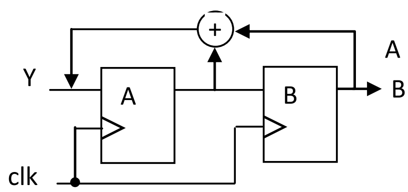
A.



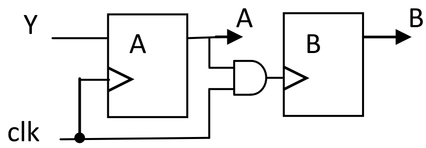
B.



C.

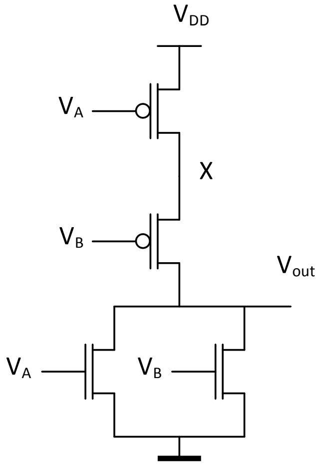


D.



E. None of the circuits corresponds to the assignment.

1a78. In case of what transition of an input signal, the circuit output does not switch and X node switches?



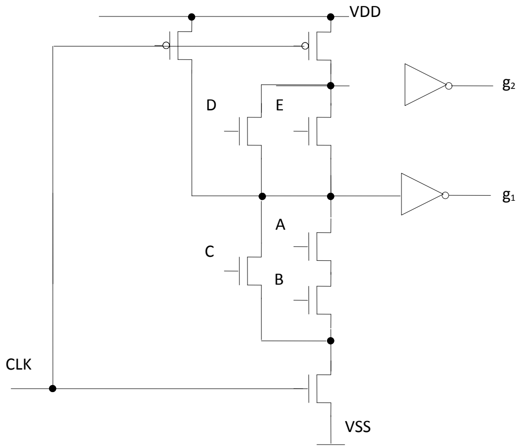
A. AB=00->01
B. AB=00->11
C. AB=01->10
D. AB=11->00
E. AB=10->00

1a79. For what purpose is Low-Doped-Drain (LDD) region created?
A. To increase threshold voltage
B. To increase saturation voltage
C. To increase gate-source break-down voltage
D. To reduce gate capacitance
E. To increase gate's oxide break-down voltage

1a80. The first stage of 12-input 2-stage decoder is implemented by 3AND cells, and the second one - by 4AND cells. How many 3AND cells are there in the first stage?
A. 16
B. 24
C. 32
D. 8
E. 64

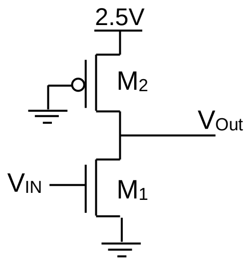
1a81. Considering that memory array has equal number of 1-bit cells in lines and columns, define how many word lines 10 address bit memory has if the word length is 4 bits.
A. 32
B. 64
C. 128
D. 10242
E. 256

1a82. What logic function does the circuit implement?



A. $g_1=(A+B)C$, $g_2=(A+B)C+ED$
B. $g_1=AB+C$, $g_2=(AB+C)(E+D)$
C. $g_1=AB+C$, $g_2=(AB+C)ED$
D. $g_1=AB\oplus C$, $g_2=(AB\oplus C)ED$
E. $g_1=AB+C$, $g_2=(AB+C)(E\oplus D)$

1a83. Which answer is correct if VIN=1.25V, Vtp=-1V; Vtn=1V, VSP=1.25V?



A. M1-in saturation mode, M2- in linear mode
B. M1-in linear mode, M2-in linear mode
C. M1- in linear mode, M2-in saturation mode
D. M1-in saturation mode, M2-in saturation mode
E. None

1a84. Assuming that the inputs of XOR2 cell are independently distributed evenly, what is the
probability of output switching?
A. 0.25
B. 0.375
C. 0.5
D. 0.75
E. 0.875

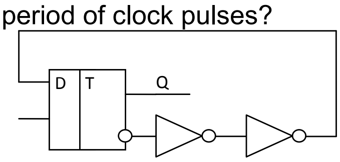
1a85. What does the threshold voltage of MOS transistor depend on?
A. Channel length
B. Concentration of substrate dopant atoms

C. Diffusion depth of source and drain
D. Gate voltage
E. Drain voltage

1a86. Assuming k_n=2.5k_p, in what case will the resistances from the output of NOR2 cell to VDD and VSS be equal?
A. W_p=4W_n
B. W_p=W_n
C. W_p=2W_n
D. W_p=10Wn
E. W_p=5W_n

1a87. Assuming k_n=rk_p, in what case will the resistances from the output of 4NAND cell to VDD and VSS be equal?
A. W_p/W_n=r
B. W_p/W_n=r/8
C. W_p/W_n=r/4
D. W_p/W_n=r/16
E. W_p/W_n=2r

1a88. The figure shows the circuit of a frequency divider.
What expression gives the minimum period of clock pulses?



A. $T_{min}=t_{su}+t_{c2q}+2t_{pinv}$
B. $T_{min}= t_{c2q}+2t_{pinv}$
C. $T_{min}=t_{su}+t_{hd}+t_{c2q}+2t_{pinv}$
D. $T_{min}= t_{hd}+t_{c2q}+2t_{pinv}$
E. $T_{min}= t_{su}+t_{hd}+2t_{pinv}$

1a89. When passing from one technology node to another, transistors are scaled by S <1 coefficient due to which the gate capacitance of a transistor with minimum sizes depends on S (assuming gate oxide thickness does not change):
A. Increases by square law
B. Decreases by square law
C. Increases linearly
D. Decreases by cubic law
E. Does not change

1a90. Before reading from 1T DRAM cell, the bitline should:
A. Discharge to VSS
B. Discharge to V_t
C. Discharge to VDD
D. Charge to VDD/2
E. Charge to VDD-V_t

1a91. For the same size inverter what version has the minimum input capacitance?
A. PMOS low-vt, NMOS high-vt
B. PMOS standard-vt, NMOS high-vt
C. PMOS high-vt, NMOS standard-vt
D. PMOS high-vt, NMOS low-vt
E. PMOS low-vt, NMOS standard-vt

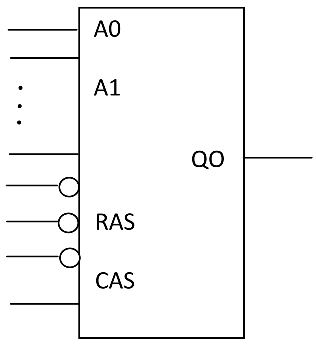
1a92. What is the minimum number of transistors in a pass gate implemented 1:4 multiplexer, assuming that normal and complemented select variables are available?
A. 16
B. 12
C. 8
D. 6
E. 4

1a93. Define in which state 6 bit Johnson's counter will be after the 10th clock pulse. The initial state is 000111.
A. 011110
B. 011111
C. 111111
D. 111101
E. The correct answer is missing

1a94. A fragment of Verilog description is presented below. What value will Y variable take after execution of this fragment?
reg A; **reg** [1:0] B,C; **reg** [2:0] D;
reg [15:0] Y;
A=1'b1; B=2'b01; C=2'b10; D=3'b110;
Y={2{A}, 3{B}, C, 2{D}};

A. Y = 10'b 1100_1100_0111_1001
B. Y = 10'b 1000_1111_1010_0101
C. Y = 10'b 1101_0101_1011_0110
D. Y = 10'b 1100_0100_0111_1001
E. The correct answer is missing1a101.

1a95. Define the volume of the IC DRAM presented below.



A. 256 M bit
B. 16 K bit
C. 16 M bit
D. 32M bit
E. The correct answer is missing

1a96. Which of the choices represents the number -7/256 as a floating point number with single precision (standard IEEE 754)?
A. 1284 F000
B. BCE0 0000
C. DA00 1000
D. CA01 1000
E. The correct answer is missing

1a97. How many address inputs does IC DRAM have with organization 512 Mx1Bit?

A. 28
B. 15
C. 12
D. 4
E. The correct answer is missing

1a98. Given $F(x_1,x_2,x_3) = x_1 \oplus x_1 \cdot x_3 \oplus x_2 \cdot x_3$ function. Which of the mentioned expressions corresponds to the given function?

A. $F = x_2 \cdot x_3 + x_1 \cdot \overline{x_3}$
B. $F = x_1 \square x_2 + \square x_1 \square x_3 + \square\square x_1 \square x_2 \square\square x_3$
C. $F = \square x_1 \square\square x_2 + x_1 x_2 + x_2 \square\square x_3$
D. $F = \square x_1 \square x_2 + x_1 \square x_2 + x_2 \square\square x_3$
E. The correct answer is missing

1a99. Which size does IC ROM have, implementing combinational multiplication of two 8 bit numbers?

A. 128K□8
B. 256□16
C. 64Kx16
D. 256K□16
E. The correct answer is missing

1a100. How many ICs with 512Kx8 organization are required to implement static memory module of 8M 16 bit words size?

A. 16
B. 32
C. 8
D. 24
E. The correct answer is missing

1a101. The following examples are expected to be models of logical shifter (written in Verilog HDL). Which of these examples will serve as pure combinational logic?

1)
```
wire [7:0] my_signal;
assign my_signal=my_signal<<1;
```
2)
```
reg [7:0] my_signal;
always @ (*) begin
  my_signal = my_signal << 1;
end
```
3)
```
reg [7:0] my_signal;
always @ (posedge clock) begin
  my_signal <= my_signal << 1;
end
```
Select the only correct version of these four possible answers:

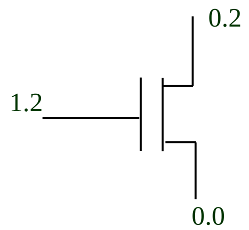
A. Only example 1) is the correct one
B. Only example 2) is the correct one
C. Only example 3) is the correct one
D. Only examples 1) and 2) are the correct ones
E. All examples are correct

1a102. The following examples are expected to be models of logical "NOT" cell (written in Verilog HDL). Which of these examples will serve as correct combinational logic?

1)
```
module not_cell (input_sig,  output_sig);
input  input_sig;
output output_sig;
  always @ (*) begin
    output_sig = 1'b1;
     if (input_sig == 1'b1)   begin
       output_sig = 1'b0;
    end
  end
endmodule
```
2)
```
module not_cell (input_sig, output_sig);
input  input_sig;
output output_sig;
  always @ (*) begin
    if (input_sig == 1'b1) begin
      output_sig = 1'b0;
    end
    else begin
      output_sig = 1'b1;
    end
  end
endmodule
```
3)
```
module not_cell (input_sig, output_sig);
input  input_sig;
output output_sig;
  always @ (input_sig) begin
    if (input_sig == 1'b1) begin
      output_sig = 1'b0;
    end
    else begin
      output_sig = 1'b1;
    end
  end
endmodule
```
Select the only correct version of these four possible answers:

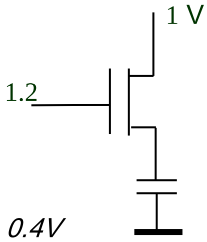
A. Only example 1) is the correct one
B. Only example 2) is the correct one
C. Only example 3) is the correct one
D. All examples are incorrect
E. All examples are correct.

1a103. For the circuit shown below determine the operating mode if V_{T0}=0.4V.



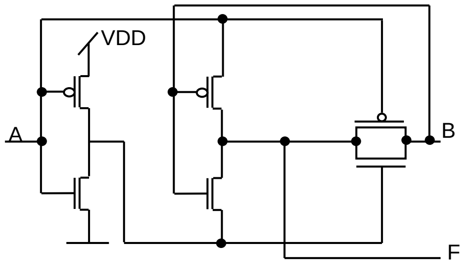
A. Cut-off
B. Linear
C. Tetrode
D. Non-linear
E. Saturation

1a104. For the circuit shown below determine the steady state voltage across the capacitor. Assume the capacitor was initially discharged and V_{T0}=0.4V.



A. 0.4V
B. 1.2V
C. 0.8V
D. 1.0V
E. 0.6V

1a105. What is the logic function performed by this circuit?



A. F=A+B
B. F=A&B
C. F=!A+!B
D. F= A⊕B
E. OUT=A⊕!B

1a106. What is the output switching activity of the AND2 circuit if inputs are independent and uniformly distributed?

A. 0.25
B. 0.1875
C. 0.5
D. 0.75
E. 0.375

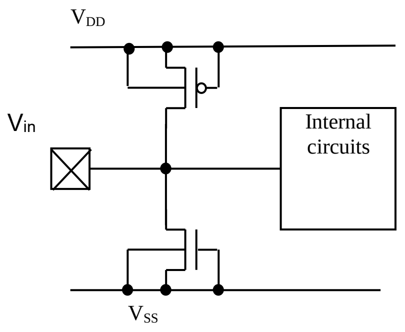
1a107. Assuming $k_n=3k_p$, in what case in a NOR2 cell the output to V_{DD} and output to V_{SS} impedances are equal?

A. $W_p=4W_n$
B. $W_p=W_n$
C. $W_p=3W_n$
D. $W_p=12W_n$
E. $W_p=6W_n$

1a108. Assuming $k_n=rk_p$, in what case in a NOR2 cell the output to V_{DD} and output to V_{SS} impedances are equal?

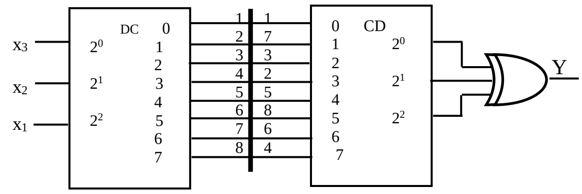
A. $W_p/W_n=r$
B. $W_p/W_n=r/4$
C. $W_p/W_n=r/8$
D. $W_p/W_n=r/2$
E. $W_p/W_n=2r/3$

1a109. Assuming that a p-n junction forward bias voltage is V_{pn}, what is the input voltage maximum safe margin?



A. $V_{SS} \le V_{in} \le V_{DD}$
B. $V_{SS}-V_{tn} \le V_{in} \le V_{DD}-V_{tp}$
C. $V_{SS}+V_{tn} \le V_{in} \le V_{DD}+V_{tp}$
D. $V_{SS}-V_{pn} \le V_{in} \le V_{DD}+V_{pn}$
E. $V_{SS}+V_{pn} \le V_{in} \le V_{DD}+V_{pn}$

1a110. What function is realized by this circuit?



A. $Y= x_1 \cdot \overline{x_3} + \overline{x_1} \cdot x_2$
B. $Y= \overline{x_1} \cdot \overline{x_2} + x_2 \cdot x_3 + x_1 \cdot x_2$
C. $Y= x_1 \cdot \overline{x_2} + \overline{x_1} \cdot x_3 + \overline{x_1} \cdot x_2$
D. $Y= x_1 \cdot \overline{x_2} + \overline{x_2} \cdot x_3 + \overline{x_1}$
E. None of the above

1a111. The number A is represented in memory in floating point form (standard IEEE 754) and is equal to 40C0 0000 (hexadecimal system). Which of the mentioned numbers corresponds to the given A number?

A. 6
B. 10
C. 35
D. 20
E. None of the above

1a112. A fragment of a program by Verilog is presented. Define at what moment of time the change of c will occur and what will equal the value c.

```
initial
begin
a <= 0;
b<=1;
#20 a <= 1;
b <= #20 a + 1;
c <= #20 b + 1;
end
```

A. *c=1. time=20*
B. *c=2. time=20*
C. *c=3. time=40*
D. *c=2. time=40*
E. *None of the above*

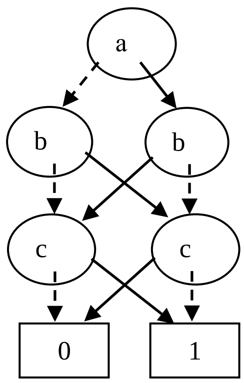
1a113. Which of the following expressions corresponds to polynomial representation of $y = x_1 + x_2$ function (Zhegalkin polynomial)

A. $y = x_1 \oplus x_2 \oplus x_1 \cdot x_2$
B. $y = x_1 \oplus x_2$
C. $y = x_1 \oplus x_2 \cdot x_2$
D. $y = 1 \oplus x_1 x_2 \oplus x_2$
E. *None of the above*

1a114. An FSM is given. The number of states is 66. After minimization, 32 states remained. How much will the number of those FFs decrease which are necessary for implementation of FSM memory? Assume the number of used FFs is minimum.

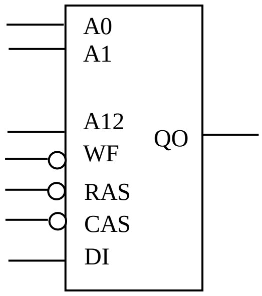
A. *3*
B. *2*
C. *5*
D. *1*
E. *None of the above*

1a115. Define which of the following expressions corresponds to the function, presented in the form of ROBDD.



A. $f(a,b,c) = a \oplus a \cdot c \oplus b \cdot c$
B. $f(a,b,c) = a \cdot b \cdot c + \bar{a} \cdot b + a \cdot \bar{b}$
C. $f(a,b,c) = a \oplus b \oplus c$
D. $f(a,b,c) = a \cdot b \cdot + \bar{a} \cdot c + a \cdot \bar{b}$
E. *None of the above*

1a116. Define the volume of the presented DRAM microcircuit.



A. *64 M bit*
B. *8 K bit*
C. *16 M bit*
D. *32M bit*
E. *None of the above*

1a117. How many SRAMs with 128Kx8 organization are needed to design a 1MB size memory block?

A. *16*
B. *8*
C. *4*
D. *12*
E. *None of the above*

1a118. The difference between clock gating and power gating is that:

A. *The first reduces the dynamic power, and the second reduces the total power consumed in the circuit*
B. *The first reduces the static power, and the second reduces the total power consumed in the circuit*
C. *The first reduces the switching activity in the circuit, and the second reduces the dynamic power only in the circuit*
D. *All of the above*
E. *None of the above*

1a119. Interconnect coupling capacitance can be a problem, because:

A. *It might create extra capacitive load on a switching signal*
B. *It causes glitches in a silent wire neighbored by a switching wire*
C. *It transforms the delay optimization problem into much more complex RCL circuit analysis problem*
D. *All of the above*
E. *None of the above*

1a120. Crosstalk in interconnects is defined as:

A. *Two logic blocks communicating (talking) to each other*

B. *An unintended noise injected into a victim wire from an aggressor wire*
C. *Two interconnects switching in the same direction*
D. *None of the above*
E. *None of the above*

1a121. Design reuse and Intellectual Property cores can be injected into the design at:
A. *Register Transfer Level or RTL*
B. *Gate-level or the synthesized netlist*
C. *Very late in the design and before fabrication*
D. *All of the above*
E. *None of the above*

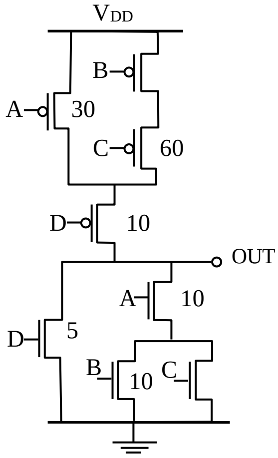
1a122. One of the main problems in RISC processors that is addressed by ARM processor is:
A. *64 general purpose registers that can be used by the user in any operational mode*
B. *ARM has a compressed THUMB mode that reduce the code density by 30 to 40%*
C. *Complex instruction set in ARM that allows variable instruction length*
D. *All of the above*
E. *None of the above*

1a123. CUDA language is used to program GPUs, one of the main reasons to use such language instead of any other programming language because:
A. *Most other languages such as C, Java, and Fortran run serially*
B. *It is based on a parallel programming model*
C. *The need of a new language to adapt to the new processor shift from a single core to many-core*
D. *All of the above*
E. *None of the above*

1a124. CUDA architecture model uses a host and a device:
A. *The host is a GPP that runs the serial part of a program and the device is a GPU that runs the parallel part of the program*
B. *The host is a GPU that runs the serial part of a program and the device is a GPP that runs the parallel part of the program*
C. *Host and device can be used independently from the nature of the code (whether serial or parallel) without any implications on the overall performance*
D. *All of the above*
E. *None of the above*

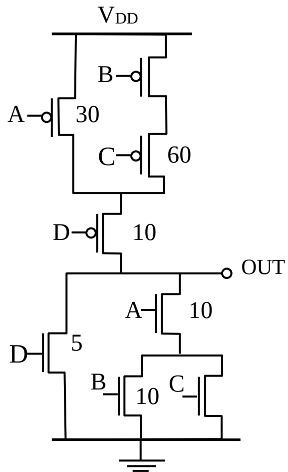
1a125. In which region of operation a MOSFET is usually used in digital circuits?
A. *Cut-off and Saturation regions*
B. *Saturation and triode regions*
C. *Cut-off and triode regions*
D. *Saturation region only*
E. *None of the above*

1a126. Find the Boolean function OUT implemented by the CMOS structure shown in this figure.



A. $OUT = \overline{A(B+C)+D}$
B. $OUT = \overline{B(A+C)+D}$
C. $OUT = \overline{C(B+A)+D}$
D. $OUT = \overline{D(A+C)+B}$
E. *None of the above*

1a127. Find the missing ratios of p-MOS and n-MOS transistors that guarantee the worst-case delay in this circuit.

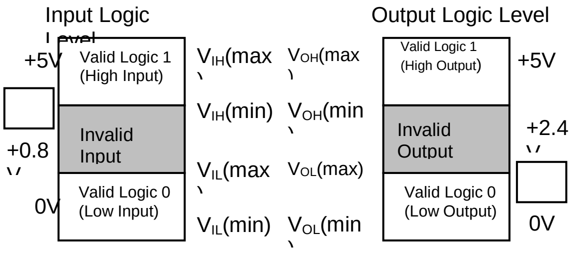


A. *B = 30, C = 5*
B. *B = 60, C = 5*
C. *B = 30, C = 10*
D. *B = 60, C = 10*
E. *None of the above*

1a128. In this figure, if the noise margin of the standard logic gate is $N_{MH} = N_{ML} = 0.4$ V, find V_{OL} (max) and V_{IH} (min)?

A. $V_{OL}(max) = 0.6V$ and V_{IH} $(min) = 1.6V$
B. $V_{OL}(max) = 0.4V$ and V_{IH} $(min) = 2.0V$
C. $V_{OL}(max) = 0.2V$ and V_{IH} $(min) = 2.0V$
D. $V_{OL}(max) = 0.4V$ and V_{IH} $(min) = 2.2V$
E. None of the above

Standart TTL Logic Gate Characteristics



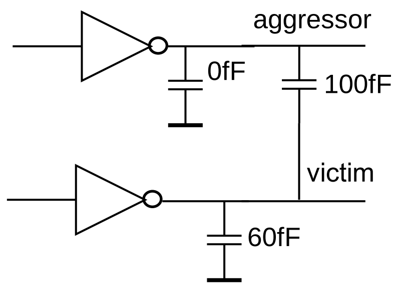
1a129. What does ECL abbreviation stand for?

A. Enhanced Conductive Logic
B. Emitter Coupled Logic
C. Emissive Conductive Logic
D. Early Conductive logic
E. None of the above

1a130. Which of the following is a characteristic that identifies ECL?

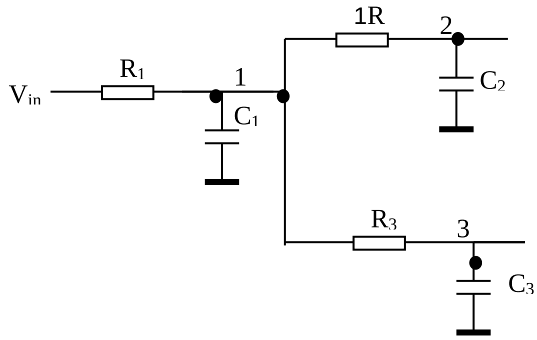
A. High Conductivity
B. Low Emission
C. Early conduction
D. Complementary outputs
E. None of the above

1a131. For the shown circuit, define victim line effective capacitance for delay calculation in case of aggressor line switching in opposite direction.



A. 160fF
B. 210 fF
C. 260 fF
D. 110fF
E. 150fF

1a132. In the circuit below the Elmore model delay from source to node 2 is defined as:



F. $R_1(C_1+C_2+C_3)$
G. $R_1C_1+R_2C_2$
H. $R_1(C_1+ C_3)+(R_1+R_2)C_2$
I. $R_1(C_1+C_2)+ R_2(C_1+C_3)$
J. $R_1(C_1+C_3)+ R_2(C_1+C_2)$

1a133. In digital circuits, nMOS transistor's

A. Delays are independent of supply voltage
B. The lowest potential is usually given to substrate
C. Threshold voltage is directly proportional to the transistor delay
D. Delays are independent of temperature
E. Resistance is independent of on threshold voltage

1a134. At switching of CMOS inverter's input voltage, the current amplitude of source-ground short connection, depending on load capacitance:

A. Increases
B. Decreases
C. Does not depend on load capacitance
D. Changes polarity
E. Doubles

1a135. How many NMOS transistors does SRAM 6T cell have?

A. 4
B. 3
C. 2
D. 1
E. 6

1a136. Signal rise speed of output buffer is proportional to

A. Output resistance
B. Load capacitance
C. Supply voltage
D. Input signal rise time
E. Incoming signal fall time

1a137. Noise level in supply buses is

A. Proportional to bus conductance
B. Proportional to bus inductance
C. Proportional to bus capacitance
D. Proportional to bus delay
E. Constant

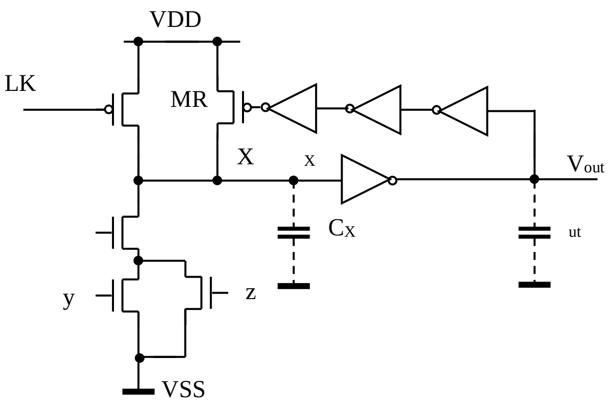
1a138. Differential signaling, in comparison to single-ended signaling

A. Increases the level of electromagnetic radiation
B. Decreases noises of supply buses, occurred due to signal switching
C. Increases the sensitivity to external noise
D. Increases delays
E. Decreases line resistance

1a139. For efficient IC protection, the protective circuits towards ESD current should have:

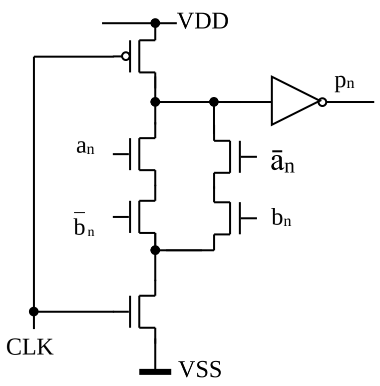
A. Small resistance
B. Large resistance
C. Small capacitance
D. Large inductance
E. Little losses

1a140. What logic function is implemented?



A. !(x(y+z))
B. x(y+z)
C. x+yz
D. !x+yz
E. !xy+z

1a141. What logic function is implemented?



A. $p_n=a_n\oplus b_n$
B. $p_n=!(a_n\oplus b_n)$
C. $p_n=!a_n\oplus b_n$
D. $p_n=!a_nb_n$
E. $p_n=!a_n+b_n$

1a142. Define the maximum permissible absolute value of noise, imposed on logic 1 in inputs of a CMOS inverter if the supply voltage is 1 V, inverter's VTC transient domain is within [0.3V-0.6V] range of input voltage.

A. 0.3 V
B. 0.6 V
C. 0.4 V
D. 0.7 V
E. 0.5 V

1a143. Considering that the inputs of NOR3 cell are independent and equally distributed, which is the probability of output switching?

A. 7/64
B. 1/8
C. 3/8
D. 3/32
E. 3/16

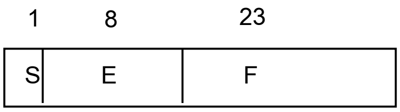
1a144. The instruction set of a processor contains 200 instructions. Number of general purpose registers (GPRs) is 64. The total size of addressable memory is 4 MB. Absolute memory addressing is used. Determine the length of the instruction format "register- memory".

A. 24
B. 32
C. 36
D. 54
E. The correct answer is missing

1a145. Signed integers A and B in a hexadecimal system are represented as follows: A = ABC9971E, B = 45A08B6F. Which option corresponds to the sum of these numbers C = A + B (the result is also represented in hexadecimal system).

A. 2528D020
B. F16A228D
C. 361A902E
D. 2A6 BC2D
E. The correct answer is missing

1a146. Which of the presented variants is considered - 0,5 number representation by ordinary accuracy single precision floating point format (standard IEEE 754)? The results are presented in hexadecimal system.



A. 1284 F000
B. BF00 0000
C. BF80 0000
D. 3F00 0000
E. The correct answer is missing

1a147. How many add address inputs does a 512 MB DRAM circuit have?

A. 29
B. 14
C. 15
D. 16
E. The correct answer is missing

1a148. ROM 64Kx16 circuit remembers whole 8-bit without sign numbers multiplication program. Which code will be registered in the cell of 2313 address? The answers are presented in decimal system.

A. 120
B. 81
C. 35
D. 80
E. The correct answer is missing

1a149. In a 6-bit counter 101010 code is preliminary registered. What will the state of the counter be if 6 clock signal is inserted to its syncro-input.

A. 110110
B. 010101
C. 101010
D. 001001
E. The correct answer is missing

1a150. Which phase of IC synthesis the sizes of transistor's gate are defined in?

A. Conceptual
B. Structural
C. Parametrical
D. Logic
E. Physical

1a151. An embedded system is:

A. Computer hardware and additional mechanical parts designed to perform a specific function
B. Computer hardware and software designed to perform a specific function
C. A combination of computer hardware, software and additional mechanical or other parts, designed to perform a specific function
D. A general-purpose computing machine similar to PC
E. Correct answer is missing

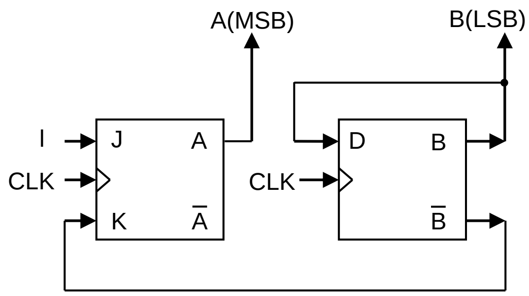
1a152. Consider the following Karnaugh map:

AB \ CD	00	01	11	10
00	1			1
01	1	1	1	1
11				
10	1			1

Which logic function best represents a minimal SOP expression?

A. $f(A,B,C,D)=\overline{B}\,\overline{D}+\overline{A}B+\overline{A}\,\overline{D}$
B. $f(A,B,C,D)=\overline{A}\,\overline{D}+\overline{A}B+A\overline{B}\,\overline{D}$
C. $f(A,B,C,D)=\overline{A}\overline{D}+\overline{A}BD+A\overline{B}\,\overline{D}$
D. $f(A,B,C,D)=\overline{B}\,\overline{D}+\overline{A}B$
E. Correct answer is missing

1a153. Flip-flops A and B form a sequential synchronous circuit as shown below.



After the clock pulse, binary count 10 (A=1, B=0) changes to:

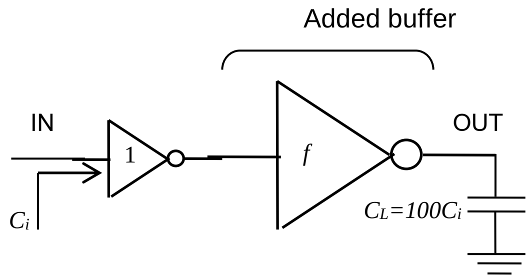
A. 00
B. 01
C. 10
D. 11
E. The correct answer is missing

1a154. For a piece of wire in CMOS technology, if all dimensions are kept constant and only its length (L) doubles, how will its delay change?

A. Wire delay doubles (twice increase)
B. Wire delay quadruples (4 times increase)
C. Wire delay halves (twice decrease)
D. Wire delay does not change
E. The correct answer is missing

For the questions **1a155.** and **1a156.** consider the following circuit.

An inverter of minimum size (with input capacitance of C_i) driving a load C_L where $C_L = 100 \times C_i$. It is required to introduce another inverter (f times larger than the first one) between the minimum sized inverter and the load C_L. The propagation delay of an unloaded minimum size inverter is assumed 20ps (t_{p0}=20 ps).



1a155. What should f be to minimize the overall propagation delay (from IN to OUT)? How much is the minimum overall propagation delay in this case (t_p)?

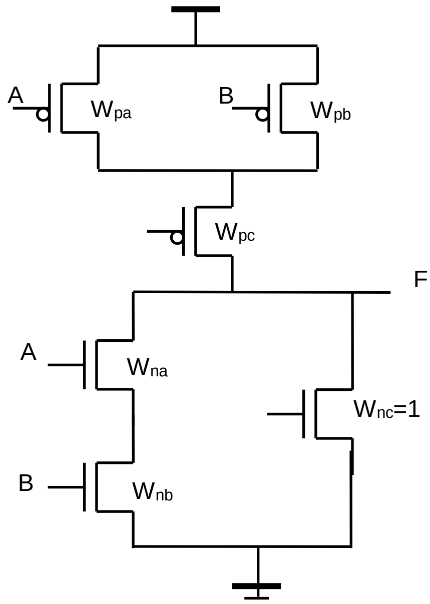
A. f=5 t_p=120 ps
B. f=5 t_p=240 ps
C. f=10 tp=440 ps
D. f=10 t_p=220 ps
E. the correct answer is missing

1a156. If any number of stages could be added to minimize the overall delay, how many TOTAL inverters will be in the circuit (N) and approximately how much would be the minimum propagation delay in this case (t_p)?

A. N=4 tp=333ps
B. N=4 t_p=63ps
C. N=5 t_p=351ps
D. N=5 t_p=70ps
E. The correct answer is missing

For the questions **1a157.** and **1a158.** consider the following circuit.

Assume all transistors are assigned minimum channel length. The parameters shown on the schematic represent normalized widths of the transistors with respect to the width of the NMOS transistor C (W_{nc}=1). Assume the NMOS/PMOS mobility ratio is 2 (K'_n/K'_p=2).



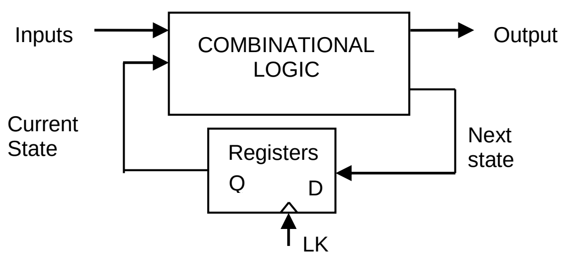
1a157. What is the logic function implemented by this circuit?

A. $F = \overline{A + BC}$
B. $F = \overline{AB + C}$
C. $F = \overline{(A + B)C}$
D. $F = \overline{A(B + C)}$
E. The correct answer is missing

1a158. Which transistor sizing is optimal for obtaining symmetric delay response (equal high-to-low and low-to-high delay)?

A. $W_{na}=W_{nb}=2$ $W_{pa}=W_{pb}=4$ $W_{pc}=8$
B. $W_{na}=W_{nb}=4$ $W_{pa}=W_{pb}=W_{pc}=8$
C. $W_{na}=W_{nb}=2$ $W_{pa}=W_{pb}=W_{pc}=4$
D. $W_{na}=2$ $W_{nb}=4$ $W_{pa}=W_{pb}=W_{pc}=4$
E. The correct answer is missing

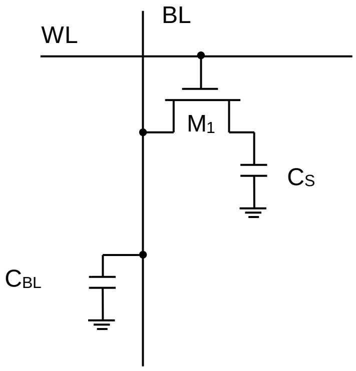
1a159. Consider the following sequential circuit. The worst case propagation delay of the combinational logic block is 400ps. The registers are positive edge triggered registers with the following delay characteristics: setup time=20ps, hold time=10ps, and clock-to-q delay=80ps.



What is the maximum clock frequency that this circuit can operate successfully without any timing failures?

A. 1 GHz
B. 1.96 GHz
C. 2.04 GHz
D. 2 GHz
E. The correct answer is missing

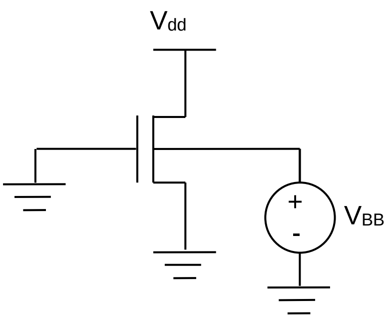
1a160. Consider DRAM based on 1-Transistor DRAM cell and operating at VDD = 2.5 V. Threshold voltage of NMOS is 0.5 V and precharge voltage of bitline is 1.25 V. Cell storage capacitance is 50 fF and the bit-line capacitance is 1 pF.



How much voltage swing is created on the bitline when a cell storing ‘1’ is accessed for the read operation?

A. 47.6 mV
B. 35.7 mV
C. 59.5 mV
D. 119 mV
E. The correct answer is missing

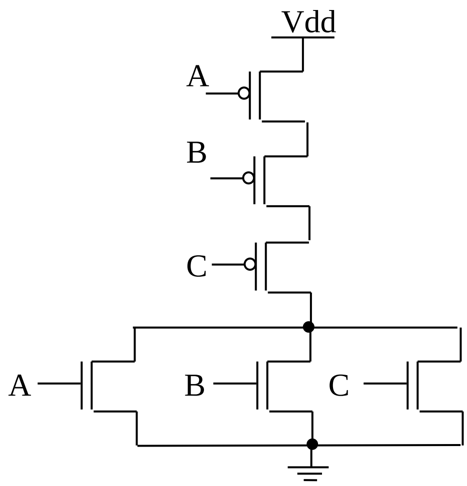
1a161. Consider the following transistor which is in the off condition (V_{gs}=0<V_t=0.2 and V_{dd}=1V). Assume subthreshold and junction leakage components are both considerable.



by applying negative V_{BB}:

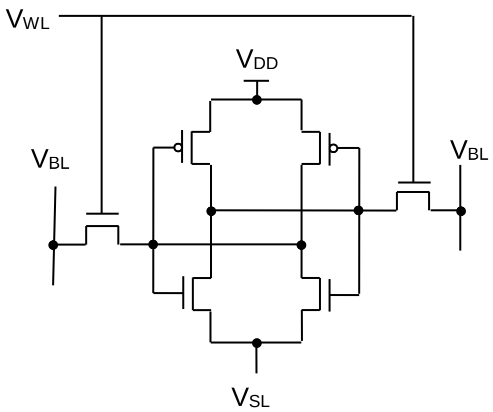
A. Both subthreshold and junction leakage decrease
B. Subthresold leakage decreases and junction leakage increases
C. Subthreshold leakage increases and junction leakage decreases
D. Both subthrehsold and junction leakage increase
E. The correct answer is missing

1a162. Consider the following 3-input NOR gate. Assume NMOS and PMOS have same threshold voltage and the leakage is dominated by subthreshold leakage. Which input state is most likely to result in minimum leakage for the NOR gate in the standby mode?



A. ABC=000
B. ABC=100
C. ABC=011
D. ABC=111
E. The correct answer is missing

1a163. Consider the following SRAM cell in the standby condition. Which biasing will result in the least leakage without losing the state of the cell?



A. V_{DD}=1V V_{SL}=0V V_{WL}=0V V_{BL}=1V
B. V_{DD}=1V V_{SL}=0V V_{WL}=-0.1V V_{BL}=1V
C. V_{DD}=1V V_{SL}=0.5V V_{WL}=0V V_{BL}=1V
D. V_{DD}=0.5V V_{SL}=0.5V V_{WL}=0V V_{BL}=0.5V
E. The correct answer is missing

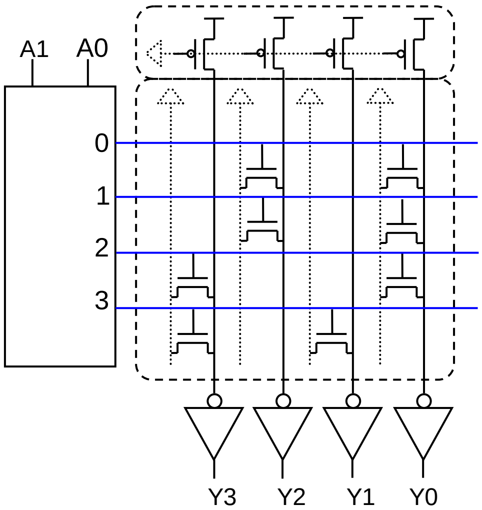
1a164. What does the Verilog code below describe?

```
always @(posedge C or posedge CLR)
begin
        if (CLR)
           Q <= 1'b0;
        else
           Q <= IN;
end
```

A. A D flip-flop with positive edge clock and synchronous reset
B. A D flip-flop with positive edge clock and asynchronous reset
C. A T flip-flop with positive edge clock and synchronous reset
D. A T flip-flop with positive edge clock and asynchronous reset
E. Correct answer is missing

1a165. The figure below shows a 4-word × 4-bit ROM. Use it to answer the following questions. In binary, what is the data stored at address 3?

A. 0101
B. 1010
C. 1100
D. 0011
E. The correct answer is missing



1a166. If the inverter delay is 100 ps, what is the frequency of a 25-stage ring oscillator?

A. 10 GHz
B. 100 MHz
C. 200 MHz
D. 400 MHz
E. The correct answer is missing

1a167. What devices do EEPROM cells use internally (inside the chip) to make them programmable?

A. Fuses
B. SRAM cells
C. Floating gate transistors
D. DRAM cells
E. The correct answer is missing

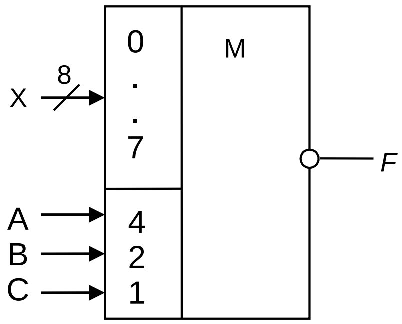
1a168. Which type of memory is used in on-chip high-speed microprocessor caches?

A. SRAM
B. DRAM
C. FRAM
D. SDRAM
E. The correct answer is missing

1a169. Consider a 16x1 unfooted non-inverting domino multiplexer implemented using four 4-input dynamic multiplexers and a single static CMOS logic gate. The static CMOS logic gate that should be used is:

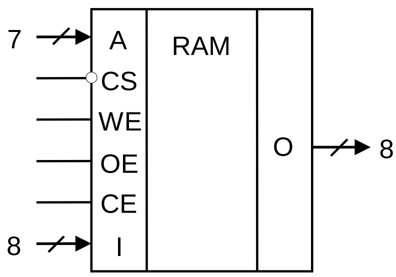
A. NOR
B. OR
C. NAND
D. AND
E. The correct answer is missing

1a170. What is the eight-bit code X (x_7 ... x_0) that must be submitted to the inputs of the multiplexer to implement the logical function $F = AB\overline{C} + A\overline{B}C + \overline{A}BC$?



A. 01101000
B. 00010110
C. 10010111
D. 11101001
E. The correct answer is missing

1a171. Specify the ROM capacity in bits.



A. 128

B. 256
C. 512
D. 1024
E. 2048

1a172. Which of these Verilog implementations are synthesized into RTL description without errors or mismatches?
A.

```
always @ (posedge SCLK or posedge RESET or posedge SS) begin

  if (~RESET) begin

      shift_register[7:0]    <= 8'b0;

  end else if (~SS) begin

      shift_register[7:0]    <= 8'b0;

  end else begin

      shift_register         <= shift_register << 1;

      shift_register[0]      <= MOSI;

  end

end
```

B.

```
always @ (posedge SCLK or negedge RESET ) begin

  if (~RESET) begin

      shift_register[7:0]     = 8'b0;

  end else if (SS) begin

      shift_register[7:0]     = 8'b0;

  end else begin

      shift_register          = shift_register << 1;

      shift_register[0]= MOSI;

  end

end
```

C.

```
always @ (posedge SCLK or negedge RESET or posedge SS) begin

  if (~RESET) begin

      shift_register[7:0]<= 8'b0;

  end else if (SS) begin

       shift_register[7:0]   <= 8'b0;

  end else begin

      shift_register         <= shift_register << 1;

      shift_register[0]      <= MOSI;

  end

end
```

D.

```
always @ (posedge SCLK or negedge RESET or posedge SS) begin

  if (~RESET) begin

      shift_register[7:0]= 8'b0;

  end else if (SS) begin

      shift_register[7:0]= 8'b0;

  end else begin

      shift_register         <= shift_register << 1;

      shift_register[0] = MOSI;

  end

end
```

E. Correct answer is missing

1a173. What is the aspect ratio of channel width to length of n-MOS transistor for the following parameters: g_m=1.2 mA/V, V_{th}=0.5V, V_{gs}=2V, V_{ds}=1V, k_n=120μA/V^2.
A. 5
B. 10
C. 15
D. 20
E. The correct answer is missing

1a174. What statement describes properties of equipments made using standard integrated circuits?
A. Easy to copy, slow prototyping, small number of soldering pins,

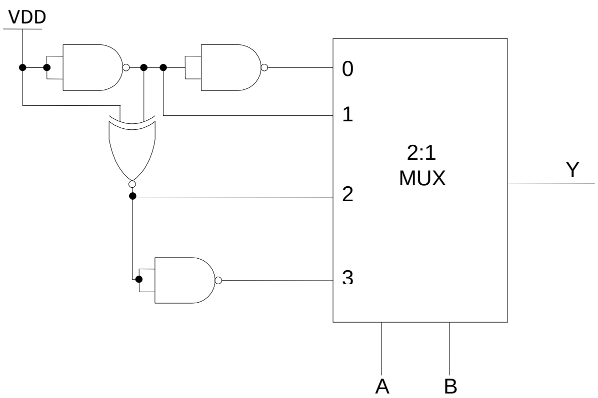
require larger PCB than ASIC, cost effective for large volume production
- B. *Easy to copy, fast prototyping, large number of soldering pins, require larger PCB than ASIC, cost effective for small volume production*
- C. *Easy to copy, fast prototyping, small number of soldering pins, require smaller PCB than ASIC, cost effective for large volume production*
- D. *Difficult to copy, slow prototyping, large number of soldering pins, require larger PCB than ASIC, cost effective for large volume production*
- E. *Difficult to copy, fast prototyping, large number of soldering pins, require smaller PCB than ASIC, appropriate for small volume production*

1a175. To obtain minimum delay CMOS inverter, the ratio between pMOS and nMOS width (W_p/W_n) should be:
- A. μ_n/μ_p
- B. μ_p/μ_n
- C. $\sqrt{\mu_n/\mu_p}$
- D. $\sqrt{\mu_p/\mu_n}$
- E. *1*

1a176. The final result of AC analysis for a linear circuit depends on:
- A. *Time step*
- B. *Initial condition*
- C. *Criteria for iterative loop termination*
- D. *Correct answers are A. and B.*
- E. *None of the above*

1a177. If one input of an OR2 cell is at logic 1 and another transits from 1 to 0, then:
- A. *There is a bus conflict*
- B. *There is an illegal input*
- C. *an event occurs*
- D. *A neutral event occurs*
- E. *The correct answer is missing*

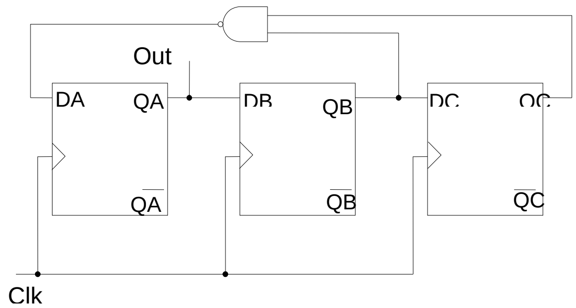
1a178. The logic function implemented by the circuit below is (VDD implies a logic “1”):



- A. *Y=NAND(A,B)*
- B. *Y=NOR(A,B)*
- C. *Y=XNOR(A,B)*
- D. *Y=XOR(A,B)*
- E. *The correct answer is missing*

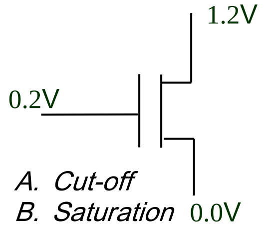
1a179. The minimum number of 2-input NOR gates required to implement the Boolean function $Z = \overline{A}B\overline{C}$, assuming that *A, B* and *C* are available is:
- A. *Three*
- B. *Four*
- C. *Five*
- D. *Six*
- E. *Seven*

1a180. Assuming that all the flip-flops are in the reset condition initially, the sequence observed at the output pin in the circuit shown below is:



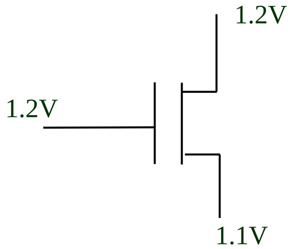
- A. *011100….*
- B. *001110….*
- C. *000111….*
- D. *010101….*
- E. *The correct answer is missing*

1a181. For the circuit shown below determine the operating mode if V_{T0}=0.4V.



- A. *Cut-off*
- B. *Saturation*
- C. *Linear*
- D. *Triode*
- E. *Diode*

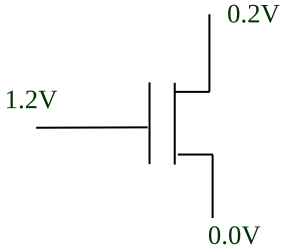
1a182. For the circuit shown below determine the operating mode if V_{T0}=0.4V.



- A. *Cut-off*

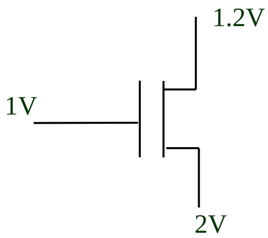
B. *Saturation*
C. *Linear*
D. *Semi-open*
E. *Diode*

1a183. For the circuit shown below determine the operating mode if V_{T0}=0.4V.



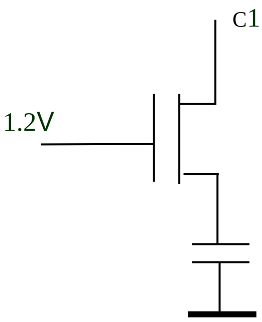
A. *Cut-off*
B. *Saturation*
C. *Linear*
D. *Semi-close*
E. *Diode*

1a184. For the circuit shown below determine the operating mode if V_{T0}=0.4V.



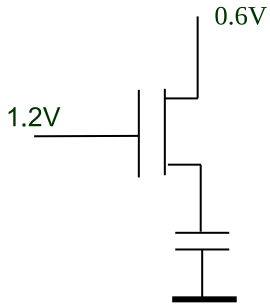
A. *Cut-off*
B. *Saturation*
C. *Linear*
D. *Semi-open*
E. *Diode*

1a185. For the circuit shown below determine the steady state voltage across the capacitor. Assume the capacitor was initially discharged and V_{T0}=0.4V.



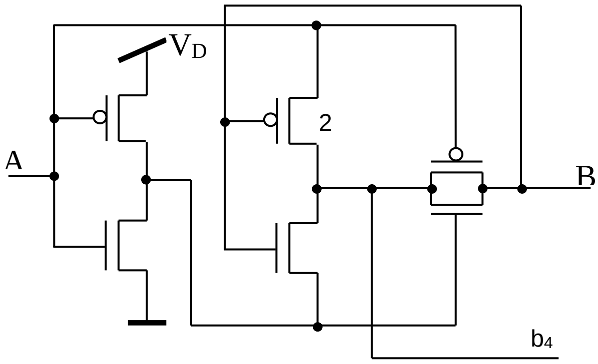
A. *0 V*
B. *0.8 V*
C. *1.2 V*
D. *1.0 V*
E. *0.2 V*

1a186. For the circuit shown below determine the steady state voltage across the capacitor. Assume the capacitor was initially discharged and V_{T0}=0.4V.



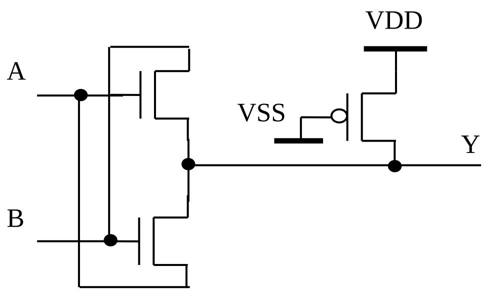
A. *0 V*
B. *0.8 V*
C. *0.6 V*
D. *1.2 V*
E. *0.2 V*

1a187. What is the logic function performed by this circuit with A and B inputs?



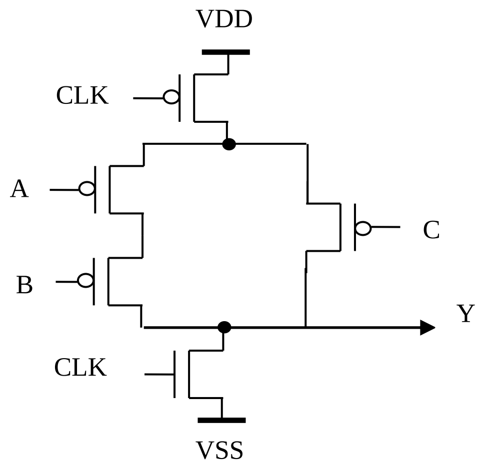
A. *Y=A⊕B*
B. *Y=A+B*
C. *Y=A&B*
D. *Y=!(A&B)*
E. *Y=!(A+B)*

1a188. What is the logic function performed by this circuit?



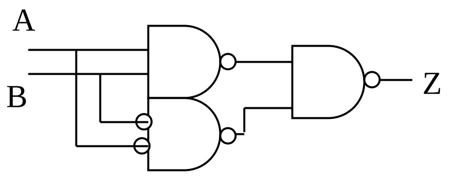
A. *Y=A&B*
B. *Y=!(A+B)*
C. *Y= A⊕B+1*
D. *Y= A⊕B*
E. *Y=A+B*

1a189. What is the logic function performed by this circuit?



A. $Y=C+AB$
B. $Y=!(C(A+B))$
C. $Y=!(C+AB)$
D. $Y=C(A+B)$
E. $Y=0$

1a190. What formula describes the given circuit?



A. Z=A&B+(!A&!B)
B. Z=(!A&B)+(!B&A)
C. Z=!A&B
D. Z=A&(!B)
E. Z=A+!B

1a191. Considering that memory array has equal number of 1-bit cells in lines and columns, define the number of word lines if the total number of address bit memory is 11, and the number of the word bit memory is 8.

A. 32
B. 64
C. 128
D. 256
E. 512

1a192. Which is the basic consequence of MOS transistor's degradation due to hot carriers?

A. The increase of threshold voltage
B. The decrease of threshold voltage
C. The increase of channel resistance
D. The decrease of channel resistance
E. The decrease of drain-package disruption voltage

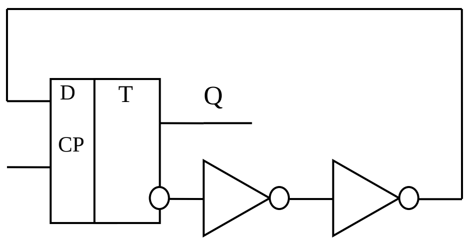
1a193. In what case is the short connection current missing in a CMOS inverter?

A. $V_{tp}=V_{tn}$
B. $V_{tp}+V_{tn}=0$
C. $V_{tp}+V_{tn}<VDD$
D. $|V_{tp}|+V_{tn}<VDD$
E. $|V_{tp}|+V_{tn}<VDD/2$

1a194. C capacitance is connected to the end of interconnect line with L length, line parameters are c [F/m], r [Ohm/m]. By what formula is the signal delay time in the line given?

A. 0.7rc
B. 0.7Lr(C+c)
C. 0.7Lr(C+Lc/2)
D. 0.7Lr(C+Lc)
E. 0.7Lr(C/2+Lc/2)

1a195. The figure shows the circuit of a frequency divider.



What expression gives the minimum period of clock pulses?

A. $T_{min}=t_{su}+t_{c2q}+2t_{pinv}$
B. $T_{min}= t_{c2q}+2t_{pinv}$
C. $T_{min}=t_{su}+t_{hd}+t_{c2q}+2t_{pinv}$
D. $T_{min}= t_{hd}+t_{c2q}+2t_{pinv}$
E. $T_{min}= t_{su}+t_{hd}+2t_{pinv}$

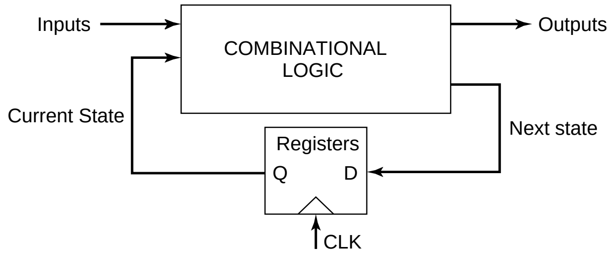
1a196. Which one of the given expressions is wrong?

A. A⊕!B = !A⊕B
B. 1⊕!B⊕A = B⊕A
C. A⊕B =! A⊕!B
D. A⊕!B = !A⊕!B
E. !A⊕B = !(A⊕B)

1a197. Which of three types of SystemC processes is part of the synthesizable subset of SystemC?

A. sc_method
B. sc_thread
C. sc_cthread
D. sc_method and sc_cthread
E. The correct answer is missing

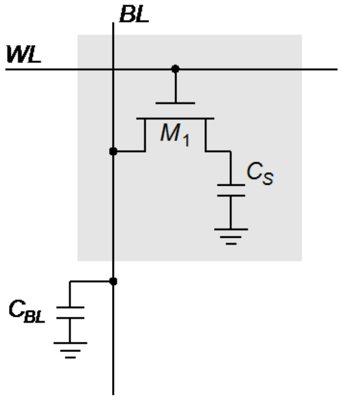
1a198. Consider the following sequential circuit. The worst case propagation delay of the combinational logic block is 400ps. The registers are positive edge triggered registers with the following delay characteristics: setup time=20ps, hold time=10ps, and clock-to-q delay=80ps.



What is the maximum clock frequency that this circuit can operate successfully without any timing failures?

A. 2 GHz
B. 1 GHz
C. 1.96 GHz
D. 2.04 GHz
E. 5 GHz

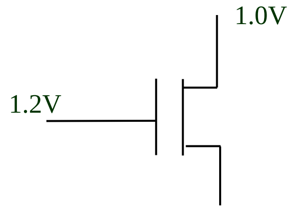
1a199. Consider DRAM based on 1-Transistor DRAM cell and operating at VDD = 2.5 V. Threshold voltage of NMOS is 0.5 V and precharge voltage of bitline is 1.25 V. Cell storage capacitance (C_S) is 50 fF and the bit-line capacitance (C_{BL}) is 1 pF.



How much voltage swing is created on the bitline when a cell storing '1' is accessed for the read operation? Ignore the body effect of the access transistor (M1).

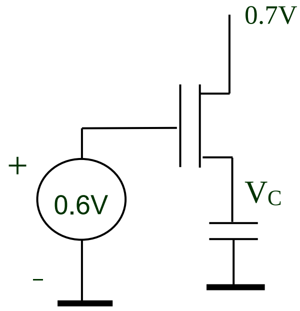
A. 47.6 mV
B. 35.7 mV
C. 59.5 mV
D. 119 mV
E. 98 mV

1a200. For the circuit shown below determine the operating mode if V_{T0}=0.5 V.



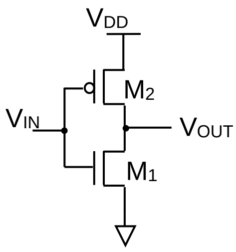
A. Triode
B. Cut-off
C. Linear
D. Saturation
E. None

1a201. For the circuit shown below determine the steady state voltage across the capacitor. Assume the capacitor was initially discharged and V_{T0}=0.4V .



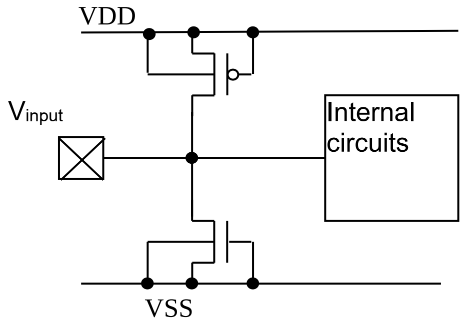
A. 0V
B. 0.2V
C. 0.6V
D. 0.7V
E. 0.4V

1a202. Mark the correct answer if V_{IN}=V_{DD}.



A. M1-in saturation mode, M2-linear mode
B. M1-linear mode, M2-linear mode
C. M1-cut off mode, M2-saturation mode
D. M1- saturation mode, M2- saturation mode
E. None of the above

1a203. Assuming that a p-n junction forward bias voltage is V_{pn}, what is the input voltage maximum safe margin?



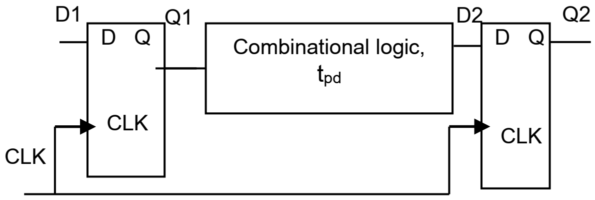
A. $VSS \le V_{in} \le VDD$
B. $VSS\text{-}V_{tn} \le V_{in} \le VDD\text{-}V_{tp}$
C. $VSS+V_{tn} \le V_{in} \le VDD+V_{tp}$
D. $VSS\text{-}V_{pn} \le V_{in} \le VDD+V_{pn}$
E. $VSS+V_{pn} \le V_{in} \le VDD+V_{pn}$

1a204. Before reading from SRAM cell, BL and $\overline{BL}$ bitlines should:
A. *Discharge to VSS*
B. *Discharge to V_t*
C. *Charge to VDD*
D. *Charge to VDD/2*
E. *BL charge to VDD, $\overline{BL}$ charge to VSS*

1a205. Which of the given expressions is wrong?
A. *A⊕!B = !(A⊕!B)*
B. *1⊕!B⊕A = B⊕A*
C. *A⊕B =! A⊕!B*
D. *A⊕!B = A⊕!B*
E. *!A⊕B = !(A⊕B)*

1a206. What equation describes the state equation of JK flip-flop?
A. Q^+*=Q&J + !Q&K*
B. Q^+*=!Q&J + Q&!K*
C. Q^+*=!Q&J + Q&K*
D. Q^+*=Q&!J + !Q&K*
E. Q^+*=Q&J + !Q&!K*

1a207. What expression gives the minimum period of clock pulses for the proper operation of the below shown circuit?



A. $T_{min}=t_{su}+t_{c2q}+t_{pd}$
B. $T_{min}= t_{c2q}+t_{pinv}$
C. $T_{min}=t_{su}+t_{hd}+t_{c2q}+t_{pd}$
D. $T_{min}= t_{hd}+t_{c2q}+t_{pd}$
E. $T_{min}= t_{su}+t_{hd}+t_{pd}$

1a208. In a short channel MOS transistor the drain current saturation, due to velocity saturation with source drain voltage increase, occurs:
A. *When at drain the channel density becomes 0*
B. *Later than at drain the channel density becomes 0*
C. *Later than at drain the channel density becomes 1*
D. *When drain-source voltage equals source-body voltage*
E. *When drain-body junction is disrupted*

1a209. In deep submicron MOS transistor channel, the mobility of free charge carriers depredates due to:
A. *Increase in horizontal field*
B. *Increase in vertical field*
C. *Increase in threshold voltage*
D. *Decrease in threshold voltage*
E. *Decrease in gate capacitance*

1a210. By what law does the sub-threshold current of an MOS transistor change, depending on the gate voltage?
A. *Exponential*
B. *Linear*
C. *By square law*
D. *By 3/2 law*
E. *By 2/3 law*

1a211. Trapped charges in the gate oxide of an MOS transistor:
A. *Decrease threshold voltage*
B. *Increase threshold voltage*
C. *Increase drain-bulk leakage current*
D. *Decrease drain-bulk leakage current*
E. *Decrease source-drain bias*

1a212. Due to the increase in the load capacitance of an inverter, the crowbar current:
A. *Increases*
B. *Does not change*
C. *Decreases*
D. *Tends to the load current*
E. *Changes its direction*

1a213. Assuming k_n=1.5k_p, in what case in a NOR2 cell the pull-up and pull-down impedances are equal?
A. $W_p=3W_n$
B. $W_p=1.5W_n$

C. $W_p=W_n$
D. $W_p=9W_n$
E. $W_p=6W_n$

1a214. On what does the threshold voltage of a MOS transistor not depend?
A. Channel length
B. Thickness of gate oxide
C. Difference of output operations of gate and body materials
D. Gate voltage
E. Density of trapped charge in in the gate oxide

1a215. On what does the noise, occurring during signal transfer between ICs, not depend?
A. Transition line length
B. Signal increase velocity
C. Supply voltage of IC core
D. Internal resistance of signal source
E. Equivalence resistance of transition line

1a216. What form of Boolean function representation is not canonical (unique)?
A. ROBDD for a given order of variables
B. Minimal representation of a Boolean function
C. Polynomial form of representation functions (polynomial Zhegalkin)
D. Representation in the form of the truth table
E. None of the above

1a217. How many states does the feedback sequential circuit with 3 feedback loops have?
A. A. 3
B. B.4
C. 8
D. 5
E. There is no right answer

1a218. What function is implemented by device, the Verilog code of which is given below.

```
module   comb_circuit (din, dout);
    input [0:3] din;
output reg [0:3] dout;
always @(in)
casex(in)
4'b1xxx: dout=4'b1000;
4'b01xx: dout=4'b0100;
4'b001x: dout=4'b0010;
4'b0001: dout=4'b0001;
default: dout=4'b0000;
endcase
endmodule
```

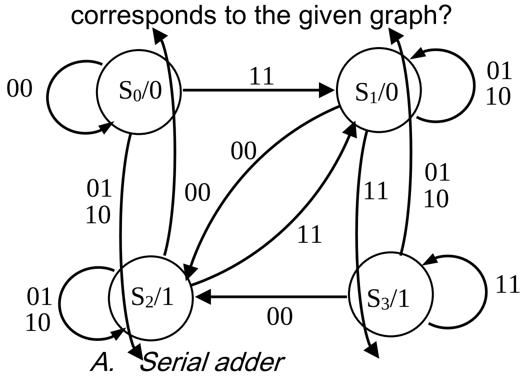
A. Priority encoder
B. Demultiplexer
C. Priority function
D. Decoder
E. None of the above

1a219. How many bits will an instruction contain, the format of which is given below, if the number of operations of a processor is equal to 120 and the number of general purpose registers (GPRs) is 128.

Op.code	r1	r2	r3

A. 64
B. 28
C. 24
D. 50
E. None of the above

1a220. A graph of the Moore FSM is given. Input alphabet X = {00,01,10,11}. Output alphabet Y = {0,1}
Which of the following devices corresponds to the given graph?



A. Serial adder
B. Serial subtractor
C. Two-bit up counter
D. Detector of input sequence 11,00,11,01
E. None of the above

1a221. Which device meets the following Verilog description?

```
module  comb (X,S,Y);
input [15:0] X;
input [3:0] S;
output [15:0] Y;
wire [15:0] T;
 assign {T,Y}={X,X} >>S;
endmodule
```

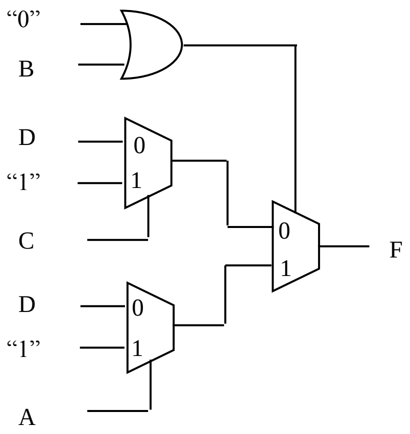
A. 16-bit barrel shifter
B. 32-bit shift register
C. Multiplexer
D. Demultiplexer

E. None of the above

1a222. What type of configuration memory is used in FPGA Xilinx Virtex-7?

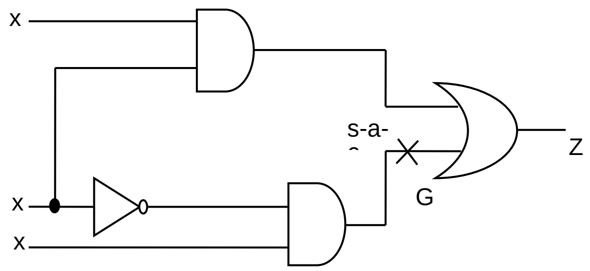
A. Flash-based memory
B. SRAM-based
C. Based on EEPROM
D. Anti-fuse
E. None of the above

1a223. What function is implemented by the given function block to present function in DNF?



A. $\bar{c}d + ab + \bar{a}c$
B. $\bar{b}c + ba + d$
C. $ab + \bar{a}dc$
D. $ab + dc$
E. None of the above

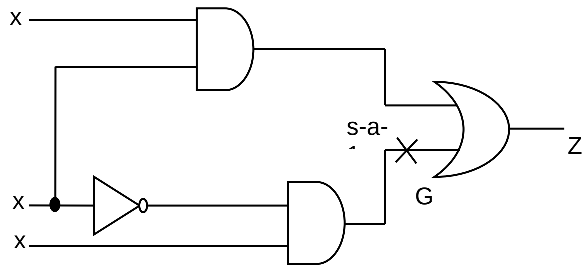
1a224. Among the test patterns listed below which one is a detection test for stuck-at-0 fault on line G?



A. (0,0,0)
B. (1,1,1)
C. (0,1,1)
D. (1,0,1)
E. (0,1,0)

1a225. In the circuit below which one of the listed patterns is a test for detection of the stuck-at-1 fault on line G?

A. (1,1,0)
B. (0,0,1)
C. (1,0,1)
D. (1,0,0)
E. (1,1,1)



1a226. Among the following well-known traditional test algorithms for testing n-cell memories which one is of linear complexity, in general?

A. GALPAT
B. Walking 1/0
C. Checkerboard
D. Sliding Diagonal
E. GALRow

1a227. What structure should n-cell memory have for the GALRow algorithm operation to have linear complexity?

A. ✓n x ✓n
B. 1 x n
C. n x 1
D. O(n) x O (1)
E. O(n) x o(1)

1a228. Metastability is:

A. Quasi-stable state of storage elements
B. Stable state of storage elements
C. A and B
D. The change of stable state of memory cells
E. None of the above

1a229. The metastability phenomenon is applicable to:

A. Analog systems
B. Digital systems
C. Mixed-signal systems
D. A and B
E. None of the above

1a230. The metastability phenomenon is applicable to:

A. Logic
B. Latch
C. Flip-flop
D. Both B and C
E. None of the above

1a231. Metastable state is a result of:

A. Unstable power
B. Stable power
C. Setup or hold time violation
D. Output overload

E. A and D

1a232. In metastable state the element's output:

A. *Can oscillate*
B. *Can have increased delay*
C. *Cannot oscillate*
D. *Both A and B*
E. *None of the above*

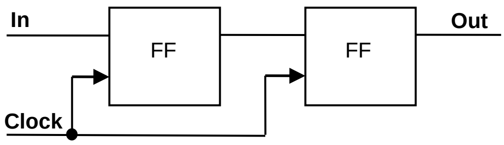
1a233. The metastable element:

A. *Will never restore stability*
B. *Will restore stability after reset only*
C. *Will restore stability after a while*
D. *Will restore stability immediately*
E. *None of the above*

1a234. To avoid metastability, a designer should:

A. *Use synchronous design techniques*
B. *Use synchronizers between clock domains*
C. *Both A and B*
D. *None of the above*
E. *A new design scheme*

1a235. The below presented clock domain synchronizer:



A. *Reduces the probability of metastability*
B. *Completely resolves the metastability problem*
C. *Increases the metastability probability*
D. *A and B*
E. *None of the above*

1a236. Clock domain is:

A. *A group of flip-flops having common clock*
B. *A group of flip-flops synchronized with rising clock edge*
C. *A group of flip-flops synchronized with falling clock edge*
D. *A and B*
E. *A and C*

1a237. Synchronous design assumes that:

A. *The design consists of clock domains*
B. *The clock domains are synchronized to avoid metastability*
C. *Clear and preset inputs are used for initialization only*
D. *Only A and B*
E. *A, B and C*

1a238. The advantage of synchronous design is:

A. *Metastability tolerance*
B. *Synthesability*
C. *High performance*
D. *Only A and B*
E. *Only A and C*

1a239. How many arbiters are needed in a bus matrix (cross-bar)?

A. *One*
B. *One per master*
C. *One per slave*
D. *One per master and one per slave*
E. *None of the above*

1a240. Which of the following flow control mechanisms for Networks-on-chip (NoCs) has the smallest requirements on buffer size?

A. *Store-and-Forward Flow Control*
B. *Virtual Cut-Through Flow Control*
C. *Wormhole Flow Control*
D. *All have same buffer requirements*
E. *None of the above*

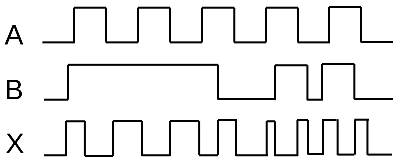
1a.241. What is the difference between $monitor, $display & $strobe?

A. *$display and $strobe display once every time they are executed, whereas $monitor displays every time one of its parameters changes*
B. *$monitor and $strobe display once every time they are executed, whereas $display displays every time one of its parameters changes*
C. *$display and $monitor display once every time they are executed, whereas $strobe displays every time one of its parameters changes*
D. *$monitor display once every time they are executed, whereas $display and $strobe displays every time one of its parameters changes*
E. *None of the above*

1a242. How many flip-flops are required to make a MOD-32 binary counter?

A. *2*
B. *4*
C. *5*
D. *8*
E. *None of the above*

1a243. The following waveform pattern is for:



A. *2-input AND gate*
B. *2-input OR gate*
C. *Exclusive-OR gate*
D. *2-input NAND gate*
E. *None of the above*

1a244. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
A. *(A > B) = 1, (A < B) = 0, (A = B) = 1*
B. *(A > B) = 0, (A < B) = 1, (A = B) = 0*
C. *(A > B) = 1, (A < B) = 0, (A = B) = 0*
D. *(A > B) = 0, (A < B) = 1, (A = B) = 1*
E. *None of the above*

1a245. When the output of the NOR gate S-R flip flop is in the HOLD state (no change), the inputs are:
A. *S=1, R=1*
B. *S=0, R=1*
C. *S=1, R=0*
D. *S=0, R=0*
E. *None of the above*

1a246. Fan-out is specified in terms of:
A. *Voltage*
B. *Current*
C. *Wattage*
D. *Unit loads*
E. *None of the above*

1a247. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?
A. *1*
B. *2*
C. *4*
D. *8*
E. *12*

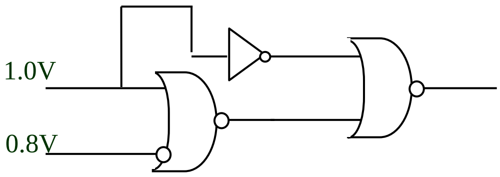
1a248. Which of the following requires refreshing?
A. *SRAM*
B. *DRAM*
C. *ROM*
D. *EPROM*
E. *None of the above*

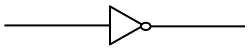
1a249. Convert decimal 153 to octal. The equivalent in octal will be:
A. *$(231)_8$*
B. *$(331)_8$*
C. *$(431)_8$*
D. *$(531)_8$*
E. *None of the above*

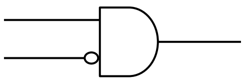
1a250 How many two-input AND and OR gates are required to implement Y=CD+EF+G?
A. *2,2*
B. *2,3*
C. *3,3*
D. *4,4*
E. *None of these*

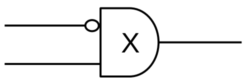
1a251. The Gray code for decimal number 6 is equivalent to:
A. *1100*
B. *1001*
C. *0101*
D. *0110*
E. *1111*

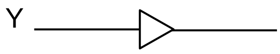
1a252. The logic circuit shown, can be minimized to:



A. 

B. 

C. 

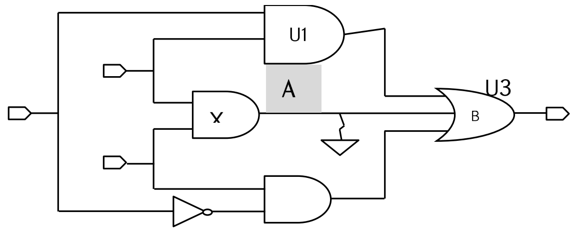
D. 

E. *None of the above*

1a253. Shifting a register content to left by one bit position is equivalent to
A. *Division by two*
B. *Addition by two*
C. *Multiplication by two*
D. *Subtraction by two*
E. *None of the above*

1a254. How many address bits are required to represent 4K memory?
A. *5*
B. *12*
C. *8*
D. *10*
E. *24*

1a255. For ATPG test, U1/Z's Stack-At 0 fault can be graded as which fault type?



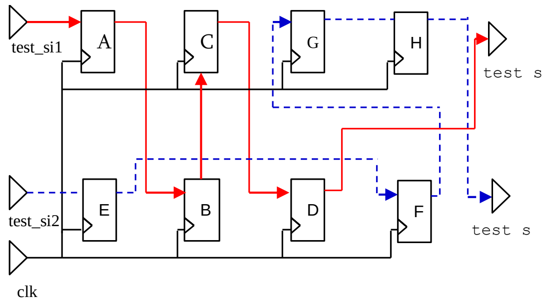
A. *Undetectable redundant*
B. *Possibly detected*
C. *Undetectable unused*
D. *Undetectable blocked*
E. *ATPG untestable*

1a256. Which option is not used for VCS interactive simulation mode?
A. *–debug_pp*
B. *–debug_all*
C. *–debug*
D. *A and C*
E. *None of the above*

1a257. Which one is not a metric of code coverage?
A. *Line*
B. *FSM*
C. *Path*
D. *Covergroup*
E. *Condition*

1a258. For the two scan-chain connections showed above and the Scandef, what will the connection be after scan-reorder?

```
DESIGN my_design ;
SCANCHAINS 2 ;
- 1
+ START PIN test_si1
+ FLOATING A ( IN SI ) ( OUT Q )
           B ( IN SI ) ( OUT Q )
           C ( IN SI ) ( OUT Q )
           D ( IN SI ) ( OUT Q )
+ PARTITION CLK_45_45
+ STOP PIN test_so1
- 2
+ START PIN test_si2
+ FLOATING E ( IN SI ) ( OUT Q )
           F ( IN SI ) ( OUT Q )
           G ( IN SI ) ( OUT Q )
           H ( IN SI ) ( OUT Q )
+ PARTITION CLK_45_45
+ STOP PIN test_so2
```

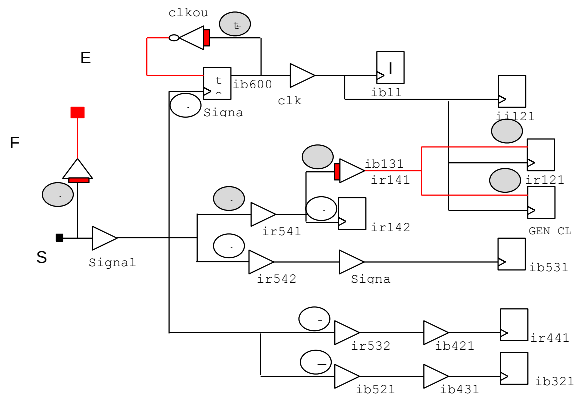


A. *test_si1-ACBD-test_so1/test_si2-EGHF-test_so2*
B. *test_si1-ACGH-test_so1/test_si2-EBDF-test_so2*
C. *test_si1-AEBC-test_so1/test_si2-GDFH-test_so2*
D. *test_si1-CABE-test_so1/test_si2-DGHF-test_so2*
E. *None of the above*

1a259. CTS tries to:

A. *Minimize skew only*
B. *Minimize skew and insertion delay*
C. *Minimize skew and maximize insertion delay*
D. *Minimize skew and meet minimum insertion delay target*
E. *Nane of the above*

1a260.

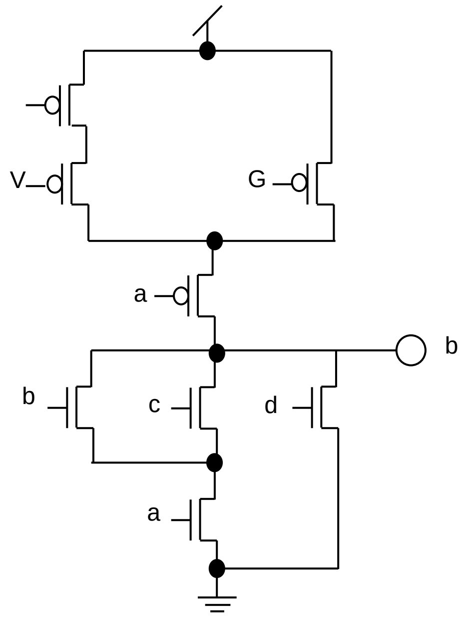


As of the above figure:
J: Implicit non-stop pin
E: Explicit ignore pin
I: Implicit ignore pin
F: Float pin
S: Stop pin
The number of endpoints needs to be balanced by CTS is:
A. *4*
B. *5*
C. *6*
D. *9*
E. *12*

1a261. Which of the four RTL codes will generate latch during synthesis?

A.
```
module newmux (out1, a, b, c, sel);
input a, b, c;
output out1;
input[1:0] sel;
reg out1;
always@(a or b or c or sel)
begin
  if (sel ==2'b10)
    out1 = a;
  else if (sel == 2'b01)
    out1 = b;
  else if (sel == 2'b11)
    out1 = c;
  end
endmodule
```
B.
```
module async2 (out, g, d);
output out;
input g, d;
reg out;
always @(g or d or out)
      begin
   out = g & d | !g & out | d & out;
      end
endmodule
```
C.
```
module latch1(q, data, clk);
output q;
input data, clk;
assign q = clk ? data : q;
endmodule
```
D.
```
module dff(q1, data1, data2, clk);
output q1;
input data1, data2, clk;
reg q1, q2;
always @(posedge clk)
begin
  q1 = data1;
end
always @(posedge clk)
begin
  q2 = data2;
end
endmodule
```
E. None of the above

1a262. What formula describes the circuit?



A. Out = !((!a+!b)&!c+!d)
B. Out = !((a+b)&c+d)
C. Out = !((a&b+c)&d)
D. Out = ((!a+!b)&!c+!d)
E. Out = !((!a&!b+!c)&!d)

1a263. Between which pins of a MOS transistor there is no direct capacitance?

A. Source and gate
B. Drain and gate
C. Gate and substrate
D. Source and substrate
E. Source and drain

1a264. The static power is affected by many factors in CMOS ICs. Some of these factors are:

A. Temperature, threshold voltage, and supply voltage
B. The activity factor at which the circuit is switching, supply voltage, and threshold voltage
C. The capacitive load of the circuit, switching activity, and supply voltage
D. The temperature, the switching activity, and the variability in the threshold voltage
E. None of the above

1a265. What is mainly used in MOS integrated circuits as a circuit resistor?

A. High doped source region
B. High doped drain region
C. Gate dielectric region
D. Transistor channel region
E. Resistive elements are not used

1a266. Design for manufacturability can be defined as:

A. Verifying all physical, electrical, and logical errors, after the chip comes back from fabrication
B. Verifying an IC before fabrication for operation at stress conditions such as low voltage, high temperature, and process variation
C. Verifying the chip before fabrication for the correct functionality under nominal conditions
D. Designing techniques that allow the designer to test an IC after fabrication
E. None of the above

1a267. After synthesis what is the result of the following Verilog description?

```
always @(posedge clk) begin
   if enable
      q <= d;
end //always
```

A. A flip flop
B. A latch
C. A flip flop with a clock gate
D. A Latch with a clock gate
E. None of the above

1a268. Consider the 2 Verilog descriptions below:

```
 always @(posedge clk) begin
   d = b + c;
   a = a + d
end //always
always @(posedge clk) begin
   d <= b + c;
   a <= a + d
end //always
```

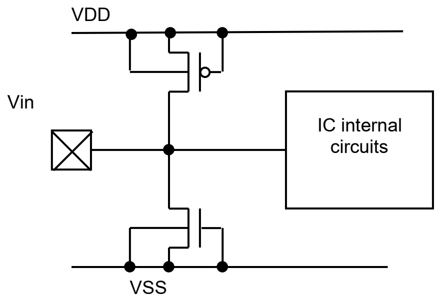
Assuming that a = 3, b = 4, c = 5, and d = 6 at the beginning of the always block, what is the value of a after the 2 statements?

A. 15 and 9
B. 9 and 15
C. 15 and 15
D. 9 and 9
E. None of the above

1a269. What structure (“number-of-rows” x “number-of-columns”) should an n-cell memory matrix have so that the traditional memory test algorithm GALCol would be of linear complexity?

A. $\sqrt{n}$ *x* $\sqrt{n}$
B. logn x (n/ logn)
C. (n/logn) x (logn)
D. C x (n/C), C=const
E. (n/C) x C, C=const

1a270. Assuming that the forward bias p-n junction voltage is V_{pn}, what is the input voltage maximum safe margine?



A. $VSS \leq V_{in} \leq VDD$
B. $VSS\text{-}V_{tn} \leq V_{in} \leq VDD\text{-}V_{tp}$
C. $VSS+V_{tn} \leq V_{in} \leq VDD+V_{tp}$
D. $VSS\text{-}V_{pn} \leq V_{in} \leq VDD+V_{pn}$
E. $VSS+V_{pn} \leq V_{in} \leq VDD+V_{pn}$

1a271. Assuming that inputs of a NOR2 cell are uniformly distributed, what is the output node switching probability?

A. 0.25
B. 0.375
C. 0.5
D. 0.75
E. 0.875

1a272. What is the main resulting degradation of a MOS transistor caused by hot carriers?

A. Increase of Vth
B. Decrease of Vth
C. Increase of channel resistance
D. Decrease of channel resistance
E. Decrease of drain-source breakdown voltage

1a273. What does the threshold voltage of a MOS transistor depend on?

A. Channel length
B. Depths of diffusion in drain and source areas
C. Gate voltage
D. Drain voltage
E. Bulk doping concentration

1a274. Which of the following equations is incorrect?

A. A⊕!B = !A⊕B
B. 1⊕!B⊕A = B⊕A
C. A⊕!B = !A⊕!B
D. A⊕B =! A⊕!B
E. !A⊕B = !(A⊕B)

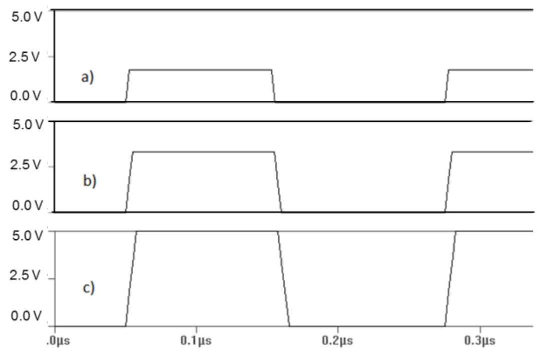
1a275. What problem is solved by DRC?

A. Provision of limitations, set by the designer
B. Compliance of circuit operation with the specification
C. Provision of limitations, set by the foundry
D. Compliance of layout with the circuit
E. Accuracy of selecting design tools

1a276. Which of the forever, repeat, for, function Verilog statements is not synthesizable?

A. forever, for
B. forever, repeat
C. forever, for, function
D. forever, for, repeat
E. None of the above

1a277. Assuming that CMOS inverter is composed of transistors, defined with threshold voltages of Vthn=-Vthp=0,7V. Denote the correct answer regarding power consumption in case it is excited with signals depicted as a), b) and c).



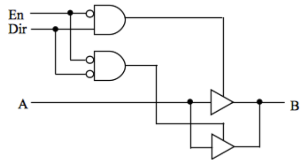
Mark the proper order of energy consumption:

A. Ea > Eb > Ec
B. Ea > Eb < Ec
C. Ea < Eb > Ec
D. Ea < Eb < Ec
E. The correct answer is missing

1a278. 16 bit signed Integer numbers are represented in the memory in two's complement code. What is the value of the minimum number represented in this format?

A. -32 767
B. -32 768
C. 0
D. -65 535
E. None of the above

1a279. What function is performed by the given circuit?



A scheme of bus transceiver is shown

A. One-bit bus transceiver
B. Tri-state buffer
C. Multiplexer/demultiplexer
D. Two-bit bus transceiver
E. None of the above

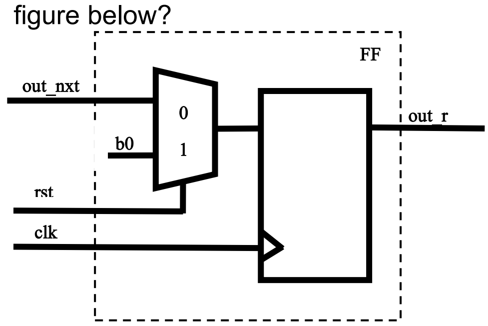
1a280. Specify the minimum radix in which the following statement $\sqrt{100}=10$ is true.

A. Radix 8
B. Radix 7
C. Radix 10
D. Radix 16
E. None of the above

1a281. Which of the following statements is not a valid specification of a constant in HDL Verilog?

A. 8'd25;
B. 8'b0110_1110;
C. 6'o39;
D. -16'h442f;
E. None of the above

1a282. Which of the Verilog-descriptions matches the flop schematics presented in the figure below?



A.
```
always @ (posedge clk)
    if(rst)
        out_r <= 1'b0;
    else
        out_r <= out_nxt;
```

B.
```
always @ (posedge clk or posedge rst)
    if(rst)
        out_r <= 1'b0;
    else
    out_r <= out_nxt;
```

C.
```
always @ (negedge clk)
  if(!rst)
```

out_r <= 1'b0;

else

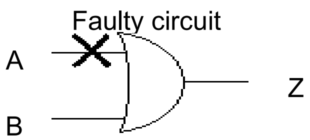
out_r <= out_nxt;

D. none of the above
E. B. and C.

1a283. How many bits are needed to convert an 8b thermometer code into BCD?

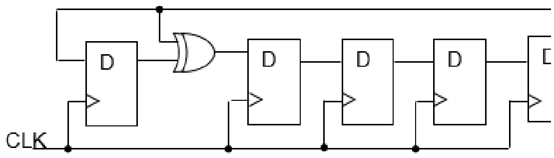
A. 2
B. 4
C. 6
D. 8
E. 16

1a284. Find the set of all input patterns for detection of the stuck-at-0 fault on the input line A of the logical gate Z = A V B depicted below:



A. {(0, 0)}
B. {(1, 0)}
C. {(1,0), (0, 1)}
D. {(0, 0), (0, 1), (1,0)}
E. The correct answer is missing

1a285. Given Galois LFSR circuit with feedback polynomial   d (x) = 1 + x + x5. Determine the state of LFSR after supplying to the CLK input 10th pulse. The initial state of LFSR 00110.

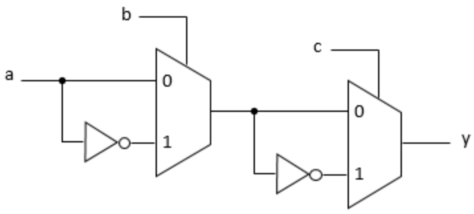


A. 10011
B. 11111
C. 00111
D. 11011
E. The correct answer is missing

1a286. Determine the minimal number of inputs and outputs of the synchronous FSM. Input alphabet of FSM contains 10 symbols, the number of states is 25, the number of symbols of the output alphabet is 6. CLK and Reset inputs are not taken into account.

A. 12
B. 13
C. 15
D. 16
E. The correct answer is missing

1a287. Which of the following functions is implemented by the given circuit?



A. a·b + c
B. a·b ⊕ a·c
C. a ⊕ b ⊕ c
D. a ⊕ b·c
E. The correct answer is missing

1a288. The instruction set of processor contains 300 instructions. The number of general purpose registers is equal 32. The amount of main memory is 4MB. Used absolute memory addressing mode. How many bits will "register- memory" instruction contain?

A. 24
B. 32
C. 36
D. 54
E. The correct answer is missing

b) Problems

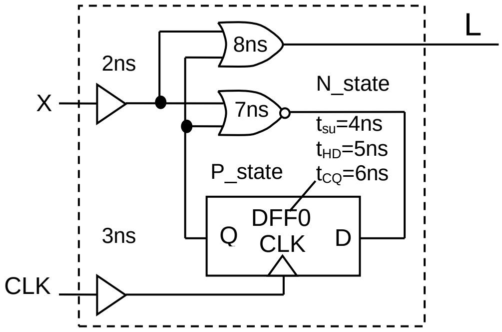
1b1.

For the presented circuit:

a. What are the external setup and hold times for input X?

b. What is the delay from the clock to output L?

c. What is the clock cycle time based on register–to–register delays (the flip-flop is drawn ''backwards'')?



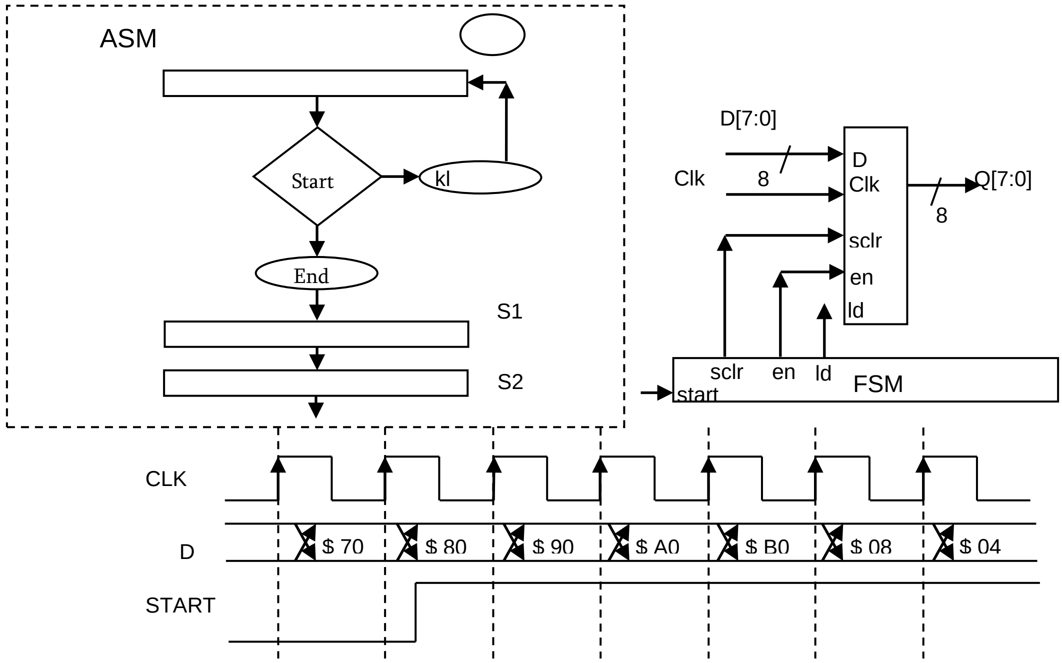
1b2.

Consider the following VHDL code.

```
library ieee;
use ieee.std_logic_1164.all;
entity pulsedet is port(
signal clk,reset,pulse_in: in std_logic;
signal pulse_out: out std_logic
);
end pulsedet;
architecture behavior of pulsedet is
signal dffout : std_logic_vector(2 downto 0);
begin
dffs: process(clk,reset)
begin
if (reset = '1') then
dffout <= "000";
elsif (clk'event and clk='1') then
dffout(2) <= dffout(1);
dffout(1) <= dffout(0);
dffout(0) <= pulse_in;
end if;
end process;
pulse_out <= dffout(2) and not dffout(1);
end behavior;
```

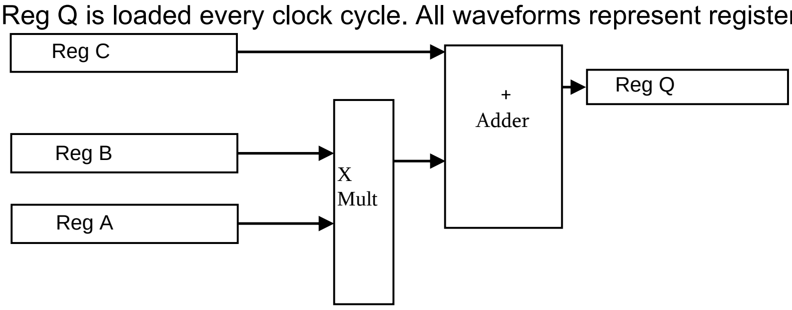
Draw a diagram of logic that implements the VHDL code. (Show logic gates and D flip-flops.)

1b3.
On the waveforms below, complete the waveforms for state, ld, en, and Q. The FSM is controlling the UP counter. Assume the initial state is S0.

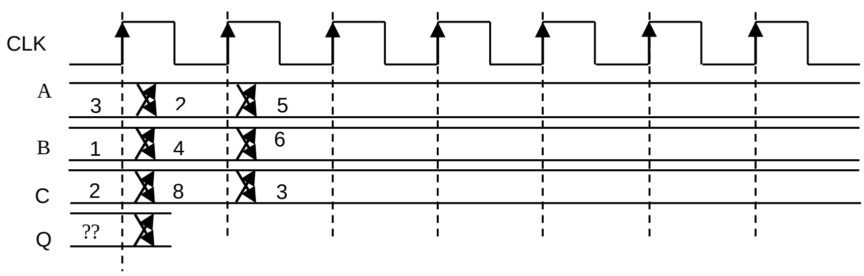


1b4.
For the figure below:

a. Give the maximum register-to-register delay.
b. Modify the diagram to add one level of pipelining but still maintain the same functionality. Add the pipeline stage in the place that will improve the register-to-register delay the most. Compute the new maximum register-to-register. Assume that adding a pipeline registers to any functional unit (adder or multiplier) breaks the combinational delay path in the unit exactly in half.
c. With the pipeline stage added, complete the 'Q' waveform shown below. Input registers change values as shown; assume Reg Q is loaded every clock cycle. All waveforms represent register outputs.



Mult delay= 18 ns, Adder delay=7 նվ, Tcq = 3 ns, Setup time= 18 ns, Hold time =2 ns



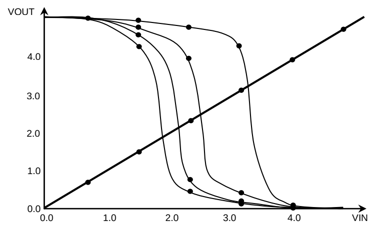
1b5.
Design a circuit for a CMOS cell which is realized by Z=!(A(B+C)+BD) logic function.

1b6.
Design a MS D-FF based on transmission gates (TG) with SET input.

1b7.
Design a MS D-FF based on switching keys with SET and RESET inputs.

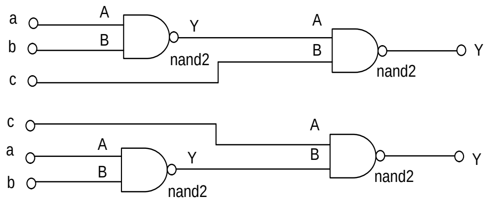
1b8.
Design a CMOS cell circuit which is described by $Y=\sum(1,2,6,7)$ function.

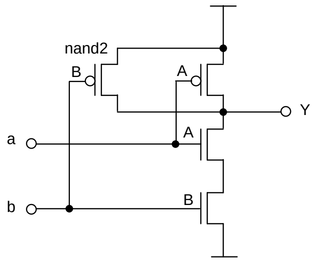
1b9.
Four inverters (VDD=5V) have WN, changing from 3um to 12um while WP is the same for each inverter (10 um). Identify which WP/WN ratio produces the most left curve in the figure.
In this process VDD is 5V. Which inverter has the most even noise margins (V_{THN}=0.6 V, V_{THP}=-0.8 V, LN=LP)?



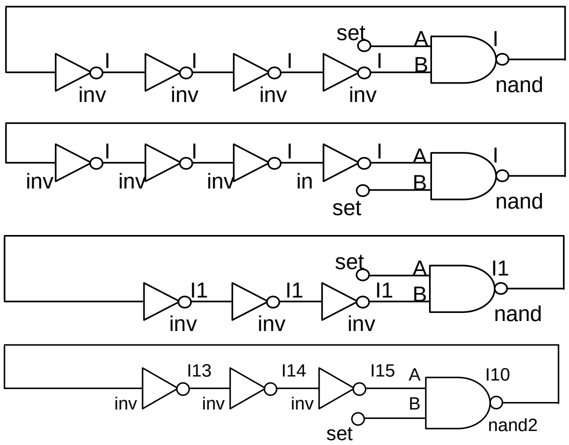
DC response of three different inverters

1b10.
Both circuits below have the same function. Which one has the smallest, best case delay? Explain the answer for full credit.

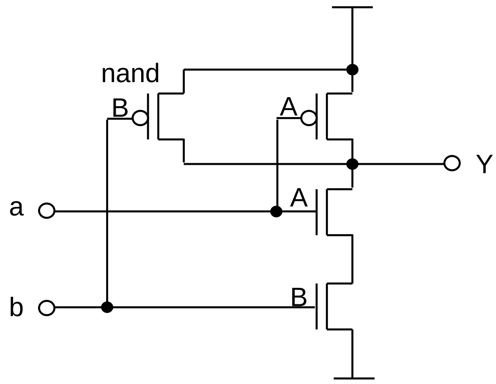




1b11.
It is necessary to design a ring oscillator that is to oscillate as fast as possible. Usually a set pin is needed to start the ring oscillator properly. Which circuit would be used for the fastest ring oscillator?
Explain why for full credit.

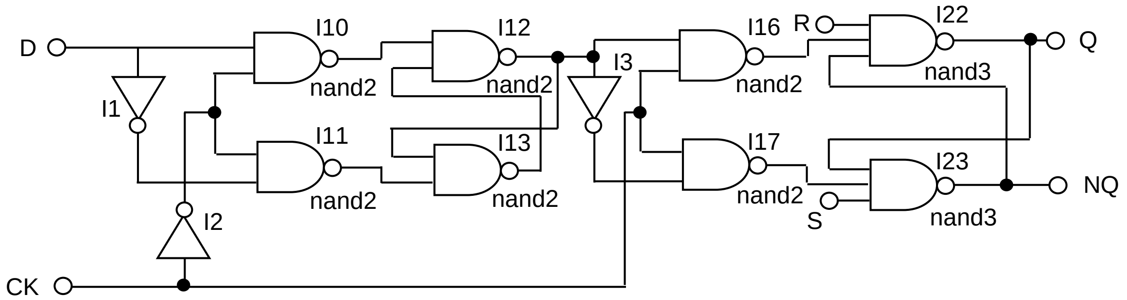


Circuits of a ring oscillator (cont.)



NAND2

1b12.
Figure shows a DFF. Using the timing data presented in the table, calculate how long CK has to remain high for Q and NQ to get the value from the output of I12 (nand2). Figure shows a DFF. Using the timing data presented in the table, calculate how long D has to remain stable before the rising clock edge so that the outputs of I12 and I13 properly get the value of D (or not(D)).



DFF

Table: Various times for various gates

	INV	NAND2	NAND3
TFALL (ps)	200	500	600
TRISE (ps)	300	500	650
τphl (ps)	100	250	300
τplh (ps)	150	250	325

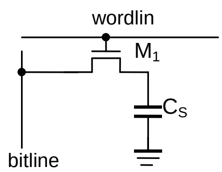
1b13.
Using the AOI technique design a CMOS circuit to implement the following logic function: Z=(ABCD+EFG)H Show the PNET and the NNET connected into a circuit.

1b14.
Using the AOI technique, design a CMOS circuit to implement the following logic function: Z=(AB+CD+EF)G Show the PNET and the NNET connected into a circuit.

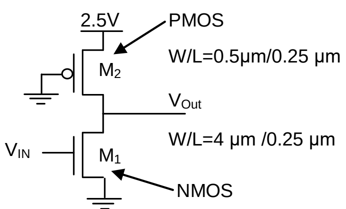
1b15.
Using the AOI technique, design a CMOS circuit to implement the following logic function: Z=(ABC+DE+F)G Show the PNET and the NNET connected into a circuit.

1b16.
Using the AOI technique, design a CMOS circuit to implement the following logic function: Minimize area and delay. (Show Euler path, but do not draw it). Z=(AB+CD+EFG)H. Show the PNET and the NNET connected into a circuit.

1b17.
For reading, the bitline is precharged to VDD/2. Determine the settled voltage on the bitline when reading logic 1 and logic 0, if Vtn=0.3V, VDD=1.2V, C_{BL}=10C_s. The voltage swing of the wordline control is from 0 to VDD. Ignore leakages and body bias effect.



1b18.
Compute the following for the pseudo-NMOS inverter shown below:
k_n = 115uA/V^2, k_p = 30uA/V^2, V_{tN} = 0.5V, V_{tP} = -0.4V
a) V_{OL} and V_{OH}
b) The static power dissipation: (1) for V_{in} low, and (2) for V_{in} high
c) For an output load of 1 pF, calculate t_{pLH}, t_{pHL} (ignore the intrinsic capacitances of transistors)

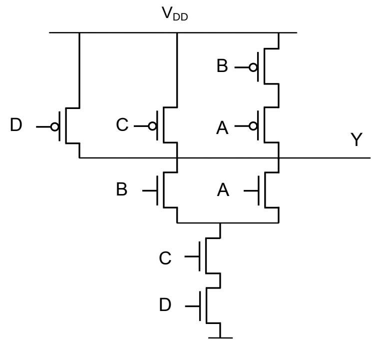


1b19.

Consider the circuit below.

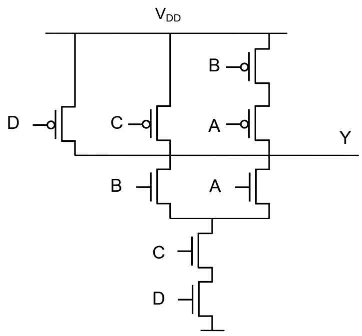
a) What is the logic function implemented by CMOS transistor network? Size the NMOS and PMOS devices such that the output resistance is the same as of an inverter with an NMOS *W/L* = 4 and PMOS *W/L* = 8.

b) What are the input patterns that give the worst case *tpHL* and *tpLH*? State the initial input patterns and tell which input(s) has to make a transition to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.



1b20.

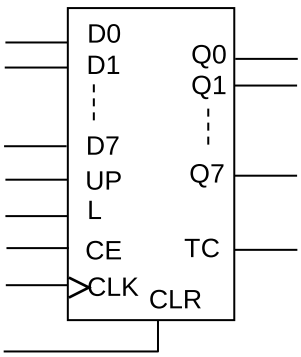
If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=0.8, determine the switching power dissipation in the logic gate. Assume *VDD*=2.5V, *Cout*=30fF and *fclk*=250MHz.



1b21.

Design an 8-bit binary up/down counter with parallel synchronous loading, asynchronous reset and an input to enable counting.

Logic symbol for the given counter:



CLK – clock input
CE – count enable input
CLR – active high asynchronous reset input
L – active high synchronous load input
D0 … D7 – parallel data inputs
UP – input of count direction change
Q0 … Q7 – data outputs
TC – carry output (output of count completion)

TC is set as soon as code FF_{16} or 00_{16} appears on counter outputs.

Truth table of the counter

CLR	L	CE	UP	CLK	Q7 … Q0	TC	Mode
1	X	X	X	X	0 … 0	0	Asynchronous reset
0	1	X	X		D7 … D0	0	Parallel loading (D[7:0]≠FF)
0	1	X	X		D7 … D0	1	Parallel loading (D[7:0] =FF)
0	1	X	X		D7 … D0	1	Parallel loading (D[7:0] ≠00))
0	1	X	X		D7 … D0	1	Parallel loading (D[7:0] =00)
0	0	1	1		+1	0	Increment (Q[7:0] ≠FF)

0	0	1	1		+1	1	Increment (Q[7:0] =FF)
0	0	1	0		-1	0	Decrement (Q[7:0]) ≠ 00)
0	0	1	0		-1	1	Decrement (Q[7:0]) = 00)
0	0	1	0	X	$Q7_n$ … $Q0_n$	TCn	Hold

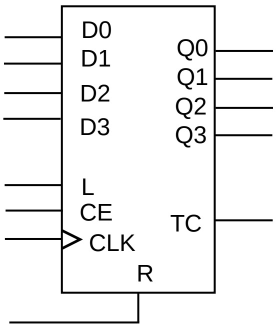
$Q7_n$ … $Q0_n$ – previous states of the counter.

a) Describe counter in Verilog and simulate by means of logic analysis tool VCS.
b) Synthesize by Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually, using T flip-flops. For simplification take the number of bits equal to 4.

1b22.

Design a 4-bit binary-coded decimal counter with parallel synchronous loading, synchronous reset and count enable inputs.

Logic symbol for the given counter:



CLK – clock input
CE – count enable input
R – active high synchronous reset input
L – active high synchronous load input
D0 … D3– parallel data inputs
Q0 … Q3 – data outputs
TC – carry output (output of count completion)

TC is set as soon as code 1001_2 appears on counter outputs.

Truth table of the counter

R	L	CE	CLK	Q3 … Q0	TC	Mode
1	X	X	↑	0 … 0	0	Synchronous reset
0	1	X	↑	D3 … D0	0	Parallel loading (D[3:0]≠1001)
0	1	X	↑	D3 … D0	1	Parallel loading (D[3:0] =1001)
0	0	1	↑	+1	0	Increment (Q[3:0]#FF)
0	0	1	↑	+1	1	Increment (Q[3:0]=FF)
0	0	0	X	$Q3_n$ … $Q0_n$	TCn	Hold

$Q3_n$…$Q0_n$ – previous states of the counter.

a) Describe the counter in Verilog and simulate by means of logic analysis tool VCS.
b) Synthesize by Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually, using T flip-flops.

1b23.

Design a clocked synchronous Moore FSM producing a remainder of division of a decimal number by 3 on its outputs. FSM receives the digits of a decimal number sequentially on its inputs.

a) Describe counter in Verilog and Simulate using logic analysis tool VCS.
b) Synthesize using Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually.

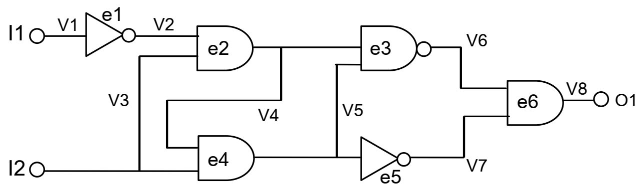
1b24.

Design a clocked synchronous FSM with two inputs, X and Y, and one output, Z. The output should be 1 if the number of 1 inputs is the multiple of 5 on X and Y since reset, and 0 otherwise.

a) Describe counter in Verilog and Simulate using logic analysis tool VCS.
b) Synthesize using Design Compiler tool. Obtain Verilog-out (Gate Level Netlist). Again simulate and compare the results.
c) Synthesize the circuit of the given counter manually.

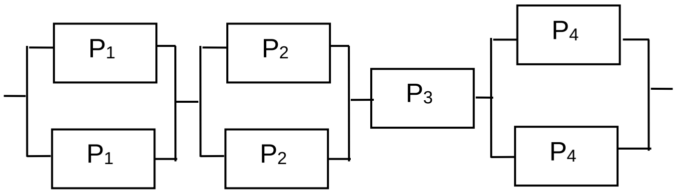
1b25.

Calculate the minimum and maximum signal formation time of the shown circuit in V_1 – V_8 nets by conventional units, if the cell delays are given by conventional units $\tau_{e1}=\tau_{e5}=10$, $\tau_{e3}=15$, $\tau_{e2}=\tau_{e4}=\tau_{e6}=20$: On the circuit mark I/O critical path and calculate the total delay of that path by conventional units.



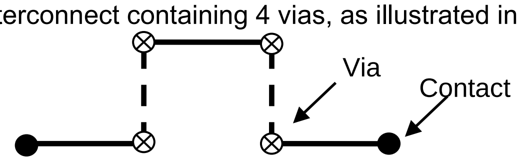
1b26.
An interconnect of 300 um length and 0,2 um width is given, the sheet resistance and capacitance of which correspondingly equal:
$R_{\square}$ =0,2 Ohm/$\square$ C =0,1 fF/um.
Construct the equivalent circuit of interconnect's 3-segment, R,C distributed parameters and calculate the delay in it.

1b27.
Calculate faultiness probability of IC consisting of 7 blocks if their connection, according to reliability, has the following view.



Given P_1=0.5; P_2=0.6; P_3=0.8; P_4=0.4.

1b28.
Two contacts are connected by an interconnect containing 4 vias, as illustrated in the figure.



Construct interconnect's R, C equivalent circuit and calculate the delay in the transmission line connecting two contacts, if given:
– Each transmission line's capacitance of interconnect equals 100 fF.
– Each programmable contact resistance equals 1 Ohm.
Ignore ohmic resistances of transmission lines and contacts as well as the capacitances of vias.

1b29.
Based on the logic of provided VHDL code, develop a digital circuit consisting of logic gates.

```
library ieee;
  use ieee.std_logic_1164.all;
  use ieee.std_logic_unsigned.all;
  entity adder2 is port(
     signal
        operand1,
        operand2: in std_logic_vector(1 downto 0);
     signal
        sum: out std_logic_vector(2 downto 0);
     );
  end adder2;
  architecture behavior of adder2 is
  begin
     sum <= operand1 + operand2;
  end behavior;
```

Determine whether the provided logic is a combinational logic or not. Argue the answer.

1b30.
Based on the logic of provided VHDL code, develop a digital circuit consisting of logic gates.

```
library ieee;
    use ieee.std_logic_1164.all;
    use ieee.std_logic_unsigned.all;
    entity incr1 is port(
       signal
          operand: in std_logic_vector(2 downto 0);
```

```
        signal
           incr_result: out std_logic_vector(3 downto 0);
        );
     end incr1;
     architecture behavior of incr1 is
     begin
        incr_result <= operand + 1;
     end behavior;
```

Determine whether the provided logic is a combinational logic or not. Argue the answer.

1b31.

Based on the logic of provided VHDL code, develop a digital circuit consisting of logic gates.

```
library ieee;
   use ieee.std_logic_1164.all;
   library types;
   use types.conversions.all;
   entity shift_ll is port(
      signal
         operand: in std_logic_vector(3 downto 0);
         shift_size: in std_logic_vector(1 downto 0);
      signal
         shift_result: out std_logic_vector(3 downto 0);
      );
   end shift_ll;
   architecture behavior of shift_ll is
   begin
      process (operand, shift_size)
      begin
         --left logical shift by shift_size
         shift_result <= operand sll to_uint(shift_size);
      end process;
   end behavior;
```

Determine whether the provided logic is a combinational logic or not. Argue the answer.

1b32.

Based on the logic of provided VHDL code, develop a digital circuit consisting of logic gates.

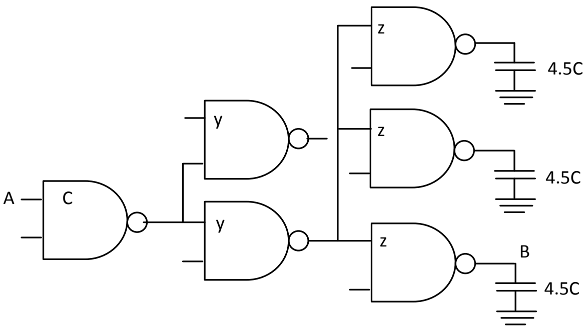
```
library ieee;
   use ieee.std_logic_1164.all;
   library types;
   use types.conversions.all;
   entity shift_rl is port(
      signal
         operand: in std_logic_vector(3 downto 0);
         shift_size: in std_logic_vector(1 downto 0);
      signal
         shift_result: out std_logic_vector(3 downto 0);
      );
   end shift_rl;
   architecture behavior of shift_rl is
   begin
      process (operand, shift_size)
      begin
         --right logical shift by shift_size
         shift_result <= operand srl to_uint(shift_size);
      end process;
   end behavior;
```

Determine whether the provided logic is a combinational logic or not. Argue the answer.

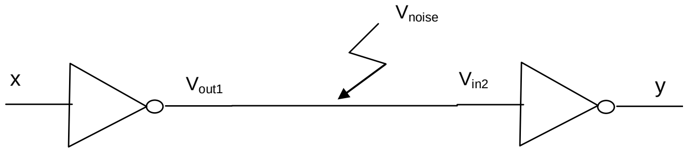
1b33.

The sizes of the first cell in the shown logic circuit are selected such that it has a driving strength of a minimal size inverter having input capacitance C, i.e. NMOS transistor sizes have been increased to compensate the consequence of serial connection.

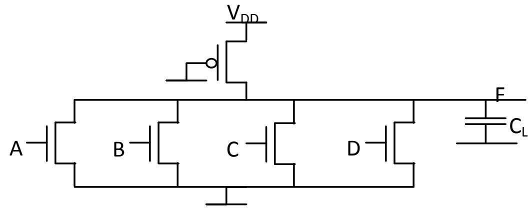
Define the second and third stage scaling ratios y and z, from the condition to get minimum delay in the A-to-B path. Ignore intrinsic output and interconnects capacitances of cells.



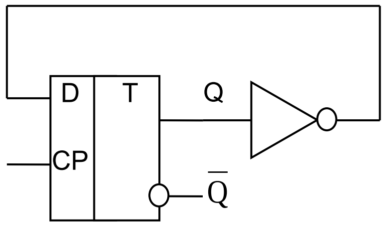
1b34.
For the following circuit define the maximum permissible noise magnitude V_{noise}, if the inverter's VTC parameters are V_{OHnom}=1V, V_{OHmin}=0.9V, V_{OLnom}=0V, V_{OLmax}=0.15V, V_{SP}=048V, V_{IHmin}=0.58V, V_{ILmax}=0.44V.



1b35.
Define four input NOR cell's output low and high levels (see the figure) (a) when only one input switches (b) when all the inputs switch simultaneously if C_L=0.05 pF. Use the following technological parameters VDD=1.8 V, $T_{ox}=10^{-8}$ m, μ_n=270 cm^2/Vv, V_{tn}=0.5V, μ_p=70 cm^2/Vv, V_{tp}=-0.5V, L_n=0.18 um, W_n=20 um, Wp=5 um.

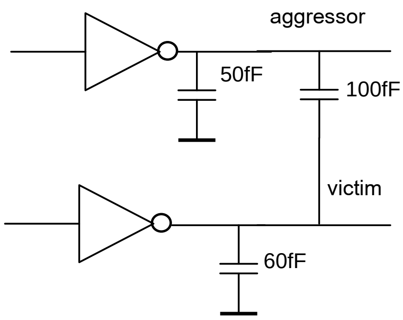


1b36.
A circuit of a frequency divider is presented.

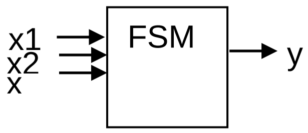


Define the minimum period of clock pulses if t_{su}=20ps, t_{hd}=-15ps, t_{c2q}=100ps, t_{pinv}=30ps.

1b37.
For the given circuit define:
a) the maximum value of the noise in victim line that occurs when the signal in the aggressor line switches from 1.0 V to 0V.
b) the effective capacitance in victim line for delay calculation if the signals in aggressor and victim lines switch in opposite directions.

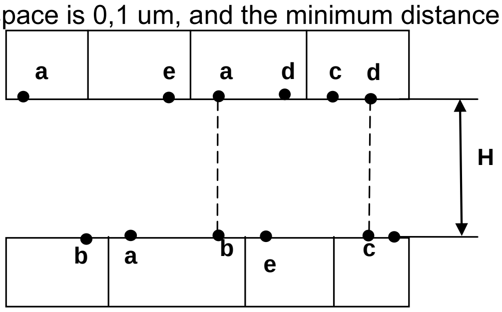


1b38.
Design Moore FSM which has 3 inputs x1, x2, x3 and 1 output. The output of FSM equals 1 when total number of ones, which are given to FSM inputs, is divided by 7. Describe by Verilog. Create a testbench and simulate by VCS.

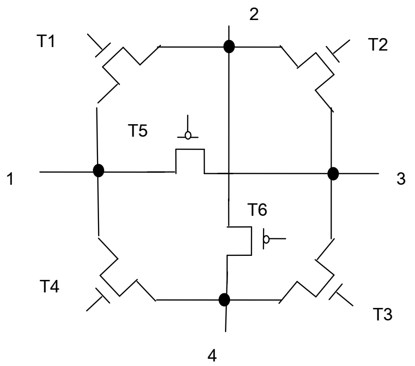


1b39.
Describe by Verilog 5-bit polynomial counter (LFSR). In feedback circuit $d(x) = 1+ x^3 +x^5$ is polynomial. The counter has 10000 initial state asynchronous preset input. The shift of information is realized by positive edge of clock signal.
Describe by Verilog. Create a testbench and simulate using VCS.

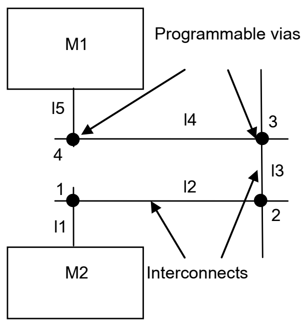
1b40.
Define the minimum H distance between two rows of cells which is necessary for routing of two-layer co-perpendicular routing of a, b, c, d, e nets if the minimum permissible size between interconnects width and space is 0,1 um, and the minimum distance between interconnects and 0,2 um.



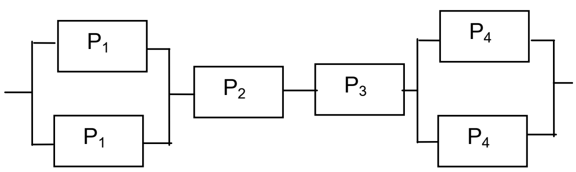
1b41.
Switching block with 4 pins (1, 2, 3, 4) is shown in the figure. It consists of 4 NMOS and 2 PMOS transistors. What kind of logic level signals (0 or 1) should be given to each gate of T1-T6 transistors to provide:
a) Simultaneous signal transfer from pin 1 to 3 and from pin 2 to 4;
b) Simultaneous signal transfer from pin 1 to 4 and from pin 2 to 3;



1b42.
Two modules (M1 and M2) are connected with 5 interconnects (I1-I5) and 4 programmable vias (1-4). Construct interconnect's R, C equivalent circuit and calculate the delay in the transmission line connecting two modules, if given:
Each transmission line capacitance of interconnect equals 100 fF.
Each programmable contact resistance equals 1 Ohm.
Ignore ohmic resistances of interconnects and contacts as well as the capacitances of programmable vias.

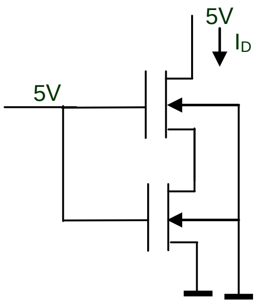


1b43.
Calculate faultness probability of IC consisting of 7 blocks if their connection, according to reliability, has the following view.
Given P_1=0,5; P_2=0,6; P_3=0,8; P_4=0,4.



1b44.

Using the following parameters, define the current through series connected transistors. Kp'=25 mkA/V^2, V_{T0}=1.0V, γ=0.39V$^{1/2}$, 2|Φ_F|=0.6V, W/L=1. Consider the body bias effect. Several iterations will be needed for the solution.



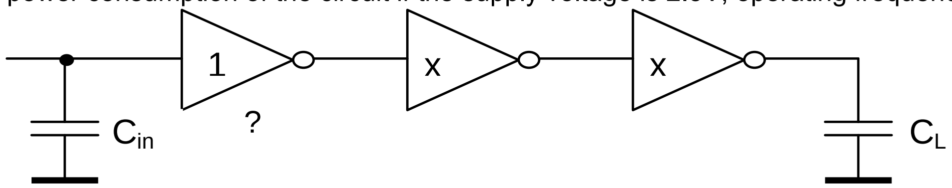
1b45.

The first inverter of the presented buffer is of minimal size, input capacitance is C_{in}=10 fF, delay 70 ps. The load capacitance of the buffer is C_L=20 pf.

a) Define the sizes of the other two inverters with respect to the minimal one. Use the condition to get minimum delay, consider that input capacitances are proportional to sizes.

b) Add any number of inverters to get minimum delay. Define the total delay.

c) Define the power consumption of the circuit if the supply voltage is 2.5V, operating frequency 200 MHz.



1b46.

Design a CMOS cell, implementing *F = AB + AC + BC function.*

Choose a transistor sizes such that NMOS and PMOS net resistances are equal to the minimal size inverter's resistances. Consider *2k'p = k'n. For what input combinations will the best and the worst resistances be obtained?*

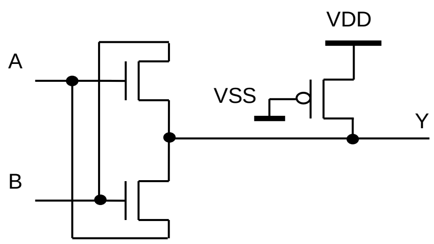
1b47.

A cell with transistor switches is presented in the figure.

a) What function does the cell implement? Show the truth table.

b) Considering inputs 0 and 2.5V, choose PMOS transistor's sizes such that V_{OL} = 0.3V. Consider 2k'$_p$ = k'$_n$ and |V_{tp}|= V_{tn}=0.5V, for NMOS transistors W/L=1.5um/0.25um.

c) Will the cell continue to operate correctly if a PMOS transistor is removed? Does the PMOS transistor implement any helpful function?



1b48.

In the presented figure C_x = 50 fF, M1 transistor's W/L = 0.375um/0.375um, M2 transistor's W/L= 0.375um/0.25um. Note that the inverter does not switch until the input V_x voltage reaches VDD/2.

V_{DD} = 2.5V

$(W/L)_3$ = 1.5um/0.25um

$(W/L)_4$ = 0.5um/0.25um

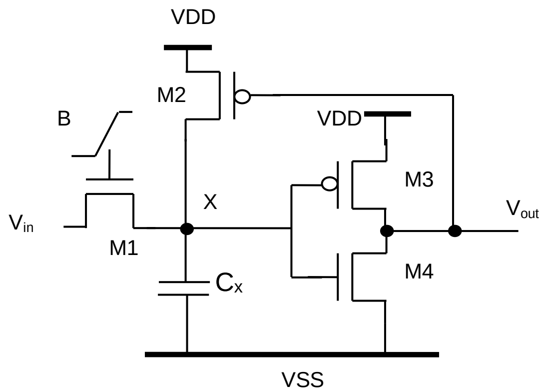
k_n' = 115mkA/V^2, k_p' = -30mkA/V^2

V_{tN} = 0.43V, V_{tP} = -0.4V

a) How long will it take for M1 transistor to move x node from 2.5V to 1.25V if V_{in} = 0V, V_B= 2.5V?

b) How long will it take for M2 transistor to move x node from 0V to 1.25V if V_{in} = 2.5V, V_B= 2.5V?

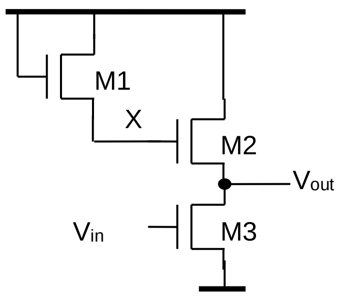
c) What is the minimum value of V_B voltage for Vx=1.25V when V_{in} = 0V?



1b49.

For the figure shown below in a MOS inverter, consider that all transistor bulks are connected to the ground and the IN input changes from 0V to 2.5V.

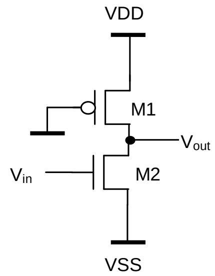
a) Get the expression to compute *x* node's voltage considering γ=0.5, $2|\Phi_f|$=0.6V, V_{t0}=0.5V, V_{DD}=2.5V.
b) Considering γ=0, define the operating modes of M2.
c) Considering γ=0, define the output value when V_{in} =0V.
d) Considering γ=0, get the expression of inverter's switching point voltage (V_{SP}) (in the switching point V_{IN}= V_{OUT}). Consider M1, M2 and M3 transistor sizes $(W/L)_1$, $(W/L)_2$ and $(W/L)_3$ respectively. Define changing limits of V_{SP} when (1) $(W/L)_1 >> (W/L)_2$, (2) $(W/L)_2 >> (W/L)_1$.



1b50.

For the given inverter $(W/L)_1$=5um/0.25um, $(W/L)_2$=4um/0.25um, k_n = 120uA/V^2, k_p = 30uA/V^2, V_{tN} = 0.5V, V_{tP} = -0.4V, V_{DD}=2.5V.

a) V_{OL} and V_{OH}
b) V_{SP}



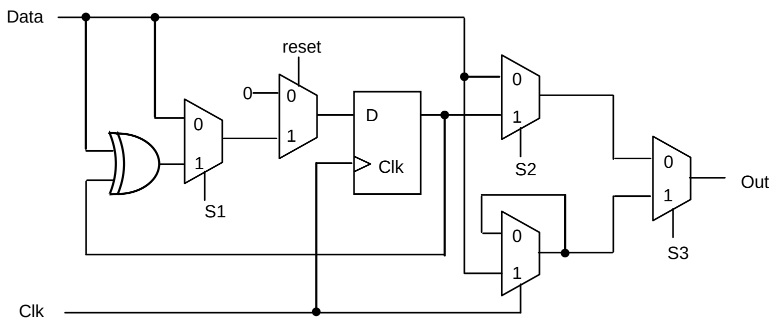
1b51.

Design a cascade differential voltage switching logic cell which is described by the equation $F = ABC\overline{D} + A\overline{B}CD$. Use minimum number of transistors. Consider that normal and inverted values of inputs are available.

1b52.

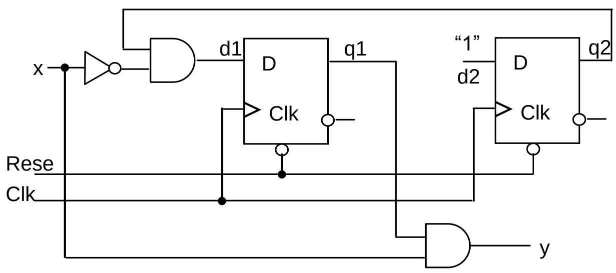
A circuit of a flip-flop with combined logic is shown. Define for which values of S1, S2, S3 signals this circuit will operate as:

- Positive edge-triggered D-flip-flop with synchronous reset
- Positive edge-triggered T- flip-flop with synchronous reset
- D-latch
- Transfer of input data to output



1b53.

Define what input binary sequence detector the given circuit is. The beginning of the following sequence can be the end of the previous one.



1b54.
Using three- and four-bit Johnson counters (one of them having odd number of states), construct a counter with 42 states. Construct a decoder that will decode every 6^{th} state starting from 0.

1b55.
It is required to design an arbiter circuit that performs the following function:
allows availability to four devices into the general resource of the given system. At any time only one device can use the resource. Each device creates a request which is given to the arbiter input by clock: The FSM for each device generates an access to permission signal – grant. The requests are processed as per priority. After processing the request from some device, the device removes the request and the FSM comes to its initial state. The system also has an additional input that defines the priorities of requests. If direction=0, the highest priority is r0 request, then r1, r2 and r3. And if direction=1, the priorities have opposite order r3,r2,r1,r0.

1. Devise transition graph of arbiter states
2. Describe the FSM in Verilog.

1b56.
Suppose there is a given "data_in" signal with one hot logic vector of 8-bit of width. And the goal is to calculate the encoded decimal value of the bit index having value of 1'b1 (the following 'case' statements show the required logic).

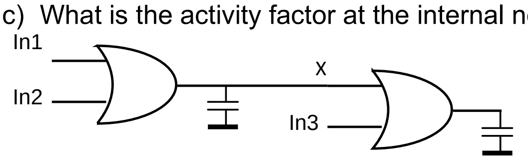
```
input  [7:0] data_in;
output [3:0] data_out;
        casez(data_in) //data_in can have only one 1 at a time
           8'b???????1: data_out = 3'd0;
           8'b??????10: data_out = 3'd1;
           8'b?????100: data_out = 3'd2;
           8'b????1000: data_out = 3'd3;
           8'b???10000: data_out = 3'd4;
           8'b??100000: data_out = 3'd5;
           8'b?1000000: data_out = 3'd6;
           8'b10000000: data_out = 3'd7;
           default:     data_out = 3'd0;
        endcase
```

Note, 'one hot logic vector' means that this vector will have only one.
1'b1 value in its bits. E.g.:

0001
0010
0100
1000

Provide an optimal gate-level logic equivalent to this case statement (using only logical AND, OR and NOT gates). The answer may be provided in either VerilogHDL or schematic drawing interpretation.
a) Provide the gate level derivation logic for data_out[0].
b) Provide the gate level derivation logic for data_out[1].
c) Provide the gate level derivation logic for data_out[2].

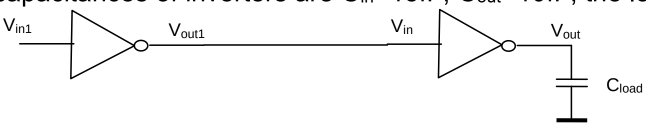
1b57.
Consider the implementation of a 3-input OR gate shown in the figure below. Assume there are 3 inputs A, B, and C where P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.1. For a static CMOS implementation of this circuit:
a) What is the best order to place these inputs to minimize power consumption?
b) What is the worst order?
c) What is the activity factor at the internal node (X) in these cases?



1b58.
Derive the truth table, state transition graph, and output transition probabilities for a three-input XOR gate with independent,
a) Identically distributed, uniform white-noise inputs.
b) P(A=1)=0.2, P(B=1)=0.4, P(C=1)=0.6.

1b59.
Implement the equation X=((!A+!B)(!C+!D+!E)+!F)!G using complementary CMOS. Size the devices such that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6.

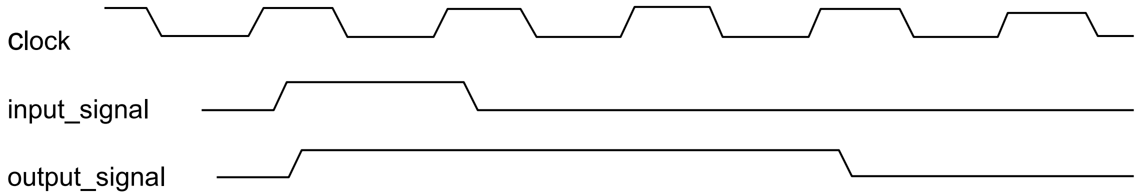
1b60.
Determine the power dissipation in the circuit, if V_{DD}=1V, the input frequency is 800 MHz, input and output capacitances of inverters are C_{in}=15fF, C_{out}=10fF, the load capacitance is C_{load}= 100fF.



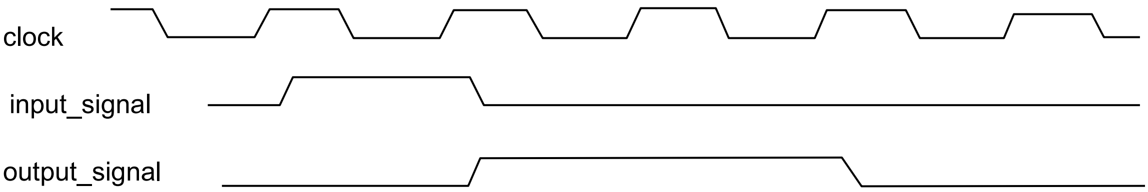
1b61.
Determine the switching point voltage of a CMOS NAND2 cell: $(W/L)_n$=14, $(W/L)_p$=12 and inputs switch simultaneously, V_{DD}=3.3 V, T_{ox}=1.5*10^{-8} m, μ_n=550 cm^2/Vs, V_{tn}=0.7 V, μ_p=180 cm^2/Vs, V_{tp}=-0.8 V.

1b62.
Calculate the 50% level rise delay at the end of a 500um x 0.5um wire. The sheet resistance is 0.08 Ohm/sq, overlap capacitance is 30 aF/um^2, fridge capacitance is 40 aF/u, the internal resistance of the signal source is 100 Ohm, the load capacitance at the end of wire can be neglected.
a) Use lamped parameters.
b) Use distributed parameters.
c) Use ladder model dividing the wire into 10um pieces.

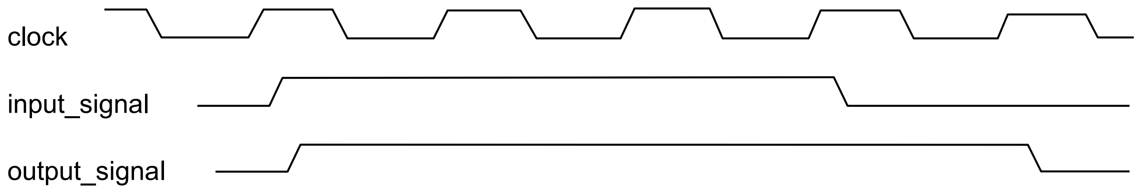
1b63.
Implement required logic satisfying the functionality shown by waveform drawing. Use logic OR, AND and NOT gates and/or D-flip-flops as needed. The implementation may be done in either principle schematic, or Verilog HDL, or VHDL formats (syntax accuracy is not required).



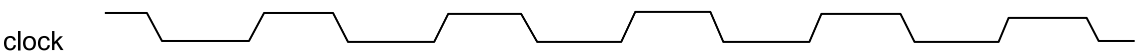
1b64.
Implement required logic satisfying the functionality shown by waveform drawing. Use logic OR, AND and NOT gates and/or D-flip-flops as needed. The implementation may be done in either principle schematic, or Verilog HDL, or VHDL formats (syntax accuracy is not required).

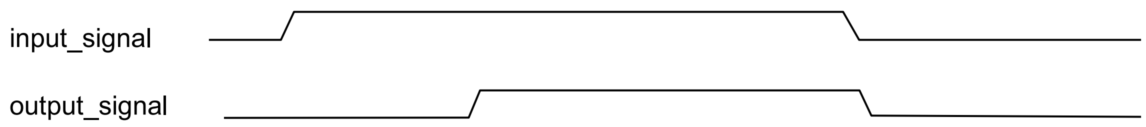


1b65.
Implement required logic satisfying the functionality shown by waveform drawing. Use logic OR, AND and NOT gates and/or D-flip-flops as needed. The implementation may be done in either principle schematic, or Verilog HDL, or VHDL formats (syntax accuracy is not required).



1b66.
Implement required logic satisfying the functionality shown by waveform drawing. Use logic OR, AND and NOT gates and/or D-flip-flops as needed. The implementation may be done in either principle schematic, or Verilog HDL, or VHDL formats (syntax accuracy is not required).





1b67.
Design modulo-3 binary counter. Sequence of states 0,1,2,0,1,2,… . Use JK-flip-flop.

1b68.
Mealy FSM is given with the following table. It has 3 states, input alphabet is X={0,1}, output alphabet is Y={0,1}, internal variables: q1, q2.

Current state	Next state, Y	
	X=0	X=1
q1 q2	q1 q2, Y	q1 q2, Y
0 0	0 1, 0	1 0, 1
0 1	1 0, 1	0 0, 1
1 0	0 0, 1	0 1, 1

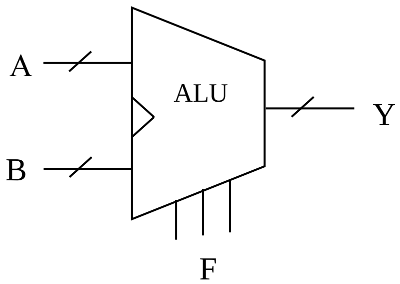
Describe the FSM on Verilog.

1b69.
Compose Verilog description of synthesized model of N-bit binary reverse counter with Up and Down inputs. If Up=1 the content of counter increases by 1, the Down=1 content of counter decreases by 1. If the state of Up=Down=0 counter does not change, Up=Down=1 input is prohibited. The counter changes its state at negative edge of the clock. The reset is synchronous. N=8.

1b70.
By Verilog describe 7-bit polynomial counter (LFSR). In feedback circuit $d(x) = 1+ x^6+x^7$ is polynomial. The data are loaded asynchronously from data input by high level of load signal.

1b71.
By Verilog describe the ALU that performs the operations, mentioned in the table. All logic operations are bitwise.

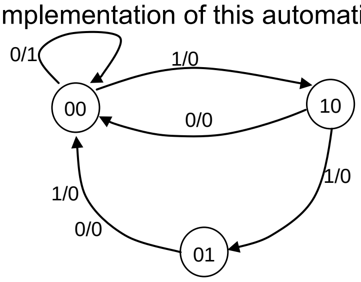
Function code (F)	Function
0 0 0	A & B
0 0 1	A | B
0 1 0	A+ B
0 1 1	Not used
1 0 0	A ⊕ B
1 0 1	A – B
1 1 0	A OR ~B
1 1 1	~ A



1b72.
Develop a circuit of addition four 4-bit numbers using CSA. Define carry propagation delay for the worst case.

1b73.
Develop a scheme of matrix multiplier for unsigned 4-bit numbers. Define the carry signal propagation delay in the worst case.

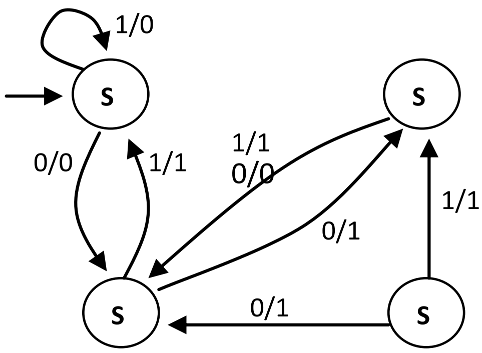
1b74.
Given below is a state transition diagram in which the states are already coded. Draw the circuit implementation of this automation.



1b75.
Determine the State-Output-Table for the given State-Transition-Graph. Which states are unreachable?

State-Transition-Graph:

	x=0	x=1



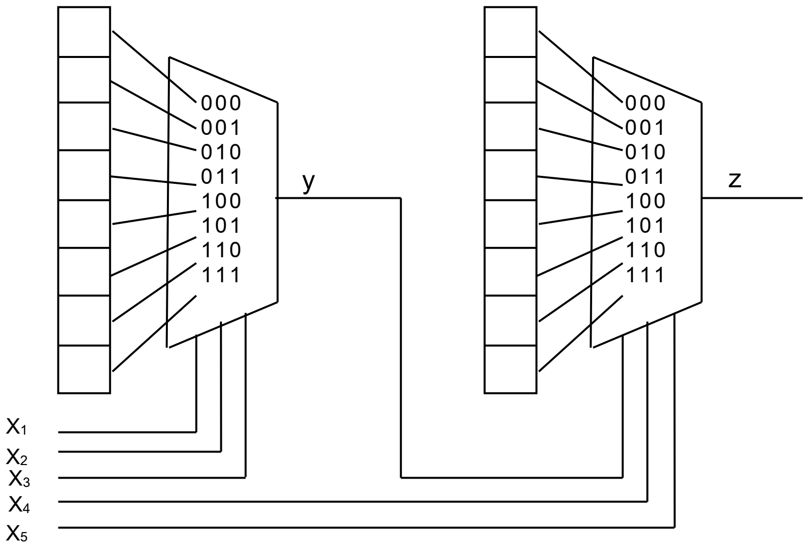
S_1		
S_2		
S_3		
S_4		

1b76.
A logic function $f(x_1,x_2,x_3,x_4,x_5)$ is decomposed into a multilevel function $z(y(x_1,x_2,x_3),x_4,x_5)$:

$$z = yx_4\bar{x}_5 + \bar{y}\bar{x}_4x_5$$

$$y = x_2x_3 + \bar{x}_1x_2 + \bar{x}_1\bar{x}_2$$

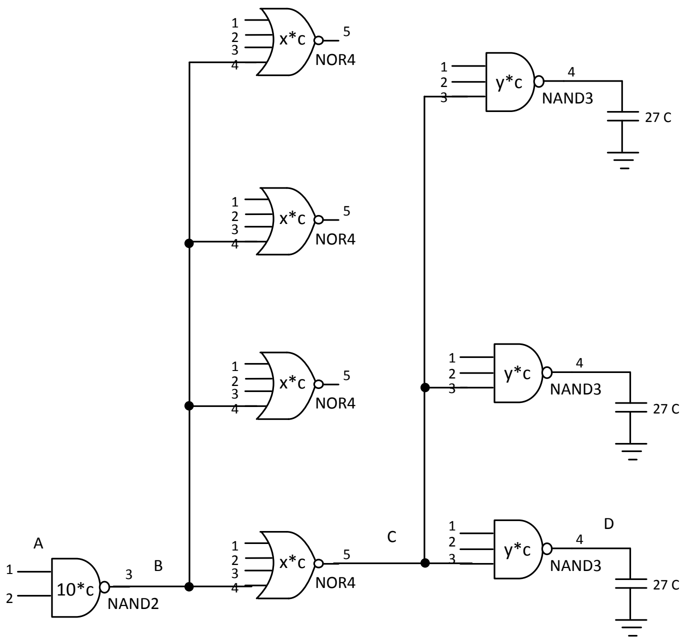
This decomposed logic function has to be realized using two lookup tables (LUTs), which are connected as shown below. Determine the logic values that have to be stored in the LUTs to implement the given function. The logic values are equal to the output of the LUT for the given row of input values.



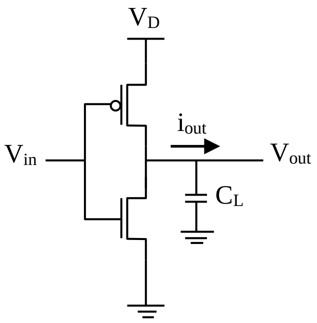
1b77.
a) Synthesize CMOS circuitry that provides output $F = \overline{(A \text{ and } B) \text{ and } (C \text{ or } D)}$;
b) Define dimensions of all transistors to obtain rising and falling times at output to be at most (worst case) equal to those that explores a unit inverter in the same technology (assume dimension of the unit inverter as $W_p/L_p=3*6\lambda/2\lambda$ and $W_n/L_n=6\lambda l/2\lambda l$).

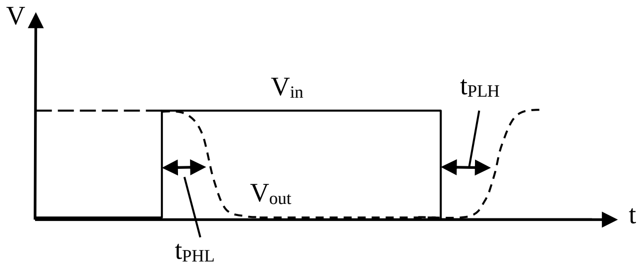
1b78.
a) Find minimal possible delay on path A - D.
b) Define dimensions of transistors in order to achieve minimal delay for the circuitry in the figure. X and Y denote multiplication factors of input capacitances in terms of capacitance of an unit nMOS (nMOS with minimal dimensions). Unit inverter input capacitance for given technology is assumed to be C_{inv}=3C, (2C from pMOS and 1C from nMOS). Give the transistor widths in terms of W_{no} of the unit nMOS.

Cell	INV	NAND2	NANDn	NOR2	NORn
Parasitic delay (p)	1	2	n	2	n
Logical effort (g)	1	4/3	(n+2)/3	5/3	(2n+1)/3



1b79.
Consider the following inverter driving a capacitive load and the V_{in}/V_{out} timing diagram shown below:





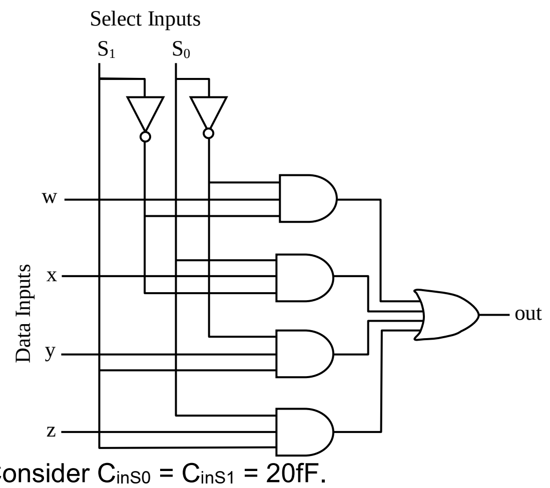
Given the capacitive load C_L = 50fF and the gate length to be L = 100nm. Consider the constants in Table 1, unless otherwise specified in the question.

a) Modeling the inverter as an RC circuit, and assuming t_{PHL}=50ps and the t_{PLH}=70ps, calculate the width of the NMOS and the PMOS transistors.

b) Calculate the switching threshold voltage V_S considering the calculated sizes in part a).

Redesign the inverter sizes such that V_S is equal to $V_{DD}/2$ exactly. Recalculate the falling and rising times.

1b80.
Consider the following multiplexer logic circuit with 2 selectors and 4 data inputs and a single output (assume all gates are identical).



Consider $C_{inS0} = C_{inS1}$ = 20fF.
Assume the ratio of the input capacitance of the selectors S_0 and S_1 to the output capacitive load is ten times (10x).

Use NANDs, and NORs with inverters to implement the ANDs and ORs. Consider the constants in Table 1, unless otherwise specified in the question.

a) Using logical effort, compute the optimal gate sizes (along the inverted path: Inverter-AND-OR) to produce minimum path delay from the selectors to the output.
b) Insert inverters along the non-inverted path of the selectors to handle the mismatch between the required input capacitance and the capacitance of the AND gates. Calculate the delay through the non-inverted path.
c) Calculate the input capacitances C_{inw} – C_{inz} for the input Data lines (w,x,y,z). If the input capacitances (C_{inw} – C_{inz}) have to be reduced to $C_{inS0}/2$ (i.e. 10fF) insert a chain of inverters into the data lines to handle the capacitance mismatch.

1b81.
Wire delay increases quadratically with wire length. With proper repeater placement, the delay of a wire becomes linear with the length of wire. Consider the constants in Table 1, unless otherwise specified in the question.

a) For a wire of length 28mm, determine the optimal size of repeaters and number of segments.
b) Compute the total delay through the buffered wire. For a 5GHz processor, how many flip-flops would be inserted in the wire to operate at this frequency? Draw a schematic of the resulting buffered wire with the flip-flops inserted (assume that the flip-flop has identical to the buffer fanout ratio).

1b82.
Consider an NMOS transistor with a threshold voltage of V_{t0}= 0.4V at room temperature (T=300ºK). A circuit designer needs to measure the impact of the voltage and temperature variations on the normalized sub-threshold leakage power consumed by the transistor. Consider W = 200nm, L=100nm, V_{ds} = V_{DD}, and V_{gs}= 0. Given that the threshold voltage is also affected by the temperature as stated by the following empirical formula:

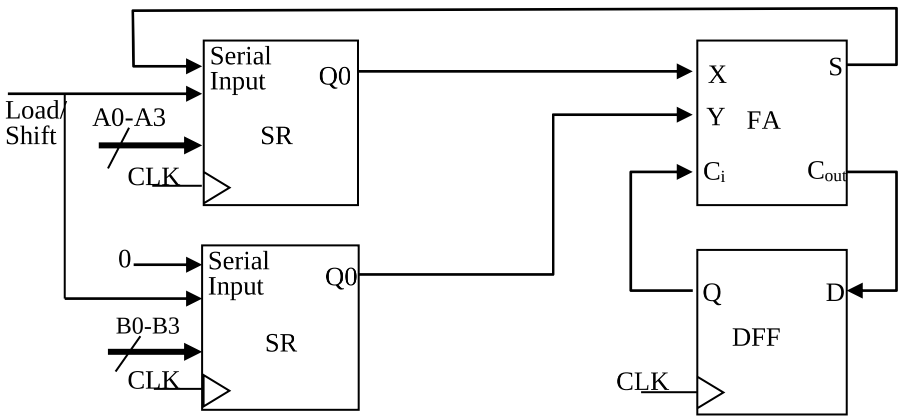
$$V_t = V_{t0} – 0.00002*\Delta T$$

where ΔT is the difference in temperature with respect to the nominal temperature 300ºK.

			Static Power Ratio
Typical	Voltage (V_{DD})	1.2V	1
	Temperature	300 ºK	
Slow	Voltage (V_{DD})	1.0V	
	Temperature	400 ºK	
Fast	Voltage (V_{DD})	1.4V	
	Temperature	270 ºK	

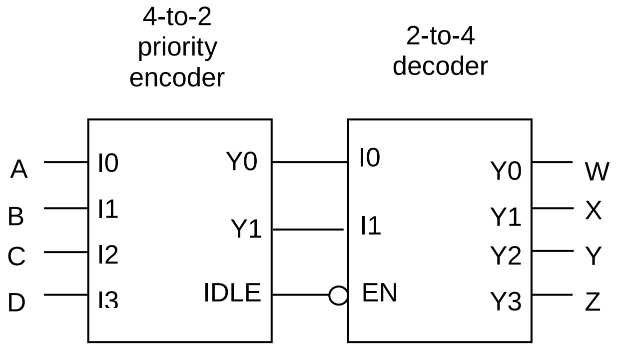
Which of the two factors has more impact on the static power consumed: the voltage or the temperature? Consider the constants in Table 1, unless otherwise specified in the question.

1b83.
Consider the following serial adder that uses a four-bit shift register (Serial Shift Register or SSR) with a load/shift control signal, DFF, and a full adder FA.



Modify the above circuit to implement an adder/subtractor (A+B/A-B). Use the two's complement for the subtraction operation. You may use XORs, MUXs, and/or DFFs as needed, keeping the circuit size at minimum. Consider the constants in Table 1, unless otherwise specified in the question.

1b84.
Consider the following circuit:



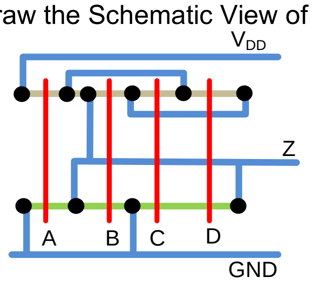
The encoder has the following priorities: I2 > I0 > I1 > I3.

Find outputs W, X, Y, and Z for all possible combinations of inputs A, B, C, and D. Consider the constants in Table 1, unless otherwise specified in the question.

1b85.

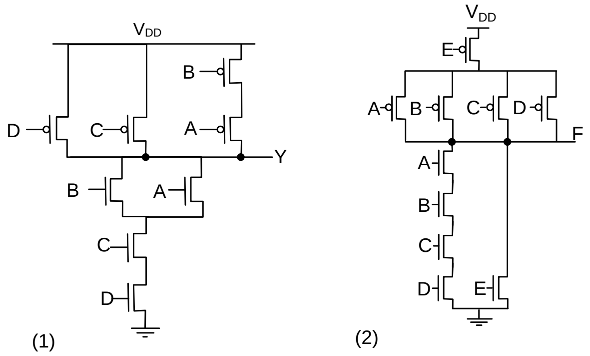
Consider the constants in Table 1, unless otherwise specified in the question.

Draw the Schematic View of the following gate:



1b86.

Consider the following two gates:



For each of the two gates:

a) Calculate the proper sizing of the PMOS and NMOS transistors for the worst-case delay scenario, such that the pull-up and pull-down equivalent sizes are equal to those of an inverter with sizes 2W, and W (for PMOS and NMOS respectively).

b) Calculate the input capacitance (gate capacitance), of input A, B, C and D based on the sizes calculated in a), ($W = W_n$= 200nm).

c) Calculate the self-capacitance based on the transistor sizes in a), ($W = W_n$= 200nm).

Consider the constants in Table 1, unless otherwise specified in the question.

Table 1

V_{DD}=1.2V	$\lvert V_{TP}\rvert=V_{TN}$ = 0.4V	E_{cn} = 6V/μm	E_{cp} = 24 V/μm
v_{sat} = 8*10^6 cm/sec	2$\lvert\Phi_F\rvert$ = 0.88V	μ_{en} =270 cm2/V-sec	μ_{ep} =70 cm2/V-sec
γ = 0.2($V^{1/2}$)	λ=0.01V^{-1}	q =1.6*10^{-19} C	n =1.4
T = 300 °K (27°C)	k = 1.38*10^{-23} J/°K	ε_o = 8.85*10^{-14} F/cm	ε_{ox} = 3.97ε_0
L= 100nm	x_d =20nm	R_{eqn} = 12.5 kΩ/☐	R_{eqp} = 30.0 kΩ/☐
C_{ox} = 1.6x10^{-6} F/cm^2	C_g = 2 fF/um	C_{eff} = 1fF/um	ρ_{Cu} = 1.7$\mu\Omega$-cm
W_{int} = 0.17μm	T_{int} = 0.8μm	C_{int} = 0.2fF/μm	V_{offset} = 0

1b87.

Design a two directional three-bit counter with the following functionality. The counter is changing its value on each positive edge of the clock. The counter's reset value is 0. After reset the counter is being incremented to value of decimal 4, then decremented back to 0, then incremented to 2, then decremented back to 0, and continue this defined whole sequence forever, i.e.:

reset, 0,1,2,3,4,3,2,1,0,1,2,1,0,1,2,3,4,3,2,1,0,1,2,1,0.......

The implementation may be done in any of hardware description languages (HDL) and the syntax accuracy is not required.

1b88.

Design a two directional three-bit counter with the following functionality. The counter is changing its value on each positive edge of the clock. The counter's reset value is 0. After reset the counter is being incremented for two steps, then is decremented back for one step, and continues this defined whole sequence forever, i.e.:

reset,0,1,2,1,2,3,2,3,4,3,4,5,4,5,6,5,6,7,6,7,0,7,0,1,0,1,2,1......

The implementation may be done in any of hardware description languages (HDL) and the syntax accuracy is not required.

1b89.

Design a three-bit increment counter with the following functionality. The counter is changing its value on each positive edge of the clock. The counter's reset value is 0. After reset the counter is being incremented to value of decimal 1, then at next step it jumps back to value of 0. Then step by step increments to 2 and again jumps back to 0. Then step by step increments to 3 and again jumps back to 0. After the reaching to value of 4 and jumping to 0 the counter should start from the beginning and continue this defined whole sequence forever, i.e.:

reset,0,1,0,1,2,0,1,2,3,0,1,2,3,4,0,1,0,1,2,0,1,2,3,0,1,2,3,4,0.......

The implementation may be done in any of hardware description languages (HDL) and the syntax accuracy is not required.

1b90.

Design a two directional three-bit counter with the following functionality. The counter is changing its value on each positive edge of the clock. The counter's reset value is 0. After reset the counter is being incremented for five steps, then is decremented back for two steps, and continues this defined whole sequence forever, i.e.:

reset,0,1,2,3,4,5,4,3,4,5,6,7,0,7,6,7,0,1,2,3,2,1,2,3,4,5,6,5,4......

The implementation may be done in any of hardware description languages (HDL) and the syntax accuracy is not required.

1b91.

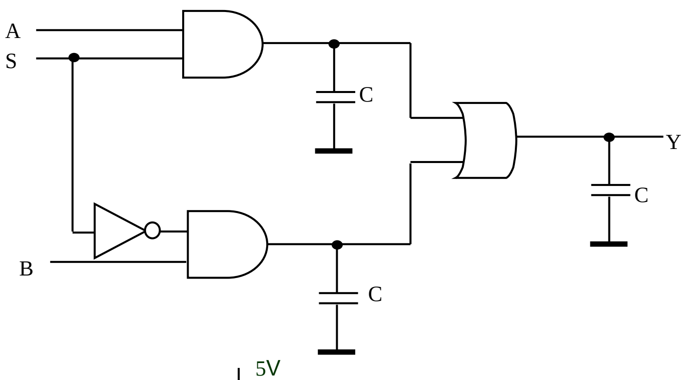
Design a logic circuit, described by $F=AB+A\bar{B}C+\bar{A}\bar{C}$ function by means of transmission gate using minimum number of transistors. Consider that normal and inverted values of variables are available.

1b92.

For a cell, described by Z=A&B+C&D function, calculate the switching probability, consuming energy in the output node if the input signals are independent and identically distributed.

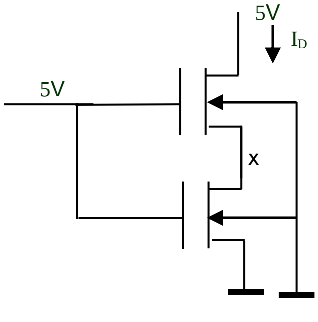
1b93.

Compute the power consumption of the presented multiplexor, considering that C=0.3 pF, VDD=2.5V, F=100 MHz, inputs are independent and identically distributed. Compute (a) for static CMOS implementation and (b) dynamic CMOS implementation



1b94.

Using the following parameters, define transistor currents: K_p'=25 mkA/V^2, V_{T0}=1.0 V, γ=0.39 V$^{1/2}$, 2|Φ_F|=0.6 V, W/L=1.

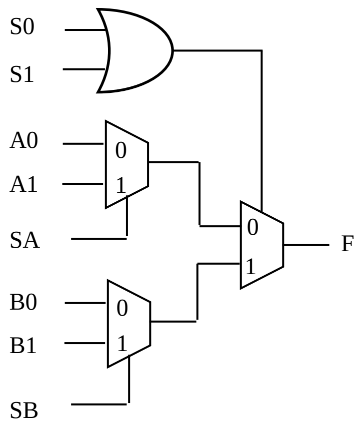


1b95.

Compute W_p of a pMOS transistor from the condition that the voltage of a switching point of a CMOS inverter is 1.2 V, if $Tox=10^{-8}$ m, VDD=3 V, μ_n=550 $cm^2/V \cdot v$, μ_p=180 $cm^2/V \cdot v$, V_{tn}=0.5 V, V_{tp}=-0.7 V, W_n=0.5 mkm, L_n=0.25 mkm, L_p=0.25 mkm.

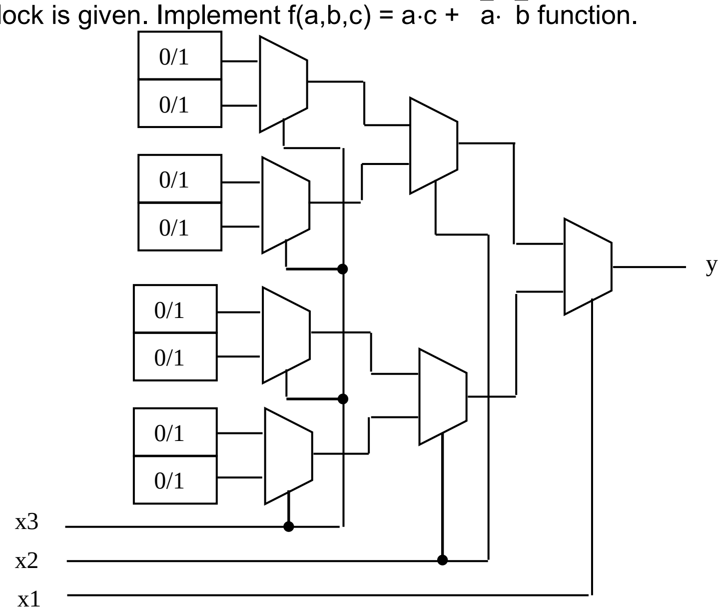
1b96.

A programmable logic block is given. Implement f(a, b,c) = $\bar{a} \cdot \bar{b} + a \cdot c + b \cdot c$ function.



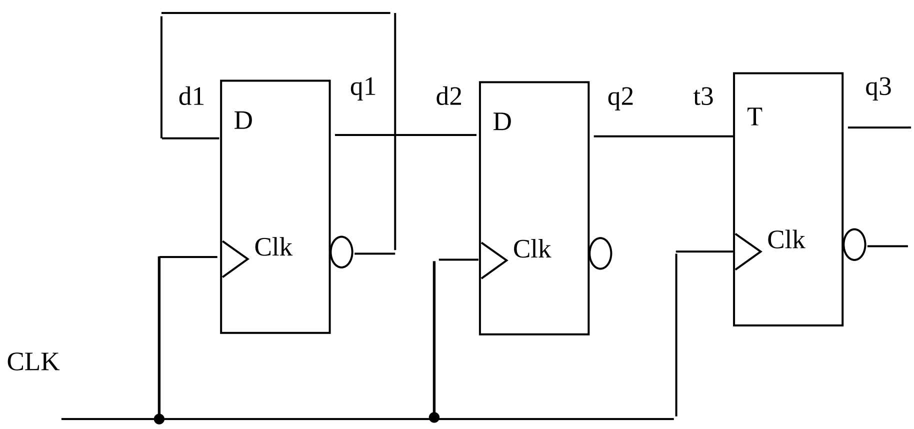
1b97.

A programmable logic block is given. Implement f(a,b,c) = $a \cdot c + \bar{a} \cdot \bar{b}$ function.



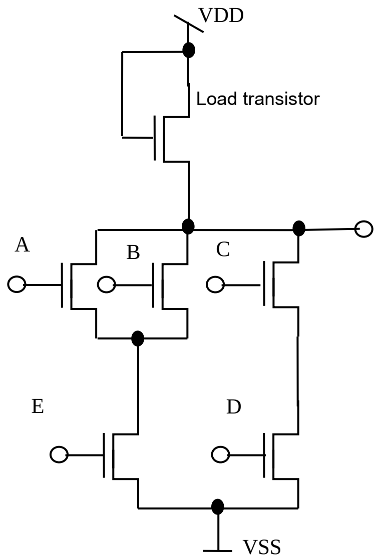
1b98.

Analyze the presented circuit. Define the sequences of all possible stats of the counter if the initial state is 000. Construct the transition graph.

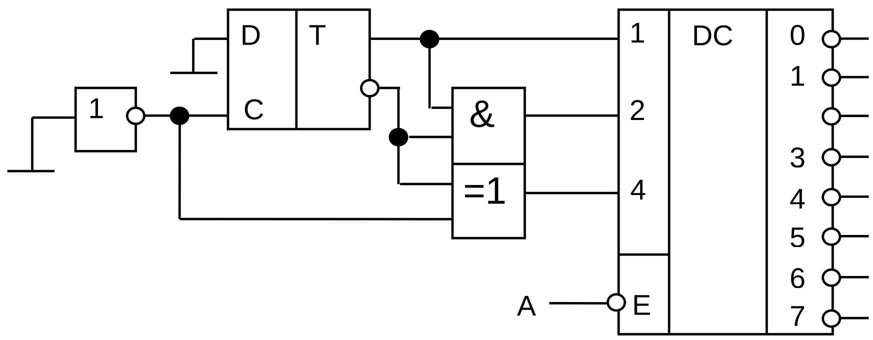


1b99.
Construct comparator of A= $a_3\ a_2\ a_1\ a_0$ B = $b_3\ b_2\ b_1\ b_0$ code by =, != using 16:1 multiplexor and 4x16 decoder. Don't use additional gates.

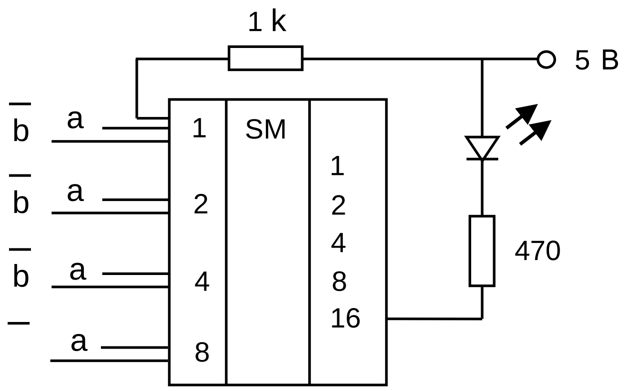
1b100.
For the given circuit of transistor level, construct the graph model of logic connections and its corresponding logic circuit.



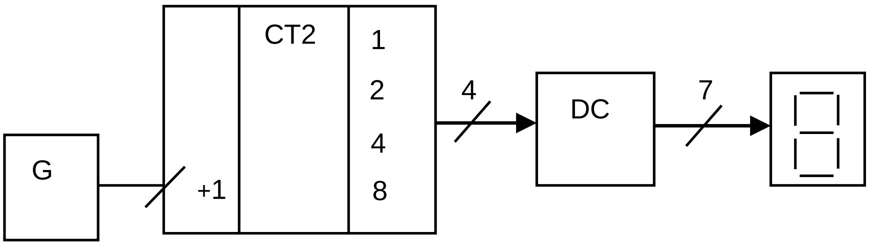
1b101.
For the circuit below, in which output of the decoder signal A is repeated? What signal will be on the other outputs of the decoder? Explain the process of solving the problem.



1b102.
4 bit A{a_1, a_2, a_3, a_4} and $\bar{B}\{\bar{b}_1, \bar{b}_2, \bar{b}_3, \bar{b}_4\}$ numbers are given to the inputs of the adder. Define what kind of comparison function of A and B numbers the output LED will detect? Explain the process of solving the problem.



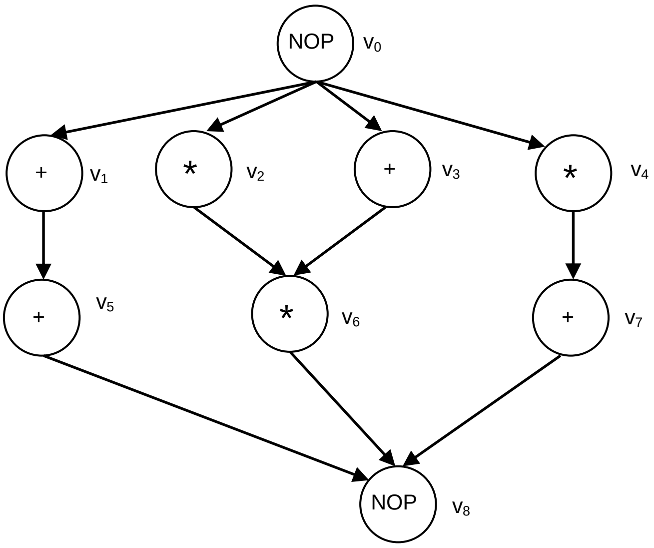
1b103.
In the presented circuit the counter is in 7 state. 125 impulse is given to its input. What number will the indicator show? Explain the process of solving the problem.



1b104.
What is considered the critical path in a combinatorial circuit? How is the mobility of an operation and the critical path in high level HW synthesis defined?

1b105.
When is it possible for a high level synthesis tool to schedule two operations at the same start time?

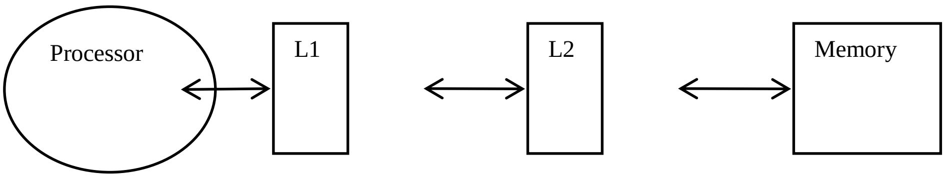
1b106.
The following sequencing graph unit is given:



Available as functional units are adders (ADD) for the add operations (+) and multipliers (MULT) for the multiplications (*). The add operation can be executed in one clock cycle and the multiplication requires two clock cycles to finish.
Compute the ASAP, ALAP times and mobility for all nodes of the graph for a maximal latency of 6.

1b107.
State two main differences between a system description with transaction level models (TLM) and on Register Transfer Level (RTL).

1b108.
A processor works at a particular frequency specified by the clock period t_clk=10ns. It is connected to two levels of data cache (L1 and L2). The L1 data cache has a hit time of 4ns. The hit rate for the Level 1 Cache is **α**. If the data is not found in the L1 cache, it is looked for in the L2 data cache. The miss penalty for the L1 cache to the L2 cache is 45ns. The hit rate for L2 cache is **β**. If the data is not found in the L2 cache either, it must be fetched from the off-chip DRAM memory. The miss penalty for the L2 cache to the memory is 483ns. It is assumed that the complete instruction memory can be accessed always in one cycle.



The execution time for an application program executing on this processor should be estimated. A total of 500 000 instructions are executed. The CPI for the processor itself is estimated to be 1.6 (CPI: cycles per instruction). About 40% of the instructions are load or store instructions.

How many wait cycles are required to access the L1 cache, L2 cache and DRAM memory?

1b109.
On average how many cycles will the processor need for a data memory access? Provide a general expression with α and β. Then compute the value for α =β=50%.

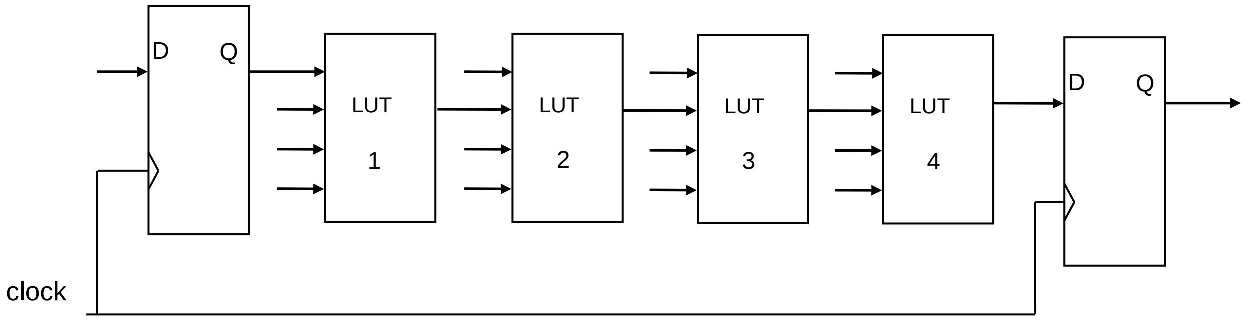
1b110.
What is the estimated execution time of the above mentioned program for α =β=50%?

1b111.
A 6-input Lookup table (LUT) inside an FPGA is to be built with the following specifications:
- The LUT is built from 5-input LUTs which share the same inputs.
- It can implement a single 6-input function or dual 5-input functions depending on how it is programmed or configured.

Use this information to design the LUT. Show all the connections and label all the signals clearly. Specify any configuration necessary to make the LUT operate in its dual 5-input mode.

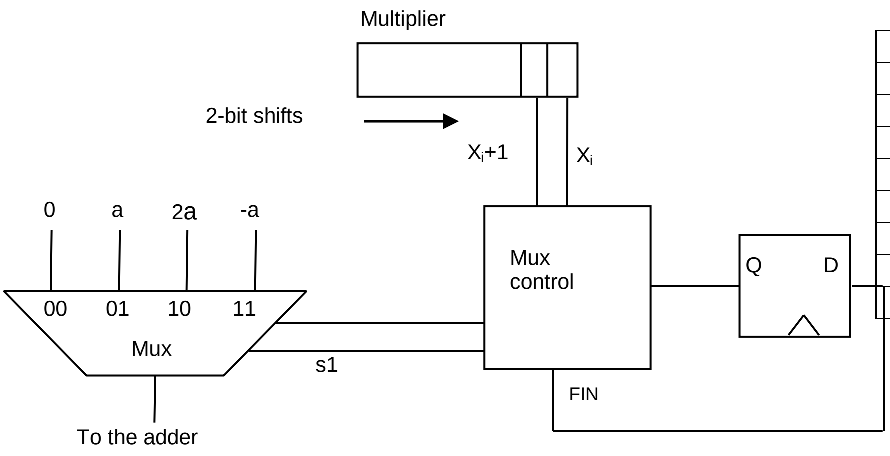
1b112.
The figure below shows an implementation of unpipelined critical path. If routing and setup and hold times are ignored and it is assumed that a single LUT delay is about 4 ns, then:

a) Estimate the clock frequency at which this design can run (assume no synthesis tool optimization options were used).
b) If the HDL code was re-written such that a third D flip-flop was inserted between LUT#3 and LUT#4, estimate the new clock frequency (again, assume no synthesis tool optimization options were used).
c) Estimate the clock frequency after the HDL modification above but now with retiming or register balancing enabled (assuming the synthesis tool is smart enough to catch this speedup opportunity).



1b113.
Derive the logic expression for all carries in a full 4-bit carry look-ahead circuit.

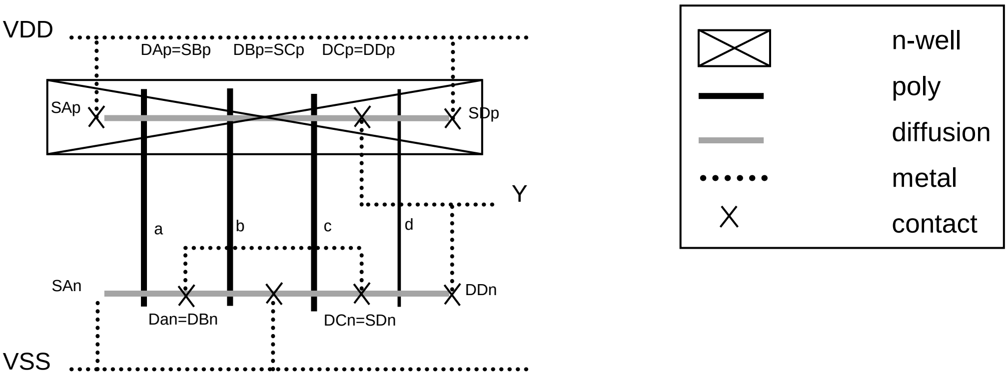
1b114.
The figure below shows the multiple generation part of a radix-4 multiplier. Fill the truth table below for the control circuit.



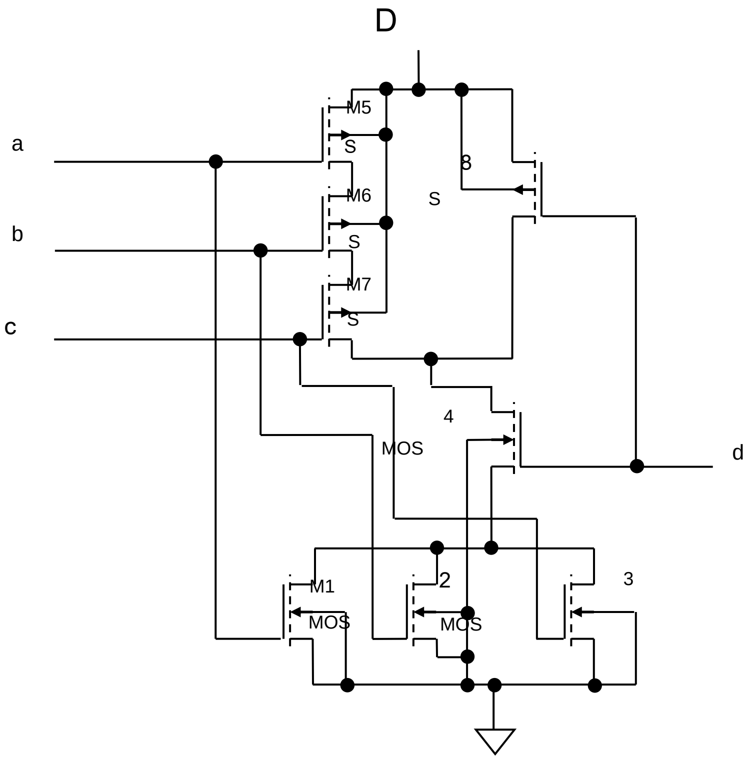
X_{i+1}	X_i	C	S2	S1	FFIN
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

1b115.
Find time-step for single step Euler's method that is sufficient to keep the local truncation error LTE $<10^{-4}$V if the expected response is v=2sin(10^3t).

1b116.
Sketch schematics of digital CMOS cell with layout represented in stick-diagram form in the figure below:



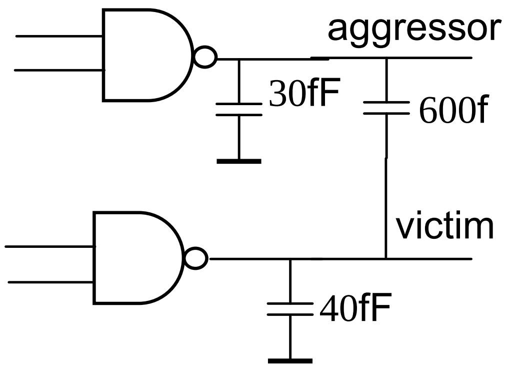
1b117.
Find W/L for all transistors in the figure to obtain the same delay as the smallest inverter for given technology that provides equal delays at rising and falling edge. Assume (μ_n/μ_p)=2, minimum active width is 3λ, while the minimum poly width is 2λ.



1b118.
Design a CMOS cell that provides logic function
$$F=\overline{(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)\;\mathrm{AND}\,d}$$

1b119. For the circuit, depicted in the figure, define the following:
a) The maximum value of the noise on the victim line, which occurs due to signal switching from 1.0 V to 0 V on the aggressor line.

b) The effective capacitance of the victim line for the delay calculation, if the aggressor line switches in the reverse direction to the victim.



1b120.

For the 3-input XOR cell, create the truth table, the output transition graph and calculate the transition probabilities.

a) when the inputs are independently equally distributed
b) when the inputs are independent and P(A=1)=0,2, P(B=1)=0,4, P(C=1)=0,6

1b121.

Construct a CMOS cell which implements X=((!A+!B)(!C+!D+!E)+!F)!G function. Choose the sizes of transistors such that the output resistance is the same as in NMOS W/L = 2 and PMOS W/L = 6 inverter.

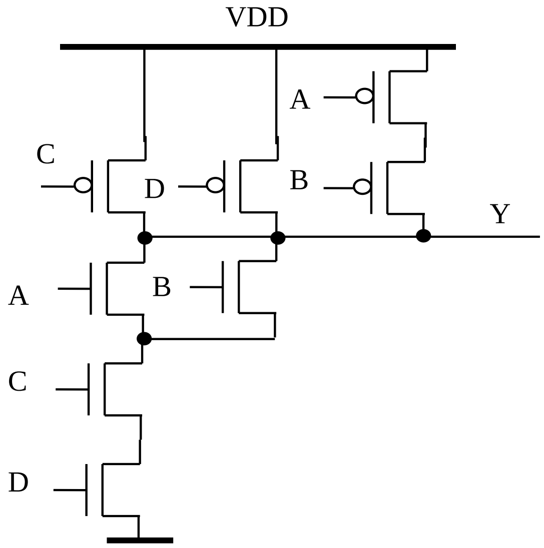
1b122.

Consider the circuit, given in the figure.

a) What logic function does the circuit implement?

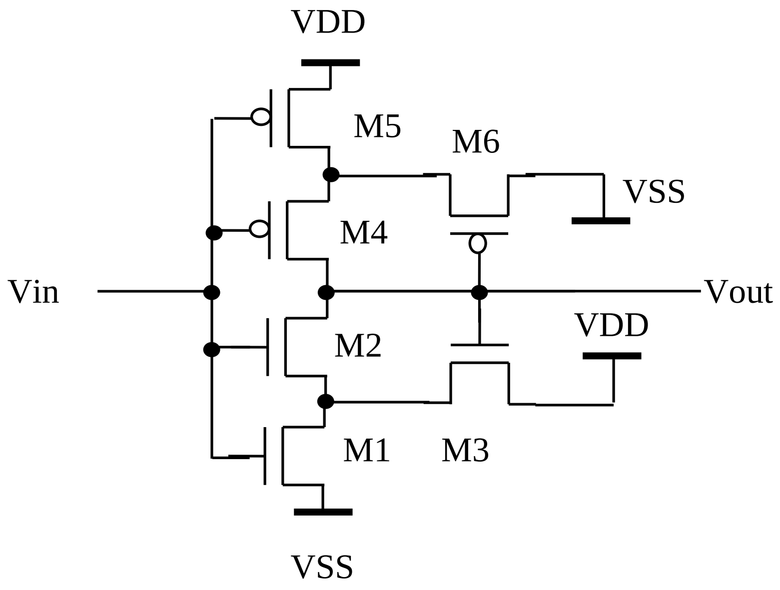
b) Determine the transistors' sizes such that the output resistance is equal to the inverter's resistance with NMOS W/L = 4 and PMOS W/L = 8 sizes.

c) In case of what input sets the maximum t_{pHL} and t_{pLH} delays are reached?

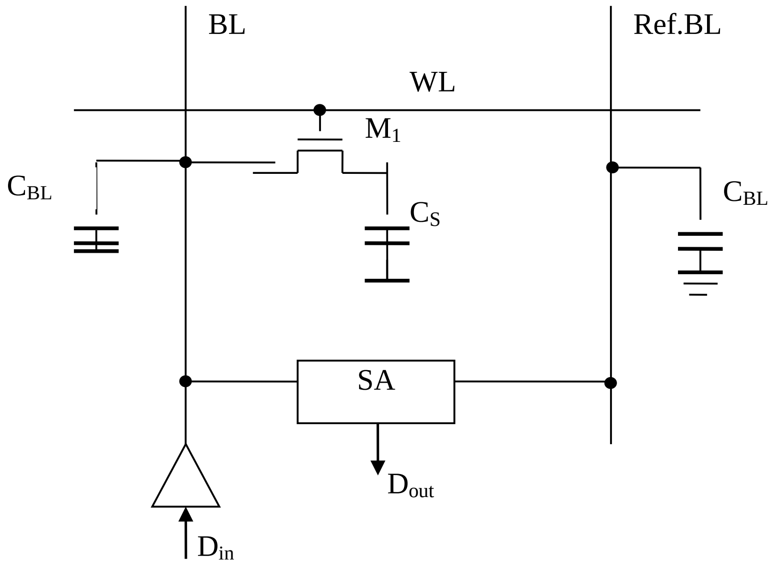


1b123.

Determine the threshold voltages of the Schmitt trigger given in the figure if W_1=9 um, W_2=18 um, W_3= 7um, W_4=54um, W_5=27um, W_6= 22um; V_{tn}=0,6 V; V_{tp}=-0,7 V; Ln=0,4 μm; Lp=0,4 μm, VDD=3,3 V.



1b124.
The Bit Line (BL) in the 1T dynamic cell, given in the figure, can be charged by the VDD/2 clocked precharging circuit (not shown in the figure). Using the parameters given below, V_{To}= 1,0 V, γ= 0,3 $V^{1/2}$, $|2\Phi_F|$ = 0,6V, determine the voltage across the capacitance Cs when a "1" bit is written, the bit line voltage is VDD= 5V during the writing.

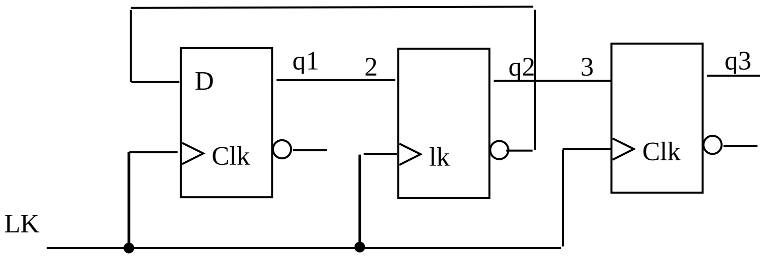


1b125.
Develop a circuit that will compute the number of "1"s in a 9-bit input code. Describe the device by Verilog.

1b126.
By means of Carnough map define if there is static hazard in the circuit of $y=\bar{x}1\cdot\bar{x}3+x2\cdot x3+x1\cdot\bar{x}2\cdot x4$ function. If so, get rid of the hazard.

1b127.
Construct a negative edge controlled DFF (master-slave) circuit of synchrosignal, based on two 2:1 multiplexors.

1b128.
Analyze the presented circuit. Define all possible sequences of states of the calculator. The initial state of the calculator is 000.



1b129.

The following assembly code is given:

```
SUB     R2, R1, R2      // R2=R1-R2
ADD     R4, R3, R2      // R4=R3+R2
BNEZ    R1, B1          // Go to B1, if R1 is not equal zero
ADD     R4, R4, R4      // R4=R4+R4
SUB     R2, R2, R1      // R2=R2-R1
B1:     ADD     R4, R4, R2      // R4=R4+R2
```

The code runs on the RISC micro-architecture with a five-stage pipeline with the stages:

Instruction Fetch - Instruction Decode – Execute – Memory Access – Write Back

The micro-architecture has no data forwarding implemented. The micro-architecture has no branch prediction implemented. It will always assume that the branch will not be taken.

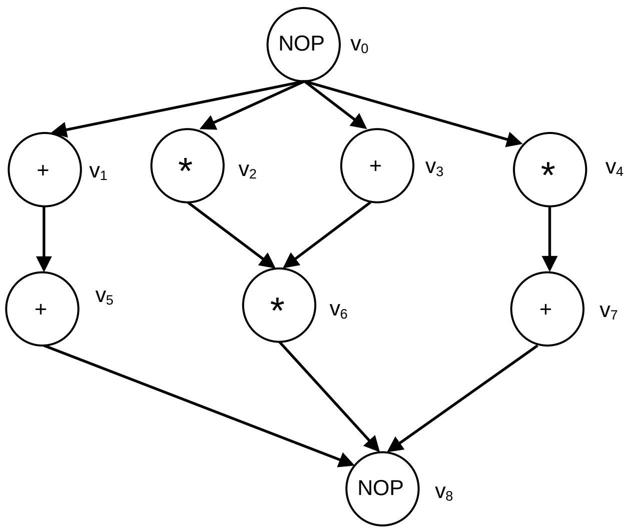
Mark possible data hazards in the code that may arise from an execution on a RISC processor with five-stage pipeline.

1b130.

Calculate how many cycles the execution of this program takes for both the execution when the branch is taken and when it is not taken. Data and control hazards should be considered.

1b131.

The following sequencing graph is given:



Available as functional units are ALUs for the add operations (+) and compare operations (>) as well as multipliers for the multiplications (*).
The add operation and compare operation can be executed in one clock cycle and the multiplication requires three clock cycles to finish.
Compute the as-soon-as-possible (ASAP) start times for all operations:

1b132.
Compute W of a pMOS transistor from the condition that the voltage of the switching point of a CMOS inverter is 0.9 V, if Tox=10^{-8} m, VDD=1,8 V, μ_n=540 $cm^2/V{\cdot}v$, μ_p=180 $cm^2/V{\cdot}v$, V_{tn}=0,5 V, V_{tp}=-0,6 V, W_n=0,5 mkm, L_n=0,15 mkm, L_p=0,15 mkm.

1b133.
Define the number of stages of non-inverting buffer, consisting of inverters with progressive dimensions and the progression coefficient of gate width from the condition of getting minimum delay. Consider C_{in1}=2fF, C_{load}=200fF.

1b134.
For the circuit, presented below V_{DD}=2,5V, 2|Φ_F|=0,6V, Vtp0=-0,6V, Vtn0=0,5V, define:
a) Voltage change boundaries in the output when γ=0.
b) Calculate V_{OH} with consideration of body effect. Consider γ= 0,5$V^{1/2}$ for NMOS and PMOS transistors.

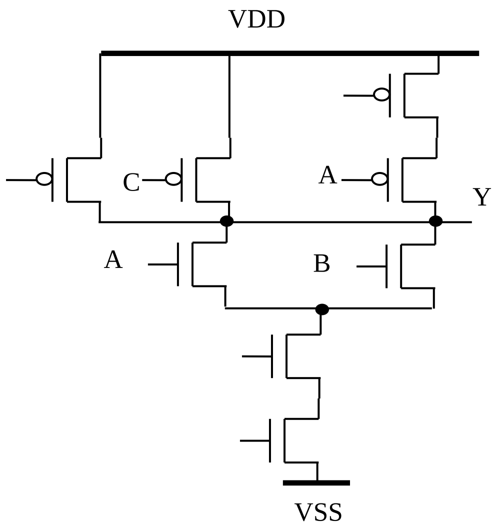
1b135.
Design the CMOS cell circuit, the output of which is in high logic state only in case of the following combinations: 0,4,6.

1b136.
C=1,5pF capacitance is connected to the end of interconnect line with L=100μm length, line parameters are c=2Ff/μm, r=0,10 Ohm/μm. Define propagation delay in the line.

1b137.
For 3-input AND cell, calculate the energy consuming switching probability at the output node if the input signals are independent and distributed as follows: P_{1A}=0.25, P_{1B}=0.5, P_{1C}=0.75.

1b138.
For a cell, described by Z=A&B+C&D function, calculate the energy consuming switching probability at the output node if the input signals are independent and identically distributed.

1b139.
Define the power consumption in the presented circuit if P(A=1)=0,5, P(B=1)=0,2, P(C=1)=0,3 and P(D=1)=0,8, VDD=2,5V, C_{out}=30fF and F_{CLK}=250MHz.



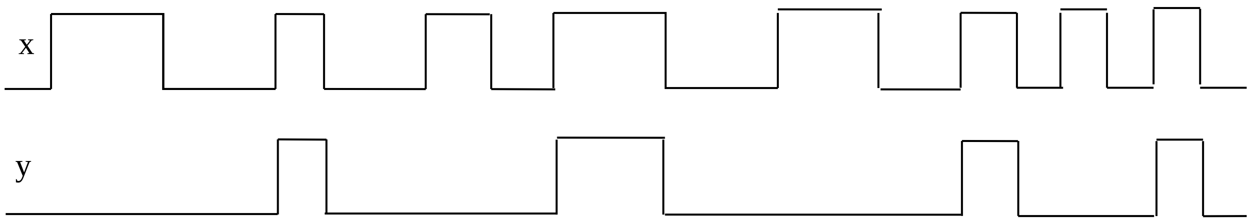
1b140.
Given a 50% duty-cycle continuous succession of clock pulses at a fixed frequency (the duty-cycle is the percentage of one period in which a signal is active). This frequency needs to be divided by 3 keeping 50% duty cycle for resulting pulses. Use logic "OR", "AND", "NOT" gates and/or "D"-flip-flops as needed. The implementation may be done in either principal schematic, in any of hardware description languages (syntactic correctness is not required).

1b141.
Given a 50% duty-cycle continuous succession of clock pulses at a fixed frequency (the duty-cycle is the percentage of one period in which a signal is active). This frequency needs to be divided by 5 keeping 50% duty cycle for resulting pulses. Use logic "OR", "AND", "NOT" gates and/or "D"-flip-flops as needed. The implementation may be done in either principal schematic, in any of hardware description languages (syntactic correctness is not required).

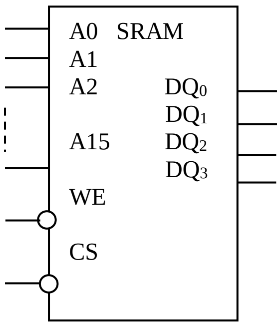
1b142.
Given a 50% duty-cycle continuous succession of clock pulses at a fixed frequency (the duty-cycle is the percentage of one period in which a signal is active). This frequency needs to be divided by 7 keeping 50% duty cycle for resulting pulses. Use logic "OR", "AND", "NOT" gates and/or "D"-flip-flops as needed. The implementation may be done in either principal schematic, in any of hardware description languages (syntactic correctness is not required).

1b143.
Given a 50% duty-cycle continuous succession of clock pulses at a fixed frequency (the duty-cycle is the percentage of one period in which a signal is active). This frequency needs to be divided by 9 keeping 50% duty cycle for resulting pulses. Use logic "OR", "AND", "NOT" gates and/or "D"-flip-flops as needed. The implementation may be done in either principal schematic, in any of hardware description languages (syntactic correctness is not required).

1b144.
An asynchronous circuit has an input **x** and an output **y**. A sequence of pulses is applied on input x. The output has to replicate every second pulse, as illustrated in the figure. Design a suitable circuit.



1b145.
Design static memory module with size 128K×8 using Intel 51258 chips. Chip size – 64K × 4. IC Logic symbol is shown in the figure.



1b146.
Consider the function $f(x_1,x_2,x_3)=\Sigma m(1,3,5,6,7)$. Show how it can be implemented using two two-input LUTs. Give the truth table implemented in each LUT.

1b147.
Draw a circuit, that corresponds to the presented Verilog code.

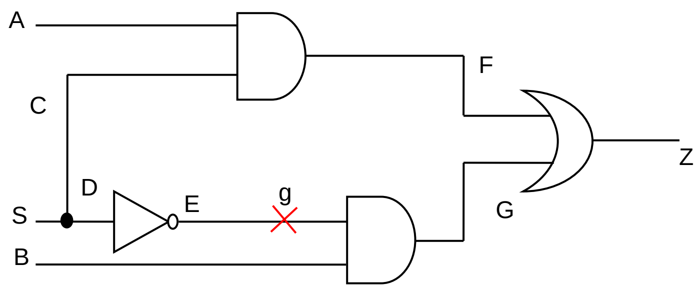
```
module lfsr(D,load, clk,Q);
input [0:4] D;
input clk,load;
output reg[0:4] Q;
        always @(posedge clk)
        if (load)
```

```
Q<=D;
else Q<={Q[4],Q[0],Q[1]^Q[4],Q[2],Q[3]};
endmodule
```

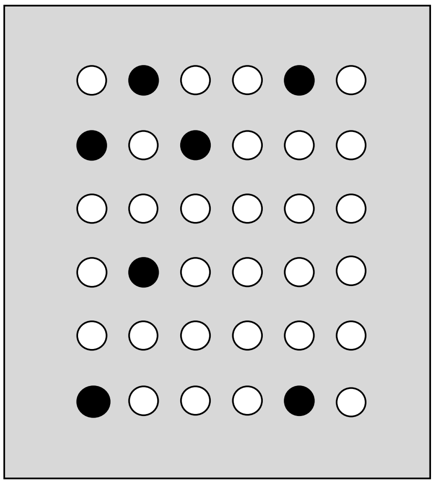
1b148.
The n-cell memory is bit-oriented and has the form of a square matrix. Estimate the order of the complexity of the traditional algorithm GALRow for testing of the memory.

1b149.
Construct a March test of minimal complexity that will have a minimal number of March elements and will detect all Transition faults: <↑/0>, <↓/1>.

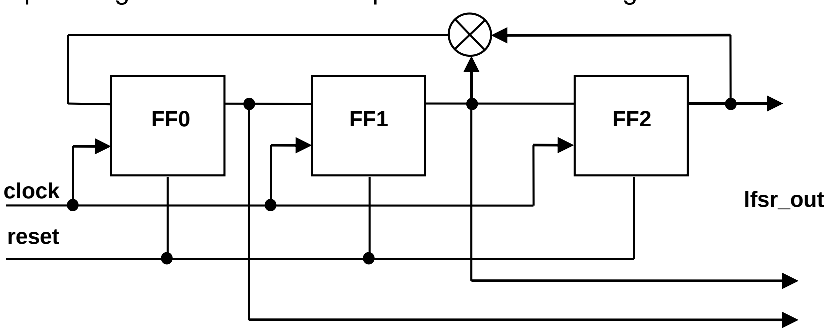
1b150.
Using the method of Boolean differences, find all test patterns detecting the faults Stuck-at-0/1 on the line E in the following circuit:



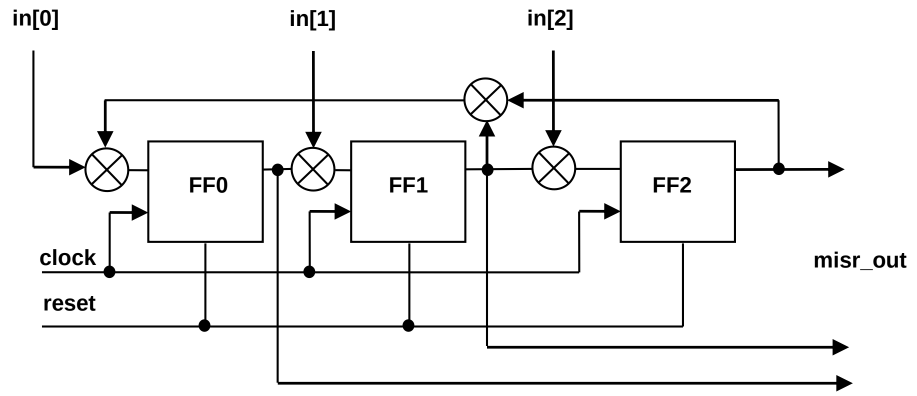
1b151.
In the depicted memory of size 6x6, repair the faults denoted as black circles by means of two spare rows and two spare columns.



1b152.
The Figure below presents a Linear Feedback Shit Register (LFSR) having $P(x) = 1 + X^2 + X^3$ characteristic polynomial. Develop Verilog RTL module for the presented LFSR using the 001 seed.

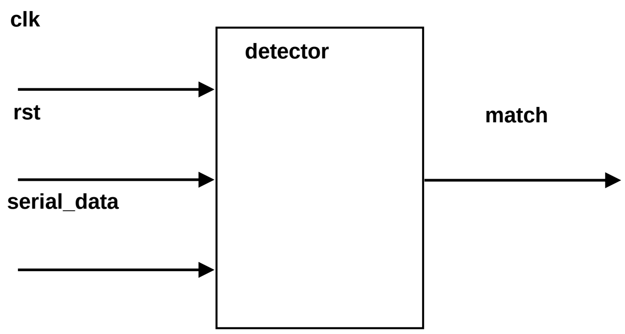


1b153.
The Figure below presents a Multiple Input Shit Register (MISR) having $P(x) = 1 + X^2 + X^3$ characteristic polynomial. Develop Verilog RTL module for the presented MISR.



1b154.

The Figure below presents a detector of serial combination. The serial combination is shifted in through the **serial_data** input synchronously with clock **clk**. The **match** output is set to 1 if the current shifted-in 7 bits match the detected combination (otherwise the **match** output is set to 0). The **detector** Verilog RTL module below presents the implementation of the detector for 1010110 combination (the left-most bit is shifted-in first). After synthesis the presented module will contain 8 flip-flops (**shift_r** and **match_r** variables). Redevelop the module to reduce the number of flip-flops to 4.

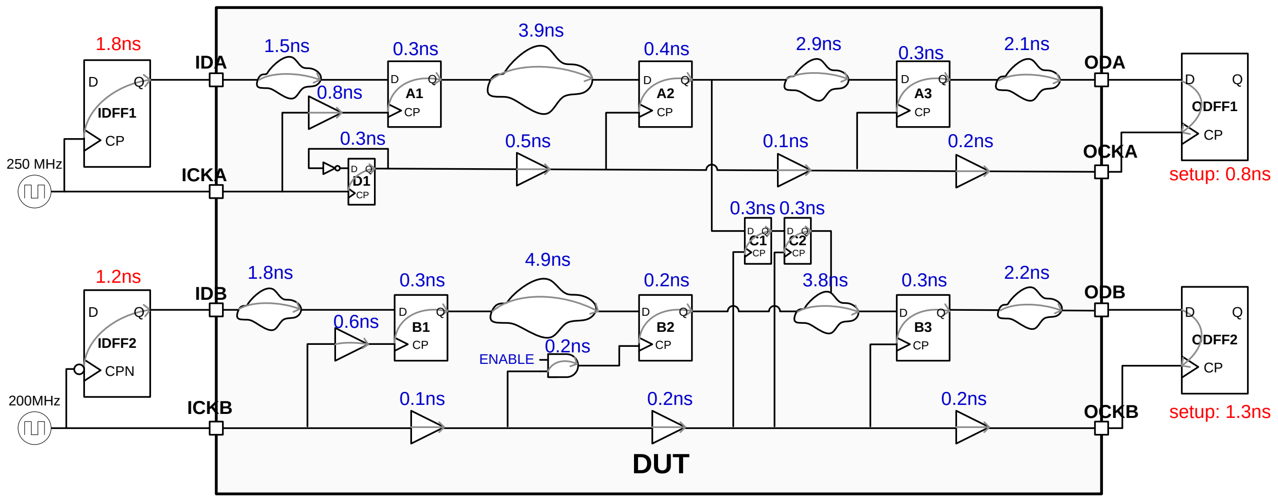



```
//Serial detector of '1010110' combination
module detector (clk, rst, serial_data, match);
input clk, rst, serial_data;
output match;
//Variables
reg match_r, match_nxt;
reg [6:0] shift_r, shift_nxt;

//Assignment
assign match = match_r;
//Shift register
always @ (shift_r or serial_data)
shift_nxt = {shift_r[5:0],serial_data};
//Comparator
always @ (shift_r)
match_nxt = (shift_r[6:0] == 7'b1010110);
//Non-blocking assignment
always @ (posedge clk or negedge rst)
```

```
if(!rst)
      begin
            shift_r <= #1 7'b0;
            match_r <= #1 1'b0;
      end
else
      begin
            shift_r <= #1 shift_nxt;
            match_r <= #1 match_nxt;
      end
endmodule //module detector
```

1b155.

Please do setup timing analysis on the below DUT circuit, the known input clock frequency ICKA is 250MHz, and ICKB is 200MHz, the detail circuit structure is shown as below:



1) The above figure shows maximum delays of all the gates and nets as well as the Register and IO port names, clock uncertainty can be ignored. Write the complete timing constraint for DUT circuit. It is required to cover all timing paths including Register-to-Register, Input-to-Register and Register-to-Output. Note that B2 always captures new data every 2 clock cycles under the control of FSM.

2) Consider Register-to-Register timing paths only. Analyze and calculate the worst timing slack (WNS) of every existing clock domain. Assume Register's Tsu (library setup time requirement) is 0.1 ns. After WNS calculation also calculate the actual maximum clock frequency, run in theory. (6 points)

3) If there is any timing violations found when calculating WNS, point out the corresponding critical paths. List at least two ways to clean the timing. (5 points)

1b156.

For F = A.B.C+ B.C.D + A.B.C , write the truth table. Simplify using Karnaugh map and implement the function using NAND gates only.

1b157.

Given an n-variable Boolean function $f(x_1, x_2, \ldots, x_n) = x_1 \vee x_2 \vee \ldots \vee x_n$, construct the Binary DecisionDiagram of function $f(x_1,\ldots, x_i,\ldots, x_n)$.

1b158.

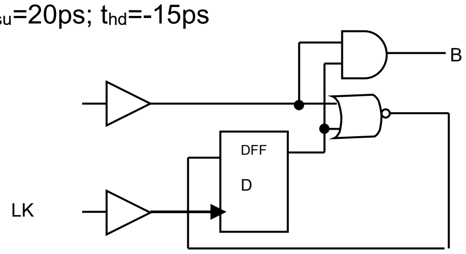
Construct a March test of minimal length for detection of all basic faults in address decoder after the occurrence of which the device is still a combinational circuit (no feedback loops).

1b159.

For the circuit shown below:

a. What is the external setup and hold times for input A?
b. What is the delay from CLK to output B?
c. What is the CLK maximum allowed frequency?

Assume:
t_{buf}=120ps; t_{and2}=150ps; t_{nor2}=160ps;
DFF: t_{c2q}=200ps; t_{su}=20ps; t_{hd}=-15ps

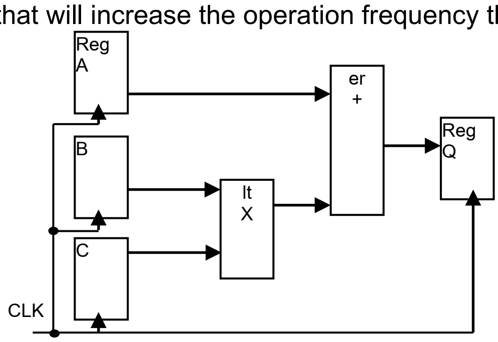


1b160.

Design CMOS cell implementing Z=!(A(B+C)+BD) Boolean function.
Determine the MOS device sizes to have the same strength as minimum size inverter; assuming for the inverter W_{PMOS}/W_{NMOS}=2/1, only one input is switching at a time.

1b161.

For the figure below:
a. Determine the maximum allowed operating frequency if t_{mult}=25ns, t_{adder}=22ns, t_{c2q}=0.5ns, t_{su}=0.2ns.
b. Modify the diagram to add one level of pipelining but still maintain the same functionality. Add the pipeline stage in the place that will increase the operation frequency the most, compute the new operating frequency.

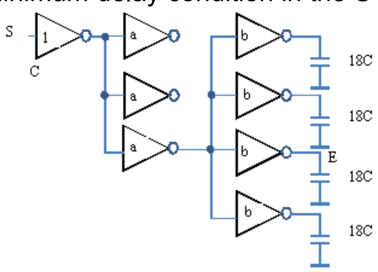


1b162.

Determine the sizes of a minimum delay progressive buffer implemented on inverters. Assume for the first stage $W_{P1}/L=2$; $W_{N1}/L=1$; C_{in1}=2fF, C_{load}=200fF.

1b163.

For the circuit shown below, the input capacitance of the first stage inverter is *C*. Determine the scale factors ***a*** and ***b*** from the minimum delay condition in the S-to-E path.

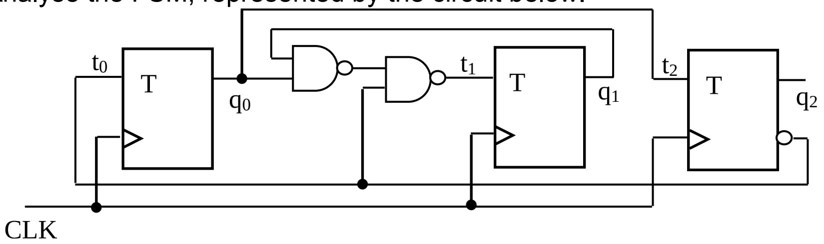


1b164.

Design a CMOS circuit implementing $Y = (C + D)(A + B)$ Boolean function, using minimum number of 2:1 two-way selectors.

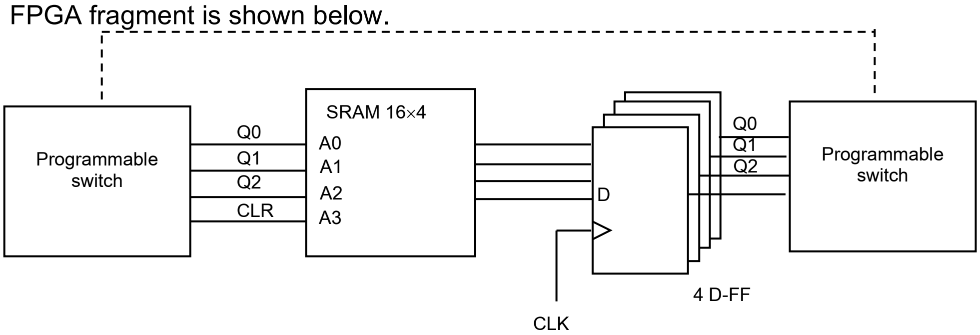
1b165.

Analyse the FSM, represented by the circuit below.



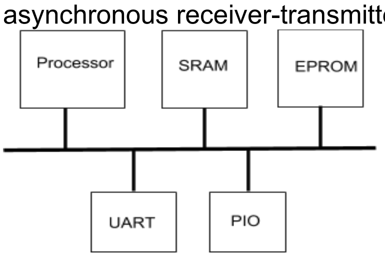
1b166.

Implement a modulo 8 counter with reset, based on FPGA. LUT (Look-up table) has 4 inputs and 4 outputs. Show LUT configuration.
FPGA fragment is shown below.

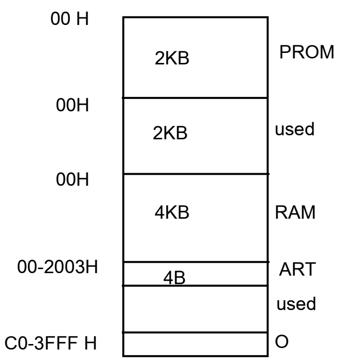


1b167.

Suppose there is a microprocessor-based system consisting of a CPU, SRAM, EEPROM. UART (Universal asynchronous receiver-transmitter) and PIO (parallel interface) are input/ output devices.



Processor address bus width is 14 bit.
Design a circuit of address decoding. Use memory-mapped I / O.
EEPROM requires 2KB of address space beginning at zero address, SRAM requires 4 KB of address space beginning at 4KB. UART uses 4 bytes of address space starting at 8KB. PIO requires 4 most significant bytes of address space (3FFC-3FFF).
Memory map:



1b168.

Implement a ROM of size 16x4, using decoder and OR gates. Cells with addresses 0,2,15 hold code 10, cells with addresses 1,8,13 - code 8, cells with addresses 3,12 - code 5, cell with address 14 – code 4. The remaining cells contain 0.

1b169.

Given the truth table of a logic circuit having two inputs (A, B) and one output (Z).

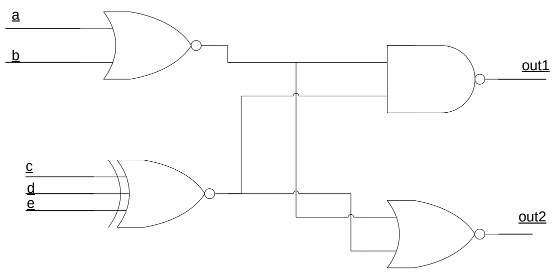
A	B	Z	T_1	T_2	T_3	T_4	T_5	T_6
1	1	1						
1	0	1						
0	1	1						
0	0	0						

It is required:

1. Determine what Boolean logic implements the given truth table and present the schematic symbol of that logic in gate level.
2. Build the basic circuit that implements the given logic in transistor level, using three nMOS and three pMOS transistors.
3. Fill in T_1, T_2,..., T_6 columns of the table with «on» or «off» words respectively.

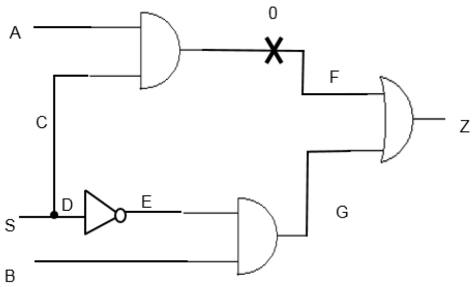
1b170.

Develop Verilog description for the circuit presented in the figure below. Declare the **out1** and **out2** variables as **reg**:



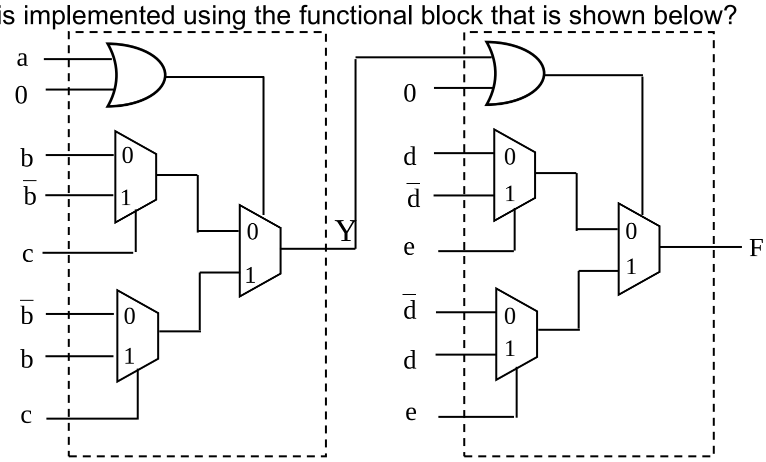
1b171.

By using the well-known method of Boolean differences, for the stuck-at-0 fault (s-a-0) on the line F in the logical circuit depicted below, find the set of all input (test) patterns that detect the fault.

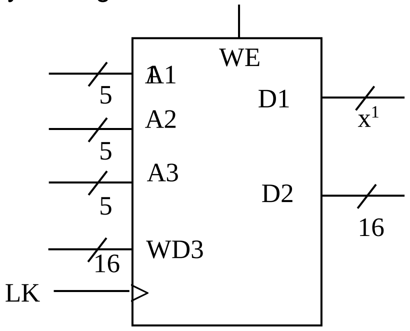


1b172.

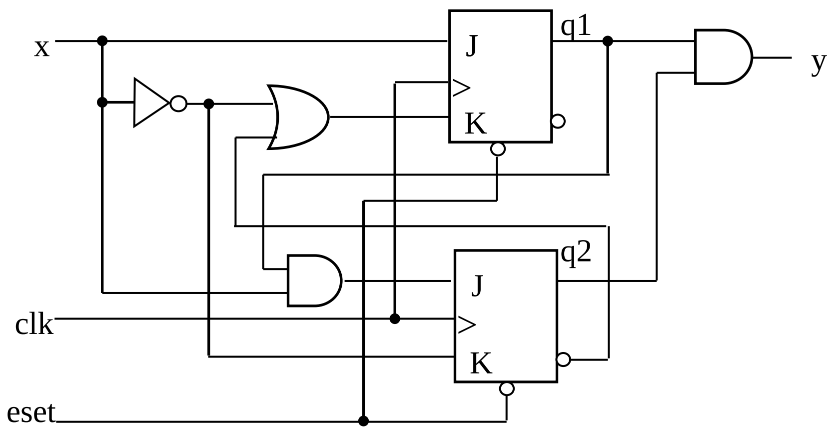
Which function is implemented using the functional block that is shown below?



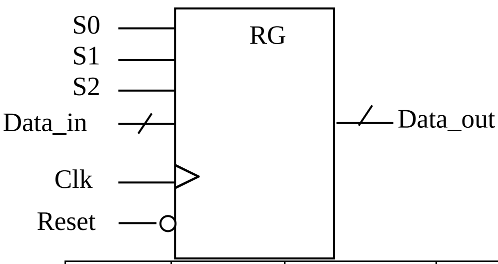
1b173.
By Verilog, describe a 32×16 3-ports register file. The figure below shows logic symbol of the register file. The register file has two read ports (A1/RD1, A2/RD2) and one write port (A3/WD3). Read operations are asynchronous, write operations – synchronous.
Describe the register file by Verilog.



1b174.
Analize the clocked synchronous FSM, represented in the figure below. Draw the state transition graph of the FSM.



1b175.
By Verilog, describe a multifunctional 16-bit shift register, the operation of which is given by the table below. Logic symbol of the register is presented in the figure below.



reset	clk	S2 S1 S0	Function
0	x	x x x	Reset
1	↑	0 0 0	Hold
1	↑	0 0 1	Logical Shift right 1 bit
1	↑	0 1 0	Shift left 1 bit
1	↑	0 1 1	Increment (+1)
1	↑	1 0 0	Rotation to 1 bit right
1	↑	1 0 1	Rotation to 1 bit left
1	↑	1 1 0	Load
1	↑	1 1 1	Decrement (-1)

1b176.
For the function $y = x1 \cdot \overline{x}2 + x3 \cdot x4 + \overline{x}2 \cdot x3$ design a circuit based on 2: 1 multiplexers. Use ROBDD.

2. ANALOG INTEGRATED CIRCUITS

a) Test questions

2a1. How is the balancing of the differential amplifier executed?

A. By applying additional biasing to one of inputs
B. Through external potentiometer connected between load resistors of two branches
C. By changing supply voltage value
D. A. and B. answers are correct
E. All the answers are wrong

2a2. What differences are between inverting and non-inverting adders based on operational amplifier?

A. Output signal's phase
B. There is interaction of signal sources in inverting adder
C. In inverting adder inputs are limited
D. Interaction of signal sources is absent in inverting adder
E. B. and C. answers are correct

2a3. Input resistance for differential signal of differential amplifier can be increased by:

A. The increase of resistors in emitter circuits
B. The increase of transistors'βs
C. The application of Darlington's transistors
D. The application of field transistors
E. All the answers are correct

2a4. What is the advantage of "R – 2R" matrix towards "R − 2R − 4R − 8R matrix in digital-analog converters?

A. More precise
B. Can be multibit
C. The current of reference voltage is constant
D. Is being heated in a more uniform way
E. All the answers are correct

2a5. Which analog-digital converter (ADC) is the fastest?

A. Sequential ADC
B. Parallel ADC
C. Double integration ADC
D. The speed depends on the applied cells
E. The most high-speed is not mentioned among the answers

2a6. Why does the increase of collector resistor value lead to transistor's saturation mode in a common emitter circuit?

A. Because it leads to collector voltage increase
B. Because it leads to base current increase
C. Because it leads to collector current increase and contributes to transistor opening
D. All the answers are correct
E. All the answers are wrong.

2a7. What is the differential amplifier's application limited by?

A. Large input resistance
B. Large output resistance
C. The difference of input resistances for common mode and differential signals
D. Large amplifier coefficient
E. All the answers are correct

2a8. What is the reason of occurrence of disbalance of differential amplifier?

A. Transistors of two branches are not similar
B. Difference of resistance values between two branches
C. The summary difference between both transistors and resistors of two branches
D. Non ideal nature of the power source
E. All the answers are correct

2a9. What properties are demonstrated by active integrator from the perspective of frequency?

A. High pass filter
B. Low pass filter
C. Band-pass filter
D. Rejecter filter
E. Has no filtering properties

2a10. The random variable signal conversion accuracy of ADC depends on:

A. Comparator accuracy
B. Resistors accuracy in R-2R matrix of internal DAC
C. Bit count of ADC
D. Performance of ADC elements
E. All the answers are correct

2a11. The quality of current source in differential amplifier depends on

A. High internal resistance

B. Thermostability
C. Current value
D. A, B, C answers are correct
E. A, B answers are correct

2a12. Analog IC production group method is based on the following factors:
A. Parameter similarity of elements produced during the same technological process
B. Elements on crystal, which are placed close to each other, heat evenly
C. Elements thermal coefficient similarity
D. A, B, C answers are correct
E. Technological restrictions on element implementation

2a13. What is the minimum value of the resistance of OpAmp negative feedback limited by?
A. Ku=1 request
B. Thermal instability of input current
C. Permissible minimum value of resistance of OpAmp output load
D. No limitation
E. All the answers are wrong

2a14. In voltage stabilizer by OpAmp application why is the feedback given to the inverse input not from OpAmp output, but from the output of output emitter repeater
A. To fade the loading of OpAmp
B. To fade stabilitron current given to the direct input
C. To compensate thermal instability of the output emitter repeater
D. To increase amplifier’s coefficient of OpAmp
E. All the answers are correct

2a15. What factors is the redundancy principle of analog microcircuitry based on?
A. Technological restrictions of element preparation
B. On those elements of the circuit which are not possible to carry out in crystal or occupy too much area, are substituted by multielement node which implements the same function.
C. A. and B. answers are correct
D. On placing redundant elements on crystal area
E. Minimization of the number of circuit elements

2a16. Why does not the emitter oscillate the voltage?
A. Because the output voltage must always be smaller than the one of the input for open state of the transistor
B. Because it is not possible to increase large nominal resistance in emitter circuit
C. Because the output signal is taken from transistor’s emitter
D. Because the emitter repeater cannot provide large output resistance
E. All the answers are correct

2a17. What is the role of additional emitter repeater in current mirror?
A. Has no influence
B. Increases the output current of current mirror
C. Balances current mirror
D. Increases the output resistance of current mirror
E. All the answers are wrong

2a18. What is the comparator’s sensibility, built on OpAmp, conditioned by?
A. Input resistances of OpAmp
B. Value of supply voltage
C. Own amplifier’s coefficient of OpAmp
D. Debalance of OpAmp
E. All the answers are wrong

2a19. What is the advantage of double integration of ADC?
A. Increases the conversion accuracy
B. Thermal stability
C. Compensates the thermal instability of integrator’s capacitor
D. A., B. answers are correct
E. A., B., C. answers are correct

2a20. Between what points is the input resistance for differential signal of differential amplifier distributed?
A. Between inputs of differential amplifier
B. Between inputs of differential amplifier and ground
C. Between one input of differential amplifier and ground
D. Between one input of differential amplifier and negative power source
E. All the answers are wrong

2a21. In what state are bipolar transistor junctions in saturation mode?
A. Emitter junction is close, collector - open
B. Emitter junction is open, collector - close

C. Both junctions are open
D. Both junctions are close
E. Saturation mode has no connection with the states of junctions

2a22. Why is not resistance applied as a stable current source in a differential amplifier?
A. Large resistances, characteristic of current source, are not possible to realize in semiconductor ICs
B. Large voltage drop is obtained on the resistance of large nominal which leads to the increase of power supply voltage value
C. The resistance cannot be current source at all
D. A., B. answers are wrong
E. All the answers are wrong

2a23. What is the function of the output cascade of OpAmp?
A. Current amplifier
B. Power amplifier
C. Provides small output resistance
D. B., C. answers are correct
E. All the answers are wrong

2a24. Why are the minimum values of output signals of differential amplifier for small signal application limited by approximately - 0.7V level with bipolar transistors?
A. Due to one of transistors falling into saturation mode
B. Due to one of transistors collector opening
C. Due to closing of one of transistors
D. A., B. answers are correct
E. Due to value limitation of collector resistance

2a25. What should the structure of a MOS transistor look like to reduce body effect?
A. Square of the bulk diffusion must be large
B. Bulk diffusion must be rounded over transistor
C. Bulk diffusion must be as close to the transistor as possible
D. A and C answers are correct
E. B and C answers are correct

2a26. What signals are the switching capacitances controlled by?
A. Overlap clock signals
B. Clock signals
C. Multi-level clock signals
D. Non overlap clock signals
E. Non clock signals

2a27. Which ADC is basically the fastest?
A. Sigma-delta
B. Dual slope integrating AC
C. SAR
D. Integrating
E. Pipeline

2a28. How can the channel modulation effect of a MOS transistor be reduced?
A. By decreasing bulk potential
B. By decreasing transistor's L
C. By decreasing transistor's W
D. By increasing transistor's W
E. By increasing transistor's L

2a29. How much is the NMOS source follower output voltage when the input transistor is in saturation mode?
A. Equal to supply voltage
B. Equal to zero
C. Larger than input voltage by threshold voltage of an input transistor
D. Smaller than input voltage by threshold voltage of an input transistor
E. Equal to input voltage

2a30. What is the advantage of using a field transistor in the input of DiffAmp?
A. Input capacitance decreases
B. Input resistance increases
C. Input offset error decreases
D. Has no advantage
E. A, B and C answers are correct

2a31. Which of the listed ADC contains DAC?
A. SAR
B. Flash
C. Integrating
D. Dual slope integrating
E. All the answers are correct

2a32. By what element is channel modulation of a MOS transistor presented in a small signal model?
A. Controlled voltage source
B. Resistance
C. Controlled current source
D. Capacitor
E. RC circuit

2a33. The effect of what errors reduces ADC's digital correction application in a pipeline?
A. Errors depending on gain of OpAmp
B. Errors depending on capacitor values scaling
C. Comparators offset error
D. Comparators sensitivity

E. C and D answers are correct

2a34. Which of the mentioned DAC is not used in ICs?

A. R-string DAC
B. R-2R DAC
C. Charge scaling DAC
D. Current DAC
E. All are used

2a35. What is the IC lifetime conditioned by?

A. Supply voltage value
B. Migration
C. Leakage power
D. Maximum clock frequency of IC
E. All the answers are correct

2a36. By what element is the body effect of a MOS transistor presented in a small signal model?

A. Controlled voltage source
B. Resistance
C. Controlled current source
D. Capacitor
E. RC circuit

2a37. What is the minimum value of OpAmp's negative feedback limited by?

A. Input resistance of OpAmp
B. Amplifying coefficient of OpAmp
C. Minimum value of OpAmp's output load resistance
D. A=1 value
E. Minimum value of OpAmp's input current

2a38. What is the reason of differential amplifier's debalance?

A. Non similarity of diffpair (transistor)
B. Accuracy of current source
C. Loads non matching
D. A and B answers are correct
E. A and C answers are correct

2a39. How many comparators does an 8 bit two-stage Flash ADC contain?

A. 15
B. 30
C. 255
D. 31
E. 63

2a40. How many comparators does a single-stage 8-bit Flash analog to digital converter have?

A. 31
B. 7
C. 255
D. 63
E. 127

2a41. What is the main disadvantage of a SAR analog to digital converter?

A. Limited accuracy
B. low performance
C. A and B answers are correct
D. A, B and E answers are correct
E. Thermal instability

2a42. What is the high performance of an ADC conditioned by?

A. High performance of input switches
B. Output change rate of output operational amplifier
C. Converter's capacity
D. A, B and C answers are correct
E. A and B answers are correct

2a43. Why are differential amplifiers applied only in case of high ohmic loads?

A. Because they have two outputs
B. Because the reduction of load resistance reduces the amplification coefficient of differential signal
C. Because the reduction of load resistance leads to amplification of common-mode signal
D. B, C and D answers are correct
E. B and C answers are correct

2a44. Why are not differential amplifiers used as a standalone amplifiers?

A. Because of too high output resistance
B. Because they cannot work with low ohmic loads
C. Because amplifying of differential signal changes with load resistance
D. A, B and C answers are correct
E. A and B answers are correct

2a45. What is the body affect in a small signal model of a MOS transistor presented by?

A. Current controlled current source
B. Voltage controlled voltage source
C. Voltage controlled current source
D. Resistance
E. Current controlled voltage source

2a46. By what is channel length modulation in a small signal model of a MOS transistor presented?

A. Current controlled current source
B. Voltage source
C. Capacitor
D. Resistor
E. Current controlled voltage source

2a47. What is the body effect of a MOS transistor conditioned by?

A. Potentials' difference of source and drain

B. Potentials' difference of source and gate

C. Potentials' difference of drain and substrate

D. Potentials' difference of gate and substrate

E. Potentials' difference of source and substrate

2a48. What is the channel length modulation of a MOS transistor conditioned by?

A. Potentials' difference of source and drain

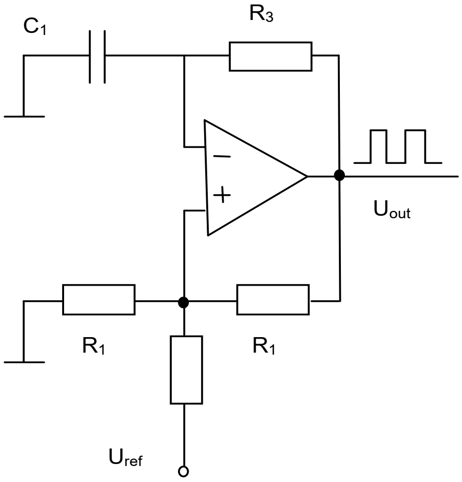
B. Potentials' difference of source and gate

C. Potentials' difference of drain and substrate

D. Potentials' difference of gate and substrate

E. Potentials' difference of source and substrate

2a49. How will the change of R1 affect this generator?



A. Output amplitude will change

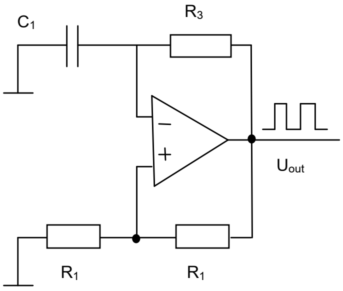
B. Output frequency will change

C. Amplitude at point A will change

D. Frequency at point A will change

E. All the answers are wrong

2a50. How will R1 change affect this generator?



A. The amplitude of output pulses will change

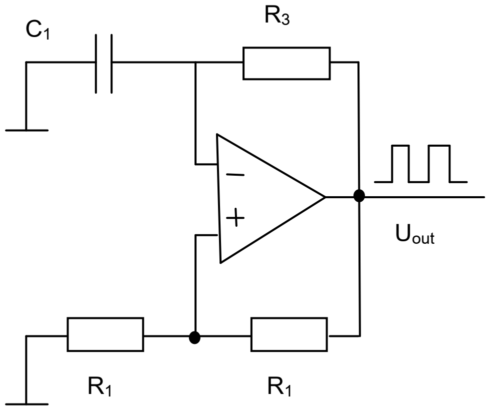
B. The frequency of output pulses will change

C. The amplitude of A point pulses will change

D. The frequency of A point pulses will change

E. B, C and D answers are correct

2a51. The change of which element of this generator will lead to the change of frequency of output signal?



A. R_2

B. R_3

C. C_1

D. B and C answers are correct

E. A, B and C answers are correct

2a52. Between which pins of a MOS transistor there is no direct capacitance?

A. Source and gate

B. Drain and gate

C. Gate and substrate

D. Source and substrate

E. Source and drain

2a53. How can the conductance of a MOS transistor change in case of the given technology and gate source voltage (ignore secondary effects)?

A. Change in gate drain voltage of a transistor

B. Change in drain source voltage of a transistor

C. Change in the sizes of channel

D. Not possible to change

E. Change in the sizes of source and drain

2a54. What does the FET transistor in saturation mode represent?

A. Current source

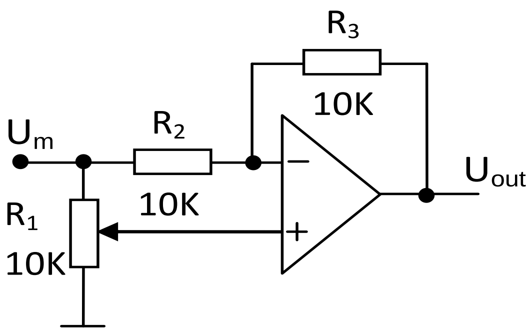
B. Voltage source

C. Linear resistance

D. Resistance

E. Infinite small resistance

2a55. Within what limitations will U_{output} voltage change when moving control of R_1 potentiometer form min position to max position?



A. From U_m to $2U_m$
B. From $–U_m$- to $-2U_m$
C. From $–2U_m$ to U_m
D. From $–U_m$- to U_m
E. From $–U_m$- to $2U_m$

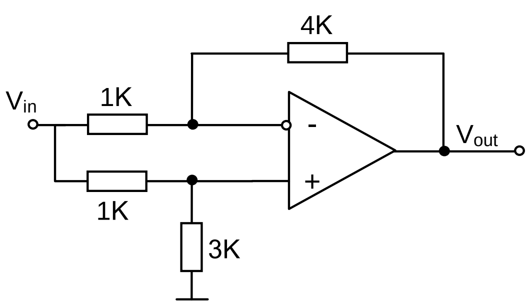
2a56. What is the accuracy of a digital-analog converter with R-2R matrix conditioned by?

A. Accuracy of making matrix resistors
B. Value of voltage offset error of output OpAmp
C. Gain of output OpAmp
D. A and B answers are correct
E. A, B and C answers are correct

2a57. How can the amplification coefficient of a single stage common source resistive load amplifier increase?

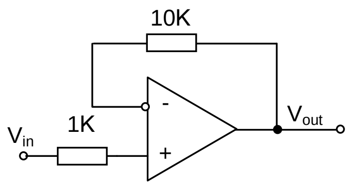
A. By increasing resistance value
B. By increasing channel width
C. By increasing channel length
D. A and B answers are correct
E. A and C answers are correct

2a58. What is the value of amplification coefficient of this amplifier?



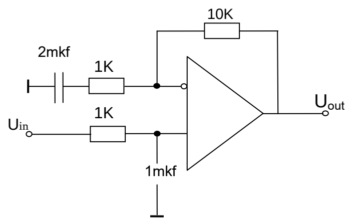
A. $K_U=10$
B. $K_U=1$
C. $K_U=-1$
D. $K_U=11$
E. $K_U=2$

2a59. What is the value of amplification coefficient of this amplifier?



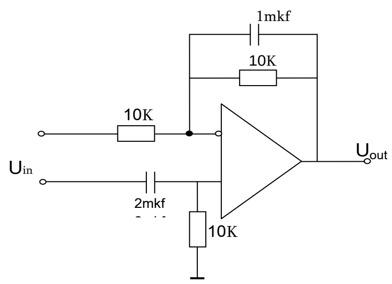
A. $K_U=0$
B. $K_U=1$
C. $K_U=11$
D. $K_U=10$
E. $K_U=2$

2a60. What function does this circuit implement?



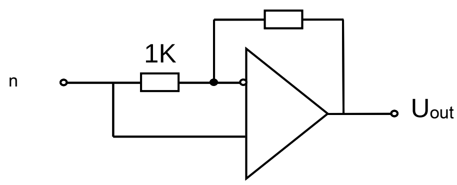
A. Low pass filter
B. Band-pass filter
C. Band-stop filter
D. Only an amplifier
E. High pass filter

2a61. What function does this circuit implement?



A. Band-pass filter
B. Low pass filter
C. Band-stop filter
D. Only an amplifier
E. High pass filter

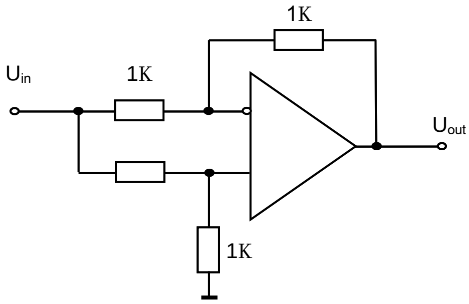
2a62. What is the value of amplification coefficient of this amplifier?



A. $K_U=-4$
B. $K_U=5$
C. $K_U=-1$

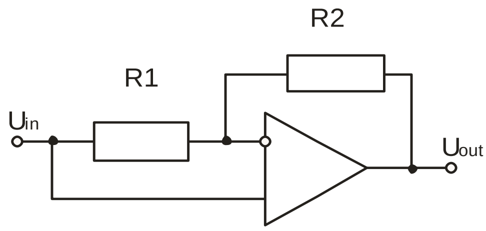
D. K_U=1
E. K_U=0

2a63. What is the value of amplification coefficient of this amplifier?



A. K_U=0
B. K_U=1
C. K_U=-1
D. K_U=-2
E. K_U=2

2a64. How will the change of R1 and R2 affect an output voltage value?



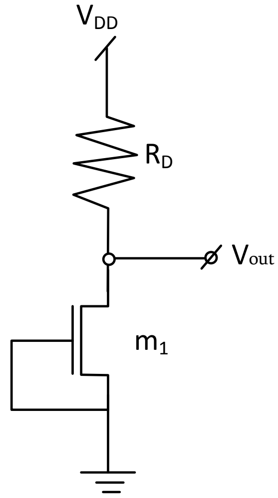
A. R1 decrease will lead to U_{out} decrease
B. R1 decrease will lead to U_{out} increase
C. R2 increase will lead to U_{out} increase
D. The change of R1 and R2 will not affect on U_{out}
E. A. B. answers are correct

2a65. What is the reason of differential amplifier's offset?
A. Non similarity of diffpair (transistor)
B. Accuracy of current source
C. Low gain
D. High gain
E. Value of phase shift

2a66. Which of the mentioned single stage amplifier has the highest amplification coefficient?
A. Common source with the resistive load
B. Common source with the current source load
C. Source follower
D. Cascode stage
E. Common gate

2a67. Which OpAmp parameter is measured with AC analysis?
A. Slew rate
B. Settling time
C. Gain margin
D. Power consumption
E. The correct answer is missing

2a68. The output voltage of the presented circuit equals:



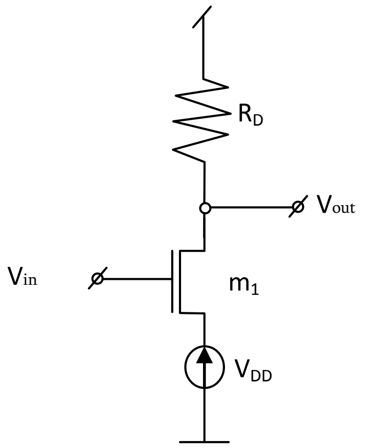
A. 0
B. vdd/2
C. v_{in}
D. vdd
E. v_{in}-v_{th}

2a69. One of the advantages of differential operation vs single-stage operation is:
A. High immunity to noise
B. Low immunity to noise
C. Possible reduction of power consumption
D. Possible reduction of area
E. Low voltage operation range

2a70. Which of the mentioned OpAmps is the fastest one (has the largest gain bandwidth)?
A. Folded cascode
B. Telescopic
C. Two-stage
D. Gain-boosted
E. All

2a71. Which OpAmp parameter is not measured with AC analysis?
A. Slew rate
B. Phase margin
C. DC gain
D. Unity gain bandwidth
E. Power supply rejection ratio

2a72. The output voltage of the presented circuit equals:



A. vin
B. vdd
C. 0
D. vdd/2
E. v_{th}

2a73. Cascode stage is the cascade connection of

A. Source follower and common gate
B. Source follower and common source
C. Common source and common gate
D. Cascade stage is not a cascade connection
E. The correct answer is missing

2a74. What is body effect in a small signal model of a MOS transistor presented by?

A. Current controlled current source
B. Voltage controlled voltage source
C. Voltage controlled current source
D. Resistor
E. Current controlled voltage source

2a75. A saturated MOS transistor can be presented as:

A. Voltage source
B. Current source
C. Resistor
D. Current controlled current source
E. Thyristor

2a76. One of the advantages of differential operation vs single-stage operation is:

A. Low immunity to noise
B. Increase of oprating voltage range
C. Possible reduction of power consumption
D. Possible reduction of area
E. Decrease of operating voltage range

2a77. Cascoded current source allows reducing the current dependence on

A. Body effect influence
B. Temperature
C. Supply voltage noise
D. Non ideality of technological process
E. Channel length modulation affect

2a78. Which of the mentioned operational amplifiers provides the maximum output voltage range?

A. Folded cascode
B. Telescopic
C. Two-stage
D. Gain-boosted
E. All

2a79. Which of the mentioned single stage amplifier has positive amplification coefficient?

A. Common source with resistive load
B. Common source with current mirror load
C. Cascode resistive load
D. Cascode current with source load
E. Common gate with resistive load

2a80. Which OpAmp parameter is measured with AC analysis?

A. Output signal slew rate
B. PSRR
C. Output signal settling time
D. Power consumption
E. None of the above

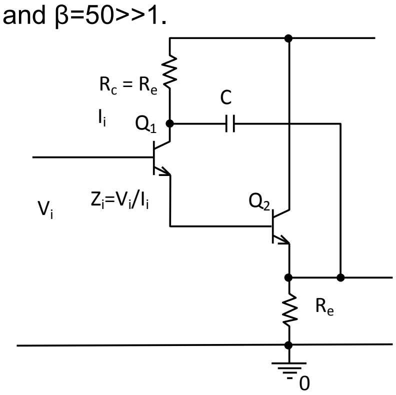
2a81. Which type of simulation is output signal settling time of OpAmp measured by?

A. Transient
B. DC
C. AC
D. FFT
E. None of the above

2a82. Calculate the maximum gain of a bipolar transistor, if early voltage is equal to 130 V.

A. 130
B. 260
C. 5000
D. 3846
E. 1300

2a83. Find input impedance ratio $Z_i(C\to\infty)/Z_i(C=0)$ if R_e=8k, h_{ie}=3k, h_{re}=0, h_{oe}=20μS, and β=50>>1.

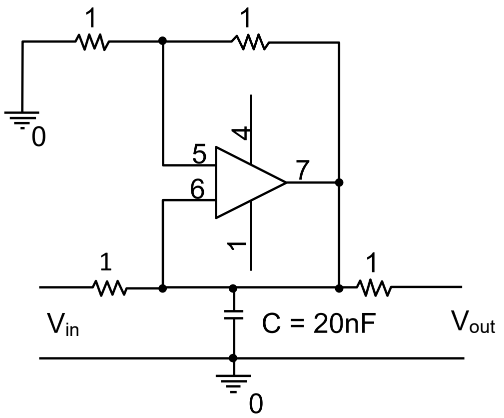


A. $Z_i(C\to\infty)/Z_i(C=0)=0.5$
B. $Z_i(C\to\infty)/Z_i(C=0)=4.05$
C. $Z_i(C\to\infty)/Z_i(C=0)=0.56$
D. $Z_i(C\to\infty)/Z_i(C=0)= 1.014$
E. $Z_i(C\to\infty)/Z_i(C=0)=2$

2a84. Find voltage drop on direct biased diode D_2 connected in serias with D_1 where voltage drop of V_{D1}=0.4V is measured. Diodes are made in same technology with area $S_1=50\cdot S_2$. Adopt kT/q=25mV.

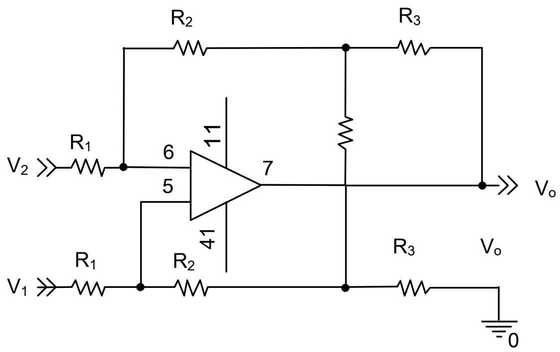
A. 0.2V
B. 0.4V
C. 0.5V
D. 0.6V
E. 0.7V

2a85. Find transfer function Vout/Vin. Assume an ideal OpAmp.



A. $s/(5\cdot 10^4)$
B. $-s/(5\cdot 10^4)$
C. $s/(5\cdot 10^5)$
D. $-s/(5\cdot 10^5)$
E. $5\cdot 10^5/s$

2a86. Assuming an ideal Opamp find R_2/R_3 that gives $A=\dfrac{V_o}{V_2-V_1}=2\dfrac{R_2}{R_1}\left(1+\dfrac{R_2}{R}\right)$



A. 1/3
B. 1/2
C. 1
D. 2
E. 3

2a87. Short-circuit power consumption is defined as:

A. *The total power consumed in a chip while the chip is partially switching*
B. *The power consumed during the signal rise and fall at which both pull-up and pull-down networks are ON*
C. *The power consumed due to leakage into the transistor gate and it is a strong function of the oxide thickness and the gate voltage*
D. *All of the above*
E. *None of the above*

2a88. The threshold voltage of a transistor is defined as:

A. *The voltage needed at the gate terminal for the channel to start conducting*
B. *A voltage barrier that need to be overcome in order for the transistor to be turned ON*
C. *The voltage required to initiate the formation of the conduction between the drain and source*
D. *All of the above*
E. *None of the above*

2a89. A transistor has three operation regions, cutoff, linear and saturation. The relationship between the gate-source voltage and the drain-source current is (considering short channel transistor):

A. *Zero in cutoff region, linear in linear region, and quadratic in saturation*
B. *Zero in cutoff region, quadratic in linear region, and linear in saturation*
C. *Exponential in cutoff region, linear in linear, and saturation regions*
D. *Zero in cutoff region, linear in linear region, and no direct relationship in the saturation region*
E. *None of the above*

2a90. Channel modulation is an empirical representation of the relationship between:

A. *The saturation current and the drain-source voltage in the saturation region*
B. *The drain-source current and the gate voltage in the linear region*
C. *The drain-source current and the drain-source voltage in the linear region*

D. The drain-source current and the change in threshold voltage in the velocity-saturation model

E. None of the above

2a91. The velocity saturation model is more accurate than the long channel model in small gate length technologies because:

A. It represents a linear relationship between the saturation current and the gate voltage

B. It uses an analytical modeling techniques as opposed to empirical models used in the long channel models

C. It includes the drain-source voltage in the saturation current model in the saturation region

D. All of the above

E. None of the above

2a92. In a short channel, velocity saturation happens because of:

A. Collisions of carriers due to high horizontal electric field

B. Mobility degradation because of high drain voltage

C. Mobility degradation because of high gate voltage

D. A. and C.

E. None of the above

2a93. Subthreshold leakage current increases (considering $V_{gs} < V_t$) if:

A. The temperature increases

B. The threshold voltage increases

C. The drain and source potential difference is less than zero

D. A. and B.

E. None of the above

2a94. The idle power (in cutoff) can be reduced by:

A. Setting lower body voltage (negative V_b) that will reduce the threshold voltage

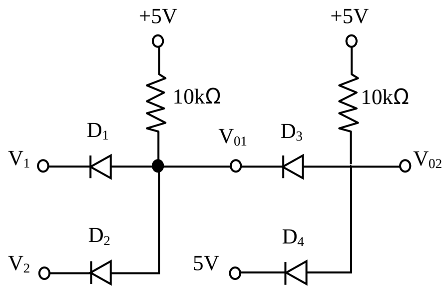
B. Increasing the source voltage that will increase the threshold voltage

C. Decreasing threshold voltage by increasing gate voltage

D. All of the above

E. None of the above

2a95. The circuit below acts like two AND gates connected together. Assume Vy=0.6V for each diode. The output of V_{O2} when V_1=5V and V_2=5V will be:



A. 0.6V

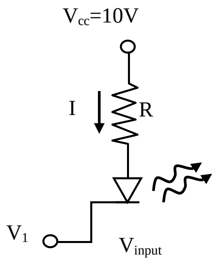
B. 1.2V

C. 5V

D. 10V

E. None of the above

2a96. The circuit below has a diode with a forward bias voltage threshold voltage of 1.2V. The value of R required to limit the current to I=12mA when V_I=0.2V should be:



A. 716.8Ohm

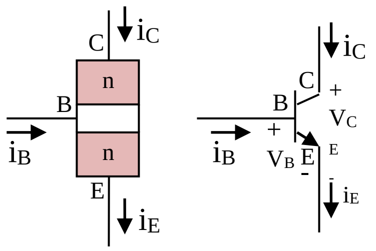
B. 816.7Ohm

C. 187.6Ohm

D. 681.7Ohm

E. None of the above

2a97. In the operation of a typical active-mode BJT transistor, as shown, the:

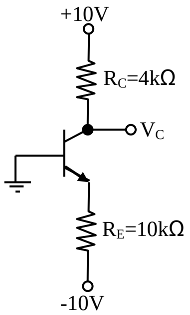


A. The B-E junction is forward biased, the B-C junction is reverse biased

B. The B-E junction is forward biased, the B-C junction is forward biased

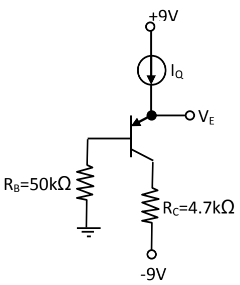
C. *The B-E junction is reverse biased, the B-C junction is reverse biased*
D. *The B-E junction is reverse biased, the B-C junction is forward biased*
E. *None of the above*

2a98. In the operation of a typical active-mode BJT transistor, the topology opposite is:



A. *A common-base connection*
B. *A common-emitter connection*
C. *A common-collector connection*
D. *A common-base and common-emitter connection*
E. *None of the above*

2a99. In the circuit, a p-n-p transistor is used, if I_Q=1mA and β=50, the value of the V_c (collector voltage) will be:



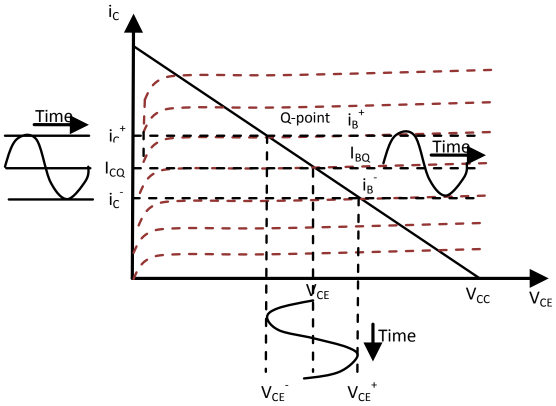
A. *+2.2V*
B. *+11.7V*
C. *-19.0V*
D. *-4.39V*
E. *None of the above*

2a100. In small signal AC analysis of BJT circuits, we:

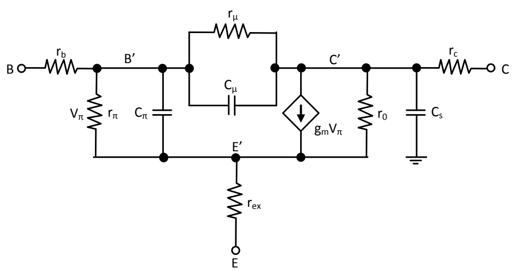
A. *Set all AC sources to ground*
B. *Set all DC sources to ground*
C. *Remove all sources*
D. *Remove all grounds*
E. *None of the above*

2a101. In load line analysis of small signal AC BJT amplifier circuits, the Q-point bias is said to be desired round the centre of the DC VCE-IC curves, because?

A. *Easier to calculate values of biasing resistors*
B. *Improves the DC performance of the circuit*
C. *Improves the linearity of the circuits by avoiding distortion*
D. *Enhances distortion and non-linearity, which are desired objectives in small-signal amplifiers*
E. *None of the above*



2a102.
In the hybrid high frequency model of a transistor, Miller capacitance:



A. *Will improve the frequency response of the amplifier by increasing the bandwidth*
B. *Has no effect on frequency*
C. *Will reduce the frequency bandwidth of an amplifier*
D. *Will increase the value of* C_π
E. *None of the above*

2a103. Consider an n-channel MOSFET with K_n'=100μA/V^2, V_{tn} = 1V and W/L=10. Find the drain current when V_{GS} = 0 and V_{DS} = 5V.

A. *3.5 mA*
B. *0*
C. *3.0 mA*
D. *4.5 mA*
E. *None of the above*

2a104. What is the way to reduce dependence of the saturation current change of MOS transistor from the channel length modulation?

A. Decreasing channel length
B. Increasing channel length
C. Decreasing channel width
D. Increasing channel width
E. Increasing substrate voltage

2a105. The amplification coefficient of which amplifier is basically the greatest?

A. Common source with current source load
B. Source follower with resistive load
C. Common gate with current source load
D. Common source with resistive load
E. Common gate with resistive load

2a106. What type of load ensures greatest amplification coefficient of a MOS transistor based amplifier?

A. Resistive
B. Diode connected
C. Triode mode
D. Current source
E. Cutoff mode

2a107. The operating domain of output voltage of which amplifier is basically the greatest?

A. Common source with current source load
B. Cascode with resistive load
C. Common gate with current source load
D. Common source with resistive load
E. Common gate with resistive load

2a108. How does the output common mode voltage of a differential amplifier depend on the input common mode voltage?

A. Direct
B. Inverse
C. Does not depend
D. $(V_{out}/V_{in})_{cm}=g_m R_D$
E. Equal

2a109. How will the output common mode voltage of a differential amplifier with n-MOS input change if tail current increases (I_{ss})?

A. Will decrease
B. Will increase
C. Will not change
D. The output common mode voltage of a differential amplifier does not depend on tail current (I_{ss})
E. Will increase 3 times

2a110. Which parameter of an OpAmp is measured with AC analysis?

A. Slew rate
B. Power supply rejection ratio
C. Settling time
D. Power consumption
E. Offset error

2a111. Which parameter of an OpAmp is measured with transient analysis?

A. Gain bandwidth
B. Power supply rejection ratio
C. Settling time
D. Unity gain bandwidth
E. Phase margin

2a112. With which analysis does the gain bandwidth of an OpAmp measured?

A. Transient
B. DC
C. AC
D. FFT
E. The correct answer is missing

2a113. Which OpAmp-based circuit has hysteresis transfer characteristics?

A. Positive feedback comparator
B. Integrator
C. Comparator without feedback
D. Non-inverting amplifier
E. Inverting amplifier

2a114. What else is an active integrator?

A. High pass filter
B. Low pass filter
C. Differentiator
D. Bandpass filter
E. Nothing

2a115. What else is a differentiator?

A. High pass filter
B. Low pass filter
C. Integrator
D. Bandpass filter
E. Nothing

2a116. Which ADC is basically the fastest?

A. Pipeline
B. Sigma-delta
C. Integrating
D. Flash
E. SAR

2a117. Which ADC has basically the highest bit?

A. Pipeline
B. Sigma-delta
C. Integrating

D. *Flash*
E. *SAR*

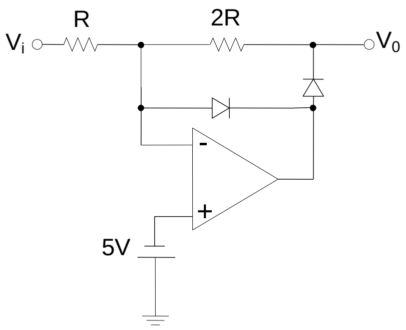
2a118. In what ADC structure there is DAC?

A. *Dual integrating*
B. *Sigma-delta*
C. *Integrating*
D. *Flash*
E. *SAR*

2a119. Which DAC is basically the fastest?

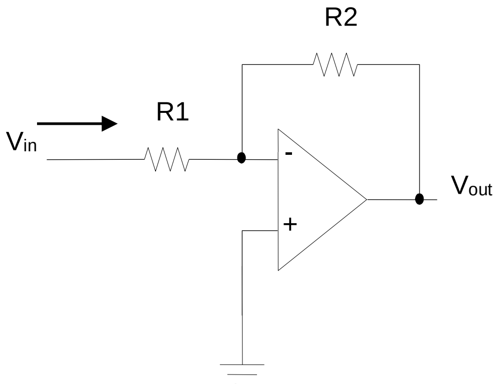
A. *R-string*
B. *R-2R*
C. *Pipeline*
D. *Current steering*
E. *Charge scaling*

2a120. For the OpAmp circuit shown below, what is the value of V_0 when V_i = 0V? The OpAmp and diodes are ideal.



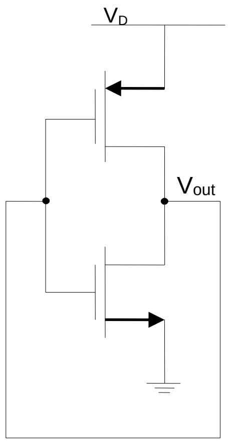
A. *+5V*
B. *-5V*
C. *0V*
D. *-15V*
E. *+15V*

2a121. The circuit shown below uses an ideal OpAmp. The input resistance is:



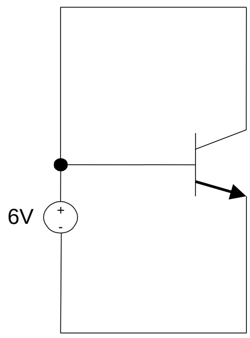
A. *0*
B. *Infinite*
C. *R1*
D. *R2*
E. *R1 + R2*

2a122. The circuit shown below acts as:



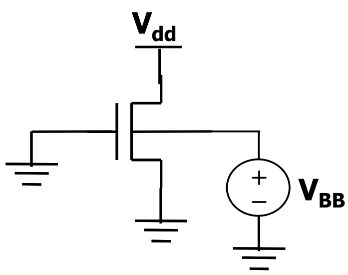
A. *Ring oscillator*
B. *Reference voltage generator*
C. *Bistable multivibrator*
D. *A stable multivibrator*
E. *None of the above*

2a123. The region of operation for the transistor shown in the circuit below is:



A. *Saturation*
B. *Reverse active*
C. *Forward active*
D. *Cutoff*
E. *Reverse saturation*

2a124. Consider the following transistor which is in the off condition (V_{gs}=0<V_t=0.2 and V_{dd}=1V). Assume subthreshold and junction leakage components are both considerable.

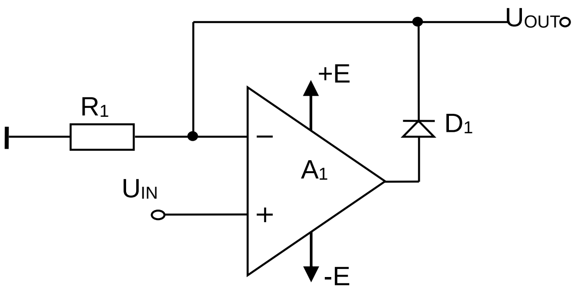


Compared to the case when V_{BB}=0 V, by applying negative V_{BB}:

A. *Both subthreshold and junction leakage decrease*
B. *Both subthrehsold and junction leakage increase*

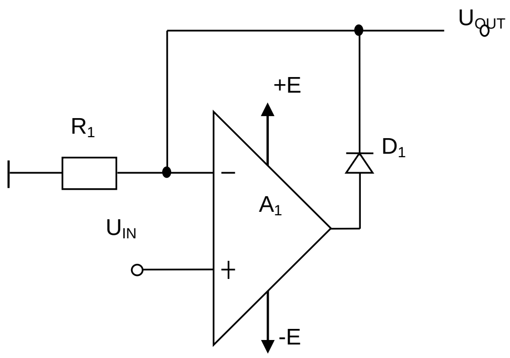
C. Subthreshold leakage increases and junction leakage decreases
D. Subthresold leakage decreases and junction leakage increases
E. Subthreshold leakage decreases and junction leakage does not change

2a125. What function does this circuit implement if U_{IN} is a variable bipolar signal, and A_1 – ideal OpAmp using bipolar power supply?



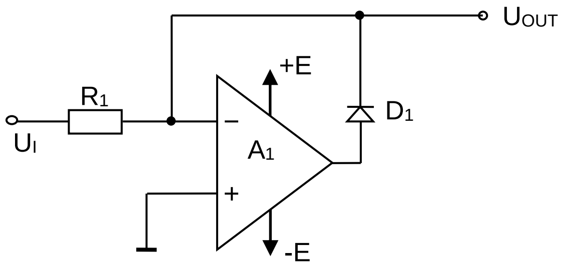
A. Half-wave rectifier output positive signal
B. Full-wave rectifier output positive signal
C. Full-wave rectifier output negative signal
D. Half-wave rectifier output negative signal
E. Logarithmic amplifier

2a126. What function does this circuit implement if U_{IN} is a variable bipolar signal, and A_1 – ideal OpAmp using bipolar power supply?



A. Repeater in open state of a diode
B. Comparator in close state of a diode
C. A. and B.
D. Non-inverse amplifier
E. Amplifier with logarithmic transfer function

2a127. What values can U_{OUT} of this circuit have if U_{IN} is a variable bipolar signal, and A_1 – ideal OpAmp using bipolar power supply?



A. Repeat positive values of U_{IN}
B. Repeat negative values of U_{IN}
C. $U_{OUT} = 0$, if $U_{IN} > 0$
D. $U_{OUT} = 0$, if $U_{IN} < 0$
E. A. and D.

2a128. How will the output signal polarity change if U_{IN} variable signal is given not to negative input of OpAmp (Fig.1), but non-inverting (Fig.2) (A_1 – ideal OpAmp using bipolar power supply).

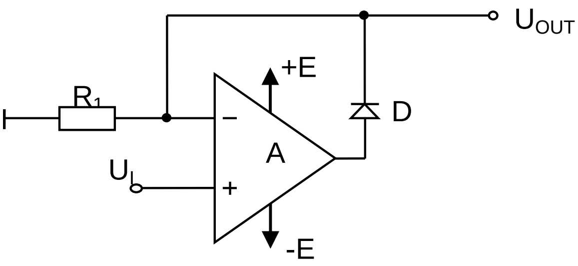


Fig.1

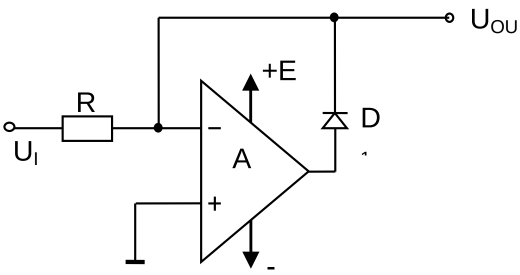
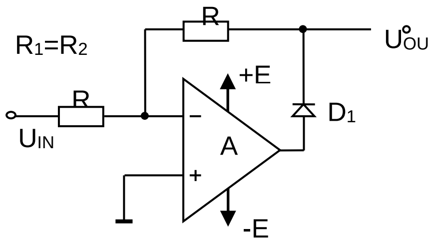


Fig. 2

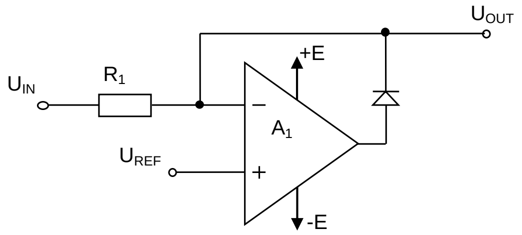
A. Will not change
B. Will change
C. Will not change if feedback diode will reverse
D. Will change if feedback diode will reverse
E. A. and C.

2a129. What function does this circuit implement if U_{IN} is a variable bipolar signal, R1=R2, and A_1 – ideal OpAmp using bipolar power supply?



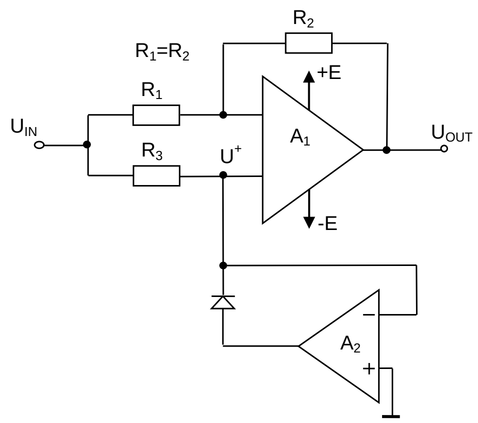
A. *Half-wave inverting rectifier*
B. *Full-wave inverting rectifier*
C. *Half-wave non-inverting rectifier*
D. *Full-wave non-inverting rectifier*
E. *Inverting follower*

2a130. What function does this circuit implement if U_{IN} is a variable bipolar signal, and A_1 – ideal OpAmp using bipolar power supply?



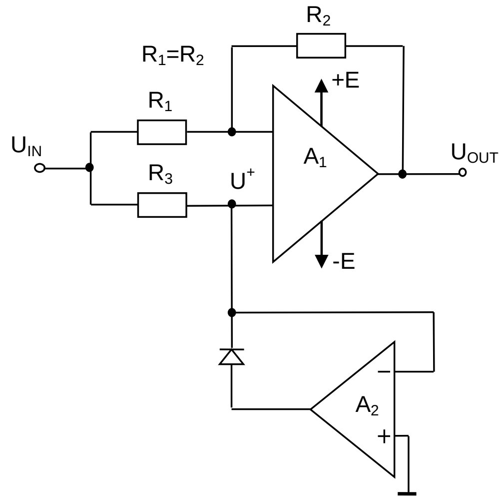
A. *Limiting U_{IN} signal top value by U_{REF} level*
B. *Limiting U_{IN} signal bottom value by U_{REF} level*
C. *Limiting U_{IN} signal top value by ($-U_{REF}$) level*
D. *Limiting U_{IN} signal bottom value by ($-U_{REF}$) level*
E. *Logarithmic substractor between U_{IN} and constant U_{REF}*

2a131. What values can U_{0UT} of this circuit have if U_{IN} is a variable bipolar signal, R1=R2, and A_1 and A_2 – ideal OpAmp using bipolar power supply?



A. *$U_{0UT} = -U_{IN}$, if $U_{IN} > 0$*
B. *$U_{0UT} = U_{IN}$, if $U_{IN} > 0$*
C. *$U_{0UT} = -U_{IN}$, if $U_{IN} < 0$*
D. *$U_{0UT} = U_{IN}$, if $U_{IN} < 0$*
E. *B. and D.*

2a132. What values does positive input of A_1 OpAmp (U^+_1) voltage in case of positive and negative values of U_{IN} input voltage?



A. U^+_1 *= 0, if $U_{IN} > 0$*
B. U^+_1 *= U_{IN}, if $U_{IN} > 0$*
C. U^+_1 *= 0, if $U_{IN} < 0$*
D. U^+_1 *= U_{IN} , if $U_{IN} > 0$*
E. *B. and C.*

2a133. How many comparators are there in 1 stage of 1.5 bit/stage structure of pipeline ADC?
A. *1*
B. *4*
C. *5*
D. *2*
E. *8*

2a134. How many OpAmps are there in in 12 bit 2.5 bit/stage structure of pipeline ADC?
A. 12
B. 24
C. 10
D. 11
E. 22

2a135. How many main models of ESD are there?
A. 2
B. 3
C. 5
D. 4
E. 8

2a136. Which of the mentioned single stage amplifier has no higher than 1 amplification coefficient?
A. *Common gate*
B. *Common source*
C. *Common drain*
D. *Cascode*
E. *Folded cascade*

2a137. What type of load ensures greatest amplification coefficient of a single stage amplifier?

A. Diode
B. Resistive
C. Current source
D. Triode
E. None of the above

2a138. How does the resistance, connected to the output of an amplifier, affect amplification coefficient?

A. Increases
B. Decreases
C. Does not affect
D. Possible to both increase and decrease
E. *None of the above*

2a139. Theoretically what does the minimal source-drain overdrive voltage of a MOS transistor depend on?

A. Transistor dimensions
B. Threshold voltage
C. Drain current
D. A and B
E. None of the above

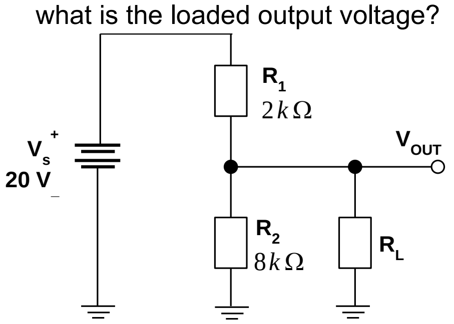
2a140. What load is used to modify the differential signal into single-ended signal?

A. Resistive
B. Active current mirror
C. Diode
D. Current source
E. None of the above

2a141. Which resistive component is designed to be temperature sensitive?

A. Thermistor
B. Rheostat
C. Potentiometer
D. Photoconductive
E. None of the above

2a142. If the R_L in the given circuit is 120 KΩ, what is the loaded output voltage?

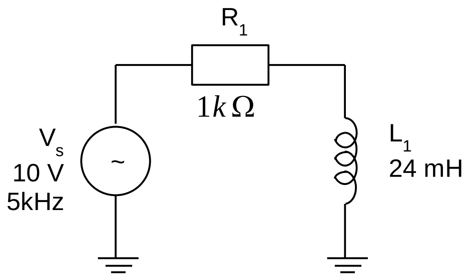


A. 4.21 V
B. 15.79 V
C. 16 V
D. 19.67 V
E. None of the above

2a143. The ____ of a capacitor affects the time it takes to charge and discharge.

A. Package style
B. Lead arrangement
C. Plate area
D. Voltage rating
E. None of the above

2a144. The voltage dropped across the resistor in the circuit in the given circuit is approximately equal to:



A. 5 V
B. 10 V
C. 7.98 V
D. 6.02 V
E. None of the above

2a145. What is the impedance of the circuit in the given circuit?

A. 125.7 Ω
B. 297.6 Ω
C. 370.1Ω
D. 423.3 Ω
E. None of the above

2a146 . If a periodic pulse waveform is applied to an RC differentiating circuit, which two conditions are possible?

A. $t_W \geq 5\tau$ or $t_W \geq 5\tau$
B. $t_W = 5\tau$ or $t_W > 5\tau$
C. $t_W \leq 5\tau$ or $t_W < 5\tau$
D. $t_W \geq 5\tau$ or $t_W < 5\tau$
E. None of the above

2a147. The voltage produced by a thermocouple is called:

A. Hot junction voltage
B. Cold junction voltage
C. Hooke voltage
D. None of the above
E. Seebeck voltage

2a148. If the frequency of a ration wave is increase, its wavelength will:

A. Increase
B. Decrease
C. Remain the same
D. Cannot tell
E. None of the above

2a149. A peak current of 12.5 mA is equivalent to:

A. An RMS value of 25 mA
B. An average value of 12.5 mA
C. A peak-to-peak value of 6.25 mA
D. An average value of 7.96 mA
E. None of the above

2a150. An ideal op-amp has very:

A. High voltage gain
B. High input impedance
C. Low input impedance
D. All of the above
E. None of the above

2a151. What is special for common source stage with source degeneration?

A. Gain versus output voltage common mode value is more linear
B. Gain is larger
C. The effect of output load to circuit performance is less
D. The effect of output load to circuit performance is more
E. Nothing special

2a152. What is the goal of common mode feedback in OpAmps?

A. To increase common mode gain
B. To decrease common mode gain
C. To compensate Phase Margin
D. To bring OpAmp parameters versus common mode value more linear
E. To bring OpAmp parameters versus differantial siganl value more linear

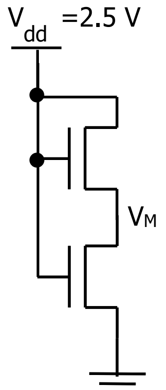
2a153. What is the accuracy of 4 bit digital-to-analog (DAC) and analog-to-digital (ADC) converters, used in two-step Flash analog-to-digital converter (ADC)?

A. Accuracy corresponds to a 4 bit converter
B. DAC – accuracy corresponds to 8 bit, and ADC – accuracy corresponds to 4 bit
C. Accuracy corresponds to 8 bit converters
D. Accuracy does not matter
E. DAC – accuracy corresponds to 4 bit, and ADC – accuracy corresponds to 8 stage

2a154. Is it necessary to perform amplitude-frequency characteristic compensation of OpAmp if it operates as a comparator?

A. Yes, amplitude-frequency characteristic compensation of OpAmp is necessary
B. No, because negative feedback is missing in comparator mode
C. B. and D. are correct
D. Comparator function will also be performed with amplitude-frequency characteristic compensation
E. Yes, if positive feedback is given to OpAmp

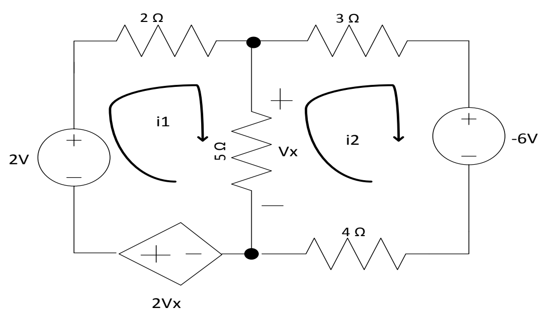
2a155. Consider the following circuit. Assume the threshold voltage of the transistor is 0.5 V. What best describes the possible voltage for the intermediate node (VM)? Assume both transistors have the same size and their body terminals are both connected to ground.



A. $1.25 < V_M < 2.5$
B. $1.25 < V_M < 2$
C. $2 < V_M < 2.5$
D. $0 < V_M < 1.25$
E. $V_M = 2$

2a156. For the circuit configuration in the figure, what is the value of i2?

A. 6/11
B. -8/11
C. 8/11
D. -6/11
E. 11/11



2a157. How will the decrease of RD load resistor, connected in drain circuit of a MOS amplifier by Common Source, affect the FMAX maximum frequency value of amplification?

A. F_{MAX} will not change
B. F_{MAX} will decrease due to decrease of gain coefficient
C. F_{MAX} will increase due to decrease of output resistance of an amplifier
D. F_{MAX} will increase due to decrease of input capacitance of an amplifier
E. C. and D. are correct

2a158. How are the amplification properties of variable signal of a MOS amplifier by Common Source, different from the one of respective bipolar transistor?

A. Their $A_m = - g_m * R_d$ small signal gain coefficients are equal
B. The gain coefficient is larger due to the lack of Miller's effect in MOS option
C. The gain coefficient is smaller due to the lack of Miller's effect in MOS option
D. The gain coefficient is larger due to g_m – small slope of input characteristics of bipolar transistor
E. The gain coefficient is smaller due to g_m – large slope of input characteristics of bipolar transistor

2a159. How much should the input resistance of I/O device be?

A. 50 Ohm
B. 100 Ohm
C. Larger than wave resistance of a wire
D. Equal to wave resistance of a wire
E. Smaller than wave resistance of a wire

2a160. Which is the function of DLL device?

A. Getting clock signals with stable delay towards each other
B. Controlling the delay of clock signal
C. Increasing the clock signal frequency
D. Decreasing the clock signal frequency
E. Creating clock signal

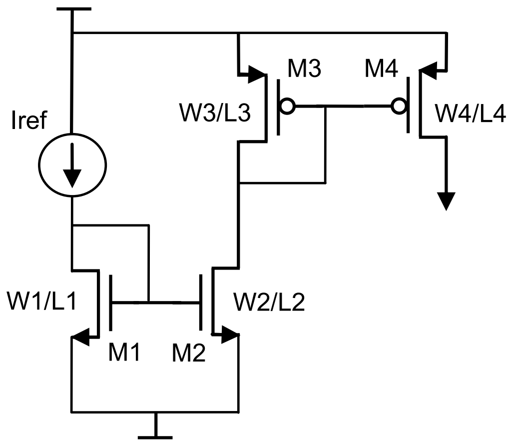
2a161. From what does the reference voltage generator receive stable voltage?

A. Only from temperature
B. Only from supply voltage value
C. From temperature and supply voltage value
D. Technological process deviations
E. The reference voltage generator does not receive stable voltage

b) Problems

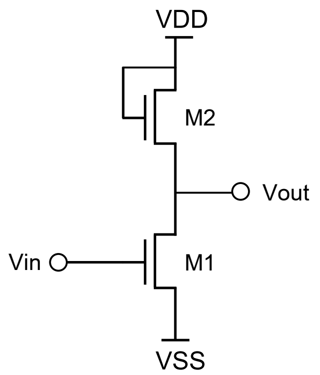
2b1.

For the following circuit find $I_{D4}=f(I_{ref})$ dependence if $\lambda=0$, $L_1=L_2=L_3=L_4$, $W_1=W_2$, $W_3=W_4$. Note that all the transistors are in saturation mode.



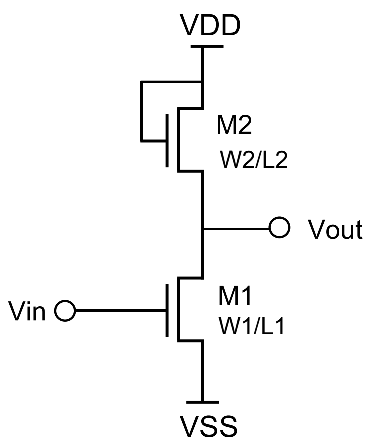
2b2.

For the following circuit define small signal gain constant (assume M1 is saturated and $\lambda=0$, $\gamma=0$).



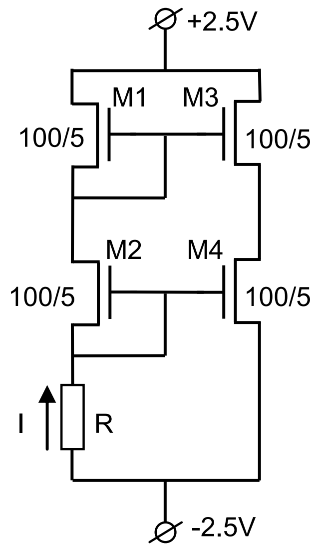
2b3.

For the following circuit define the value of input voltage in case of which M1 is out of saturation mode if $(W/L)_1=49$ $(W/L)_2=9$ $V_{TH}=0.7$ VDD=3, $\lambda=\gamma=0$.



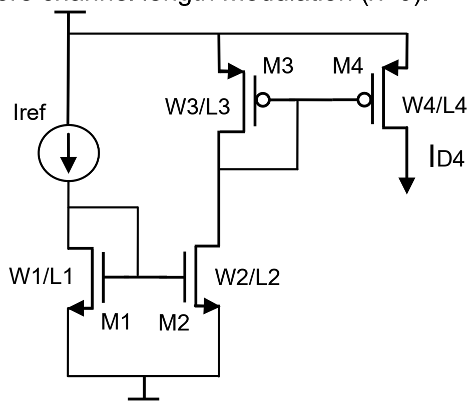
2b4.

A current mirror is given by transistors' geometrical sizes. Find the gate voltage of M1 transistor.



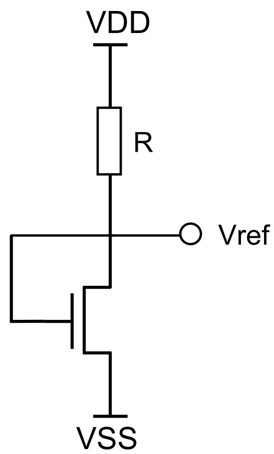
2b5.

For the following circuit find the drain current of M4 transistor if all the transistors are in saturation. Ignore channel length modulation ($\lambda=0$).

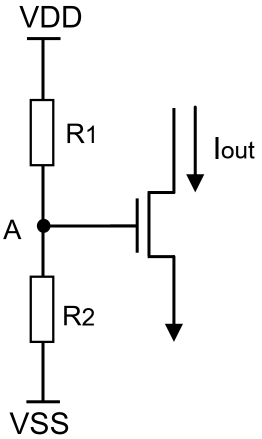


2b6.

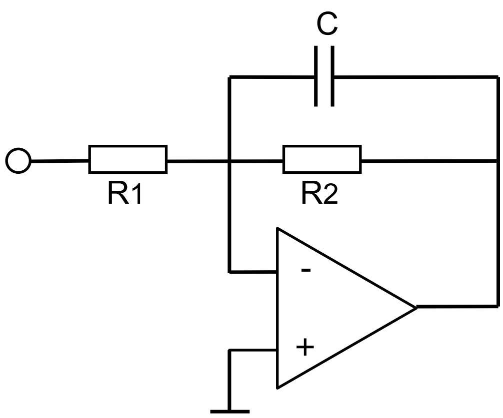
For the following circuit find V_{ref}, if $\mu_n=550\ cm^2/Vs$, $\varepsilon_{Si02}=3.9$, $\varepsilon_0=8.85*10^{-14}$ F/cm, $t_{ox}=0.16$ nm, $V_{thn}=0.8V$, $V_{DD}=2V$, $V_{SS}=0V$, W=L=10 um, $\lambda=0$, R=10 kOhm.



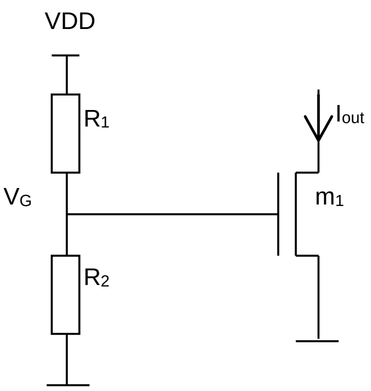
2b7.
For the following circuit define how much I_{out} will change if V_{DD} changes by $\pm 10\%$ and if the transistor is in saturation and W=50um, L=0.5um, I_{out}=0.5mA, K_n=120 uA/V^2, V_{TH}=0.5V VDD=3V, (nominal value), R_2/R_1=0.35, λ=0.



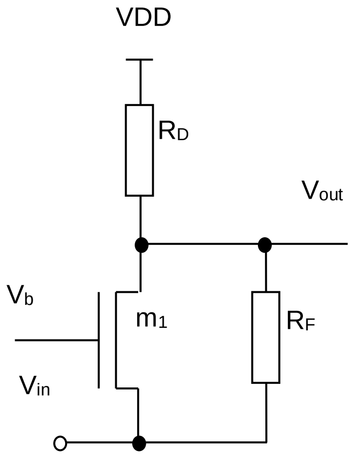
2b8.
Find the cutoff frequency of the following circuit and build amplitude-frequency characteristics, if R_1, R_2 and C are known.



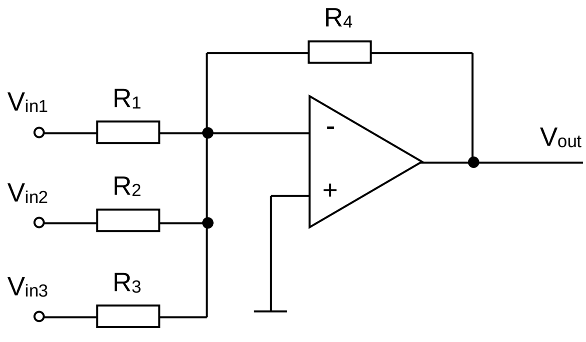
2b9.
What does I_{out} equal to when the transistor is in saturation (express transistor's conductivity by g_m). Ignore body effect and channel modulation.



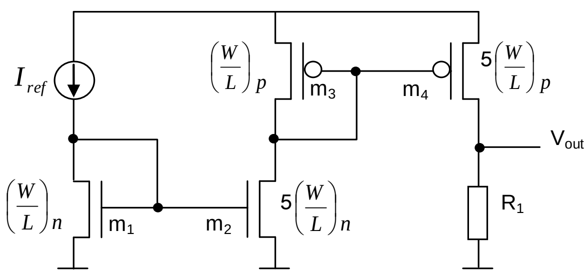
2b10.
Find V_{out} depending on V_{in}, if the transistor is in saturation. Ignore body effect and channel modulation.



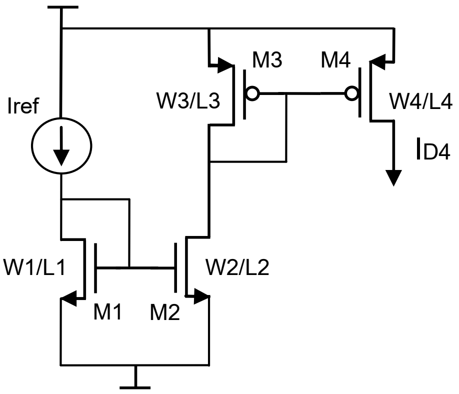
2b11.
R1, R2, R3, R4 resistances are given. Find $V_{out} = f(V_{in1}, V_{in2}, V_{in3})$, considering the real K_A amplifying coefficient.



2b12.
$\left(\frac{W}{L}\right)_n$, $\left(\frac{W}{L}\right)_p$, I_{ref}, R_1 values are given. Find V_{out}, ignore channel modulation.

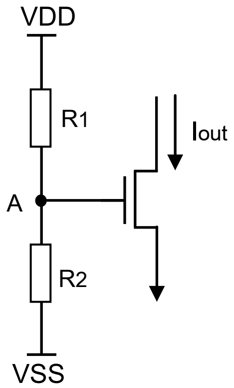


2b13.
For the following circuit find the $I_{D4}=f(I_{ref})$ dependence, if λ=0, $L_1=L_2=L_3=L_4$, $W_1=W_2=3W_3=6W_4$. All the transistors are saturated.



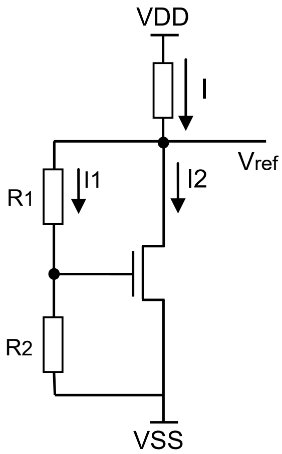
2b14.

Calculate how much will I_{out} change if VDD increases by 10%: Given W, L, μ_n, V_{TH}, C_{OX}, R_2, R_1. The transistor is saturated. Ignore secondary effects.



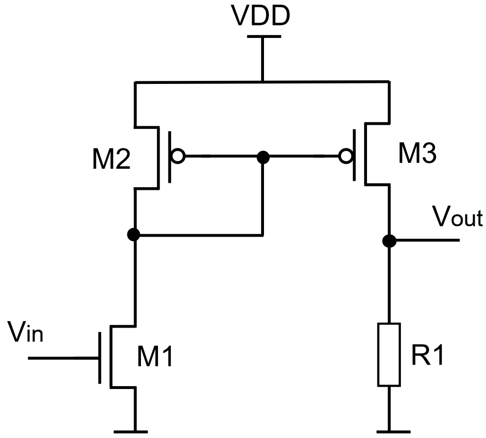
2b15.

Calculate the value of R if M1 transistor is saturated and VDD, Vref, V_{TH}, β, R_1, R_2, λ=0 are given.



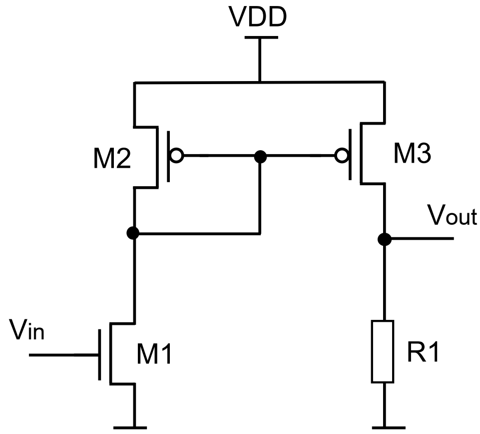
2b16.

Find $k = \frac{dV_{out}}{dV_{in}}$ coefficent (by variable component). Given $g_{m1}, g_{m2}, g_{m3}, R$.



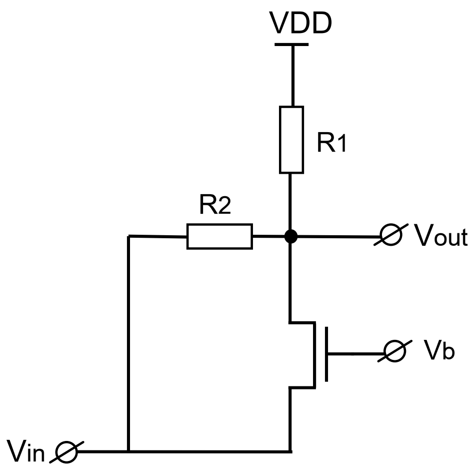
2b17.

Find A_v=dV_{out}/dV_{in} small signal gain: g_{m1}, g_{m2}, g_{m3}, R_1 values are known. Ignore secondary effects.



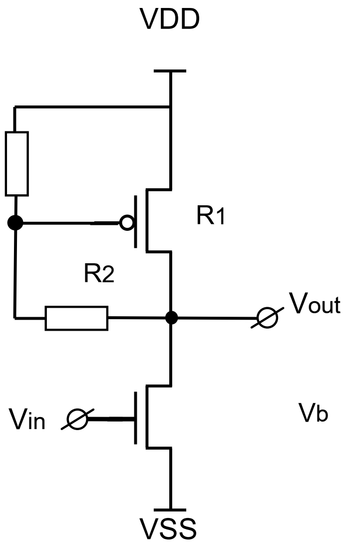
2b18.

Find A_v=dV_{out}/dV_{in} small signal gain: g_{m1},g_{mb1}, R_1, R_2 values are known. Ignore channel length modulation.

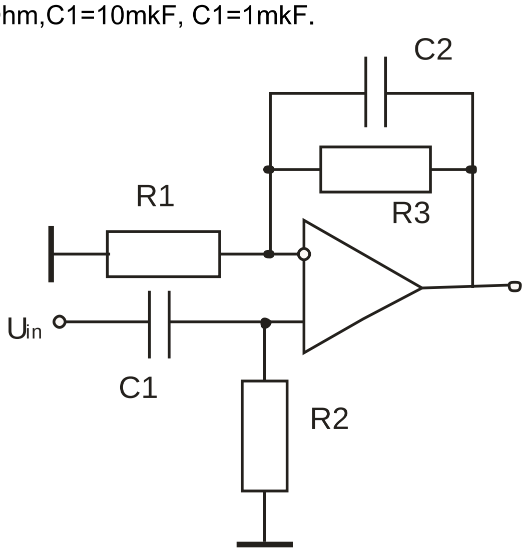


2b19.

Sketch V_{out} versus V_{in} as V_{in} varies from 0 to VDD. Identify the important transition points.



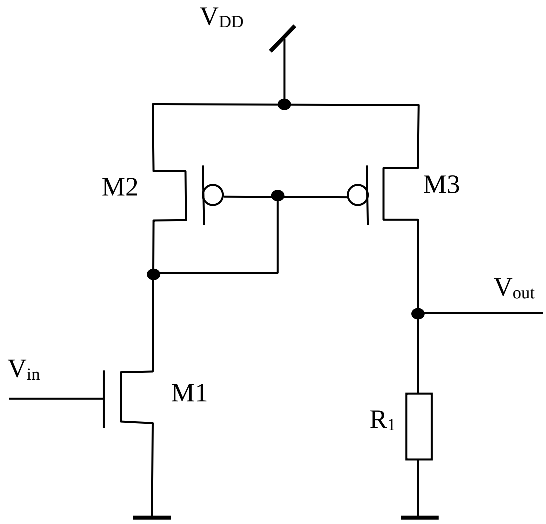
2b20.
Calculate the maximum gain and central frequency of the filter based on OpAmp if R1=1kOhm, R2=2 kOhm, R3=10 kOhm,C1=10mkF, C1=1mkF.



2b21.
The sequence $x(n)=\cos(\pi n/4)$ is a result of $u(t)=\cos\left(2\pi f_0 t\right)$ analog signal sampling with sampling frequency f_s=1000 Hz: $x(n)=u(n\Delta t)$ where $\Delta t=1/f_s$. Find two minimum f_0 values for which it takes place.

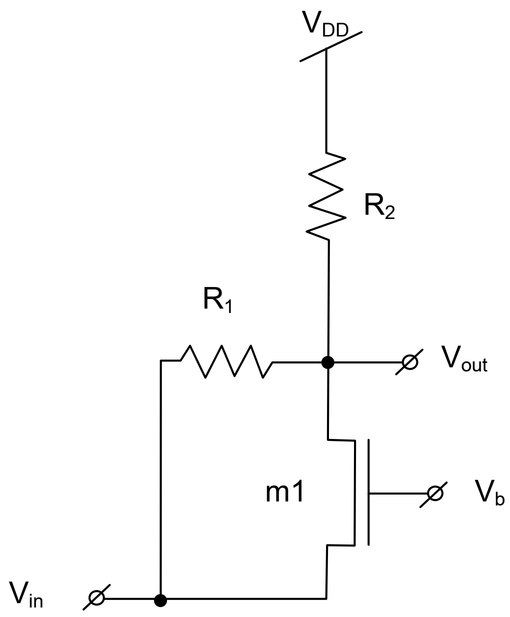
2b22.
The sequence $x(n)=\cos(\pi n/4)$ is a result of $u(t)=\cos\left(2\pi f_0 t\right)$ analog signal sampling with sampling frequency f_s=800 Hz: $x(n)=u(n\Delta t)$, where $\Delta t=1/f_s$. Find two minimum f_0>200 Hz values for which it takes place.

2b23.
Find $A_v=dV_{out}/dV_{in}$ small signal gain. g_{m1}, g_{m2}, g_{m3}, r_{01}, r_{02}, r_{03}, R_1 values are known.

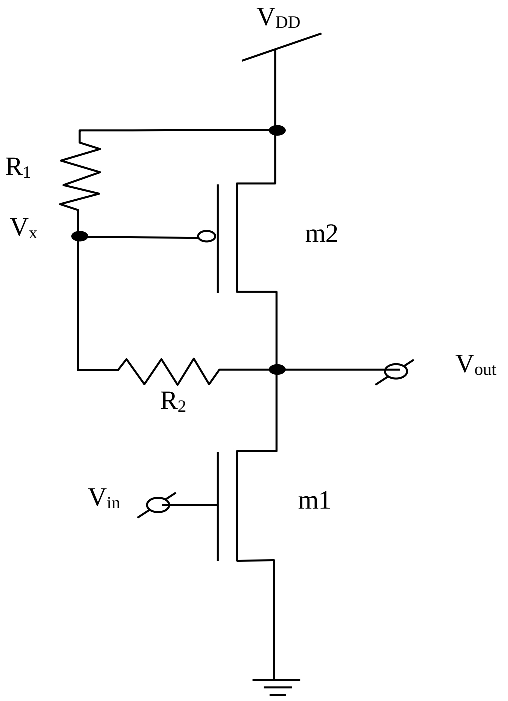


2b24.

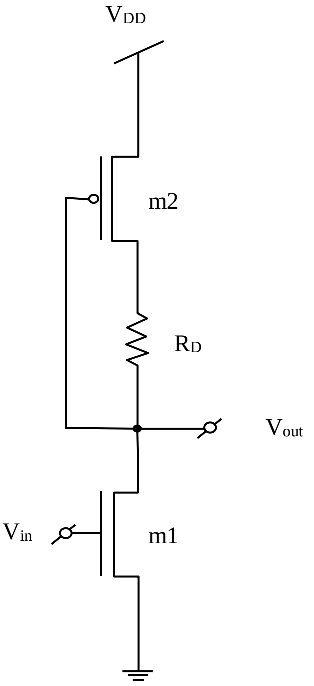
Find $A_v=dV_{out}/dV_{in}$ small signal gain. g_{m1}, g_{mb1}, R_1, R_2 values are known. Ignore channel length modulation.



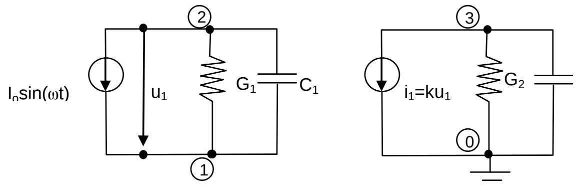
2b25.
Sketch V_{out} versus V_{in}, as V_{in} varies from 0 to V_{DD}. Identify the important transition points. Find $A_v=dV_{out}/dV_{in}$ small signal gain. g_{m1}, g_{m2}, R_1, R_2 values are known. Ignore channel length modulation. $R_1<R_2$.



2b26.
Sketch V_{out} versus V_{in}, as V_{in} varies from 0 to V_{DD}. Identify the important transition points. Find $A_v=dV_{out}/dV_{in}$ small signal gain. g_{m1}, g_{m2}, R_D values are known. Ignore channel length modulation.



2b27.
The following circuit should be analyzed with an AC analysis for a sine shaped input current signal. The circled numbers represent the node labels.



Give the value for all elements in the matrix, Y_{xy} and A_{x4}, and right side vector I_{nx} for a modified nodal analysis in the frequency domain.

$$\begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & A_{14} \\ Y_{21} & Y_{22} & Y_{23} & A_{24} \\ Y_{31} & Y_{32} & Y_{33} & A_{34} \\ Y_{41} & Y_{42} & Y_{43} & A_{44} \end{bmatrix} \cdot \begin{bmatrix} u_{n1} \\ u_{n2} \\ u_{n3} \\ i_1 \end{bmatrix} = \begin{bmatrix} I_{n1} \\ I_{n2} \\ I_{n3} \\ I_{n4} \end{bmatrix}$$

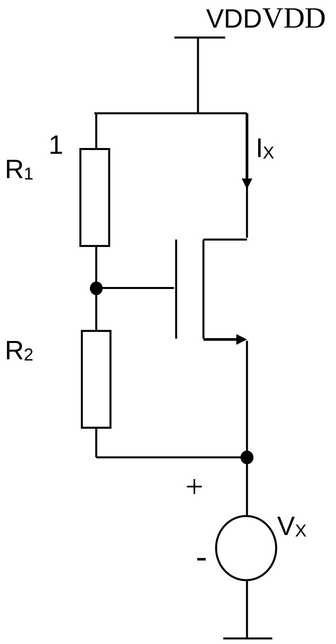
2b28.
An NMOS transistor has a threshold voltage of 0.4V and a supply voltage of V_{DD}=1.2V. The threshold voltage (V_t) has to be reduced by 100mV to obtain faster device. Consider the constants in Table 1, unless otherwise specified in the question.

a) By what factor would the saturation current increase (at $V_{gs}=V_{ds}=V_{dd}$)? Consider velocity saturation model.
b) By what factor would the sub-threshold leakage current increase at room temperature (25C, 300K) at V_{gs} =0 and $V_{ds}=V_{dd}$? Assume n = 1.4, and V_{offset}= 0.
c) By what factor would the sub-threshold leakage current change at T= 400K? Will it increase or decrease? Assume the threshold voltage is independent of T.
d) Assume the threshold voltage has to be reduced by increasing the body voltage (using body effect), what would be the value of V_{sb} to reach the targeted V_t?

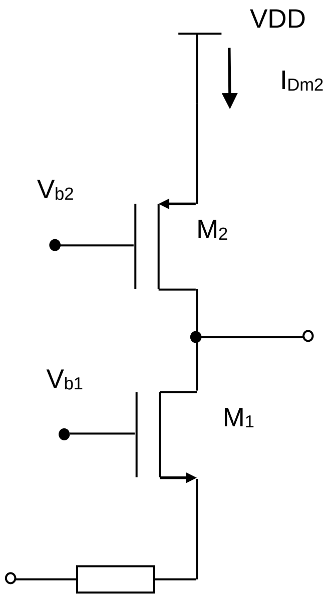
2b29.
For the 90nm technology, the device parameters are about the same as for 130 nm technology except for V_{t0} (zero-bias threshold voltage) and t_{ox} (oxide capacitance per unit area). The channel length is L=80nm (due to lateral diffusion). In order to determine V_{t0} and t_{ox}, some device measurements are made on an NMOS transistor with W = 400nm to produce the results shown in the table below. Estimate the value of V_{t0} and t_{ox} from these measurements (ECL term can be ignored). Consider the constants in Table 1, unless otherwise specified in the question.

V_{ds} (V)	V_{gs} (V)	V_{sb} (V)	I_{ds} (μA)
1.2	1.2	0.0	78.70
1.2	1.2	0.5	85.28
1.2	1.0	0.0	56.21
1.2	0.8	0.0	33.72
1.2	0.6	0.0	11.24

2b30.
Show the dependence of I_x from V_x, when V_x changes from 0 to VDD. g_{m1},V_{TH1}, R_1, R_2 values are known. Ignore secondary effects.

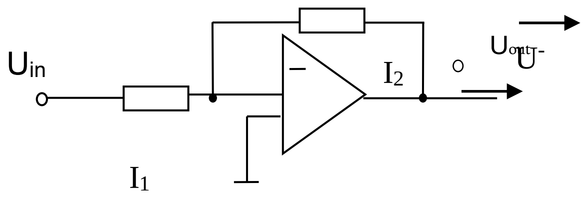


2b31.
Find A_v=dV_{out}/dV_{in} small signal amplification coefficient. g_{m1}, g_{m2}, R_S, V_{TH1}, V_{TH2}, r_{01}, r_{02} values are known. Ignore body effect. M_1 and M_2 are saturated.

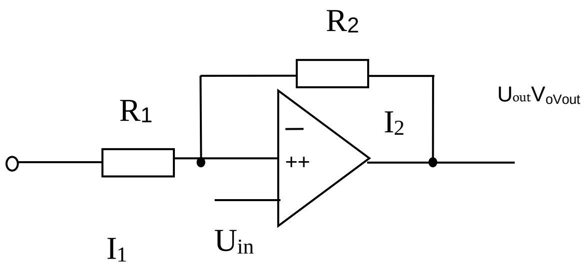


2b32.

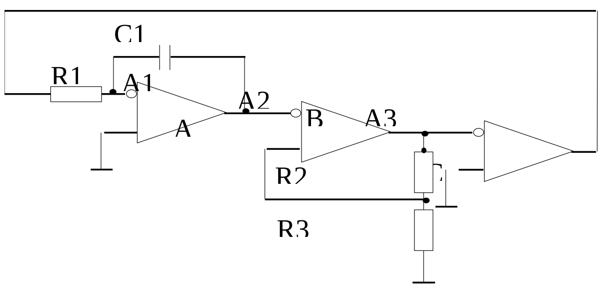
Get the output signal expression of inverse amplifier, built by OpAmp, considering OpAmp's K'u real amplification coefficient and input resistance for R'in differential signal (take Uin>0). Compare it with the version of an ideal OpAmp.



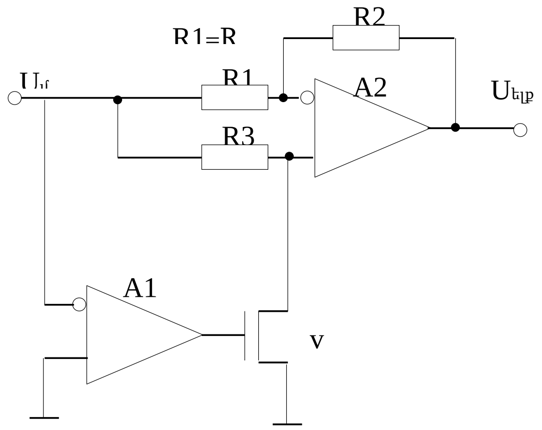
2b33.
Get the amplification coefficient expression of non-inverse amplifier, built by OpAmp, considering OpAmp's K`u real amplification coefficient and input resistance for R`in differential signal (take Uin>0). Compare it with the version of an ideal OpAmp.



2b34.
Calculate the output signals periods of the triangle and pulse waveform generator. R1=20 k, C1=0,1mkF, $U_{outA2max}$ = $U_{outA3max}$ =+5v , $U_{outA2min}$ = $U_{outA3min}$= -5v, R2 = R3 = 1 k. A1, A2 and A3 operational amplifiers are ideal.

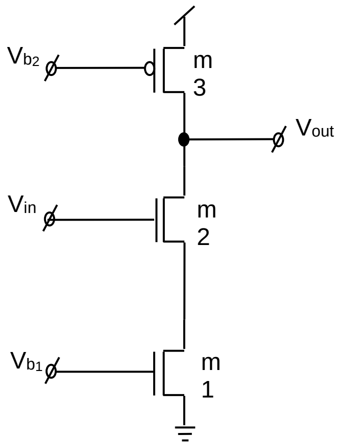


2b35.
Calculate the voltage repeating accuracy from input to output of the full wave rectifier. R1=R2=R3= 20 k, the on resistance of V1 transistor R_{on}= 0,1k , A1 and A2 are ideal



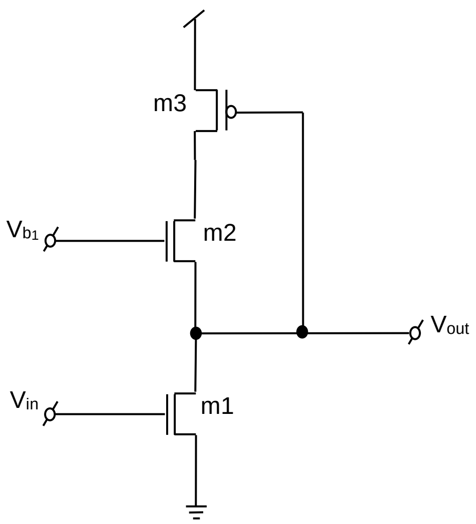
2b36.

Calculate $A_v=dV_{out}/dV_{in}$ small signal gain, considering that all transistors are saturated. Neglect Body Effect.



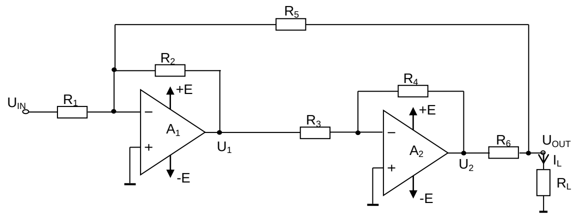
2b37.

Calculate $A_v=dV_{out}/dV_{in}$ small signal gain, considering that all transistors are saturated. Neglect Body Effect.



2b38.

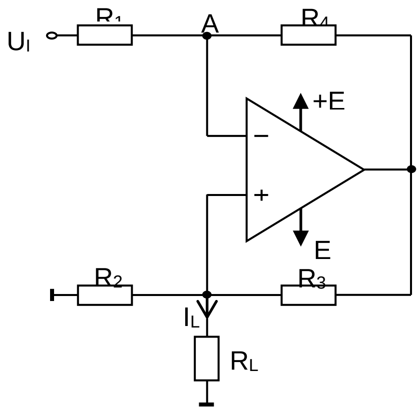
In the circuit of stable current source with connected to ground R_L, R1 = R2 = R3 = R4. Prove if R2 = R5 + R6, the output current of the circuit does not depend on R_L load resistance and $I_L = U_{IN}/R6$.



2b39.

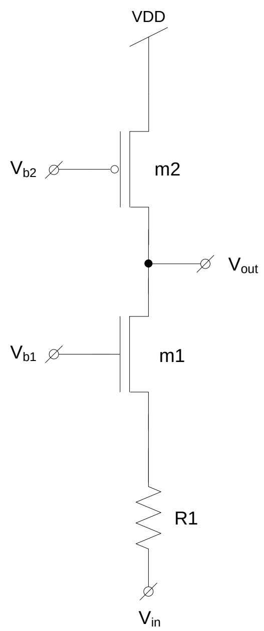
Prove that in Howland current source if R3/ R2 = R4/ R1, then the output current:

$I_L = - U_{IN}/R2$, of the circuit does not depend on R_L load resistance.

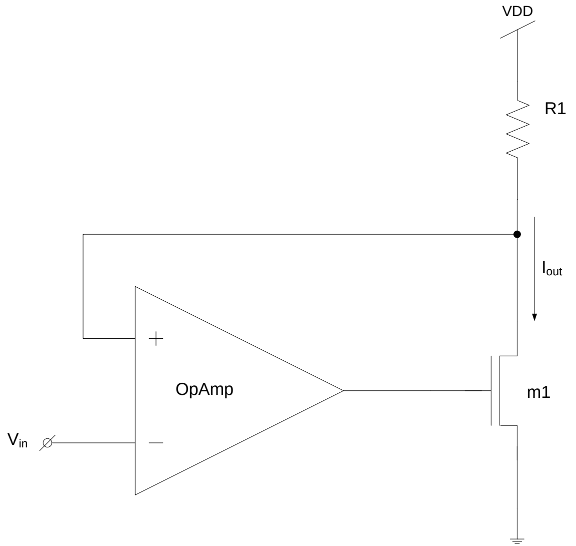


2b40.

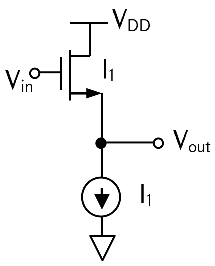
Find $A_v=dV_{out}/dV_{in}$ small signal gain, considering that all transistors are saturated. R1, g_{m1}, g_{mb1}, g_{m2}, r_{01}, r_{02} values are known.



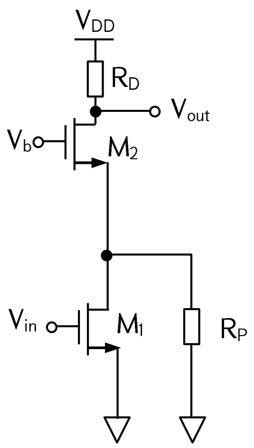
2b41.
Find the change dependence of I_{out} output current from the change of V_{in} input voltage: G= dI_{out} /dV_{in}: R1, g_{m1}, r_{01}, Av (OpAmp gain) values are known. The input resistance of OpAmp is infinitely high and m1 transistor is saturated.



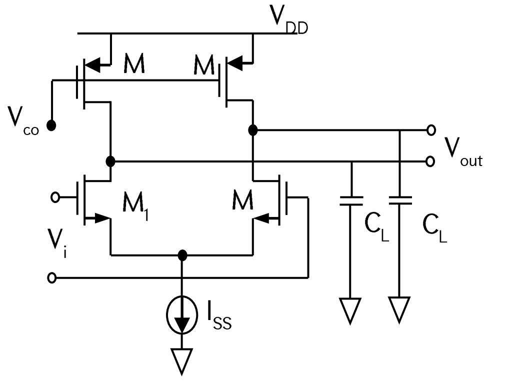
2b42.
Suppose in the given source follower, $(W/L)_1$ = 20/0,5, I_1 = 200 μA, V_{TH0} = 0,6 V, $2\Phi_F$ = 0,7 V, $\mu_n C_{ox} = 50\mu A/V^2$, and $\gamma = 0.4V^2$. Calculate V_{out} for $V_{in} = 1.2V$.



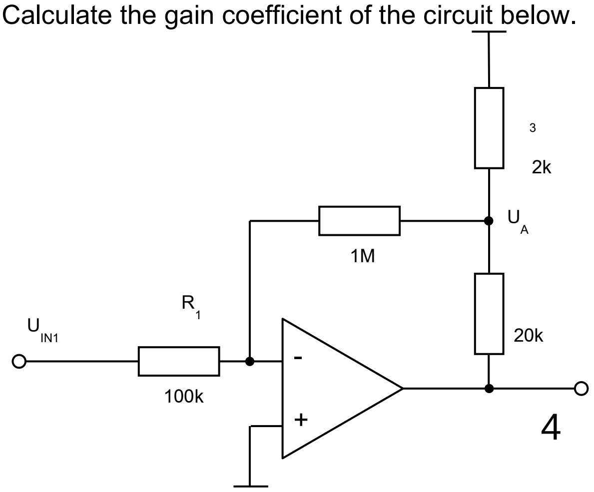
2b43.
Calculate the voltage gain of the given circuit if $\lambda = 0$.



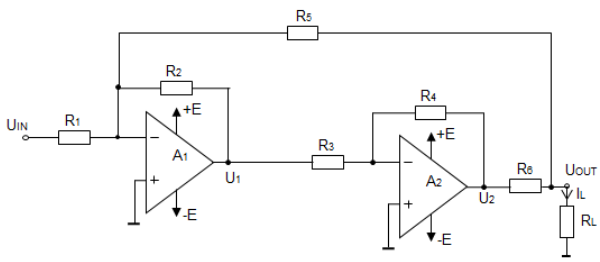
2b44.
For given dimensions and bias currents in the following figure, determine the maximum allowable value of V_{cont}. What happens if M_3 and M_4 enter saturation?



2b45.
Calculate the gain coefficient of the circuit below.

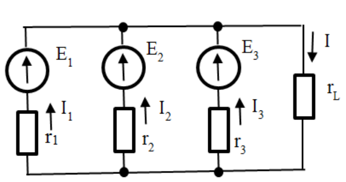


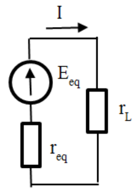
2b46.
In a current reference source with grounded load $R_1 = R_2 = R_3 = R_4$.



Bring out the expression of I_L output current and confirm that if $R_5 = R_2 - R_6$, it does not depend on R_L – load resistance.

2b47.
The figure illustrates electrical circuit, composed of voltage sources and resistances, as well as its equivalent circuit, the parameters of which are: E_1=4v; E_2=8v; E_3=2,4v; r_1=20Ohm; r_1=50Ohm; r_1=12Ohm; r_L=7Ohm

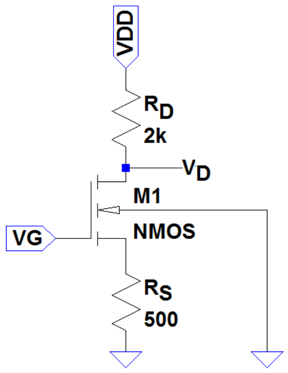




Define E_{eq}; r_{eq}; I; I_1; I_2; I_3

2b48.

For circuit in the figure, find voltage on drain (V_D) when it is known: V_{DD}=5V, V_G=1.6V, R_D=1.5kOhm, R_S=1kOhm, and MOS operates in saturation with $I_D=A(V_{GS}-V_T)^2$.
Transistor parameters are: V_T=1V, A=1mA/V^2.



2b49.

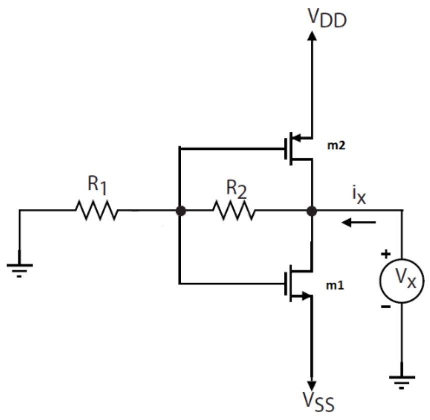
Calculate C_{IN} – input capacitance of a MOS amplifier with Common Source connection if C_{GS} = C_{DG} = 1 pF, the slope of the transfer characteristic of operating part is g_m = 1 mA/V, and the resistance of a load resistor in drain's chain is R_D = 10k.

2b50.

Calculate dU_{HIS} width of hysteresis of transfer characteristics of a comparator with positive feedback if the output voltage values of the comparator are U_{MAX} = 3 V, U_{MIN} = 0,2 V, and the resistors of feedback voltage divider are equal to each other.

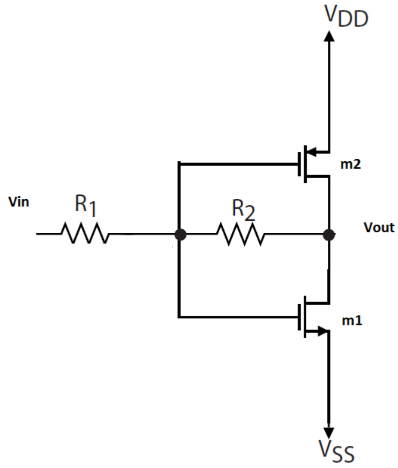
2b50.

Find the expression for the small-signal output resistance. Assume that all transistors are in saturation and R1, R2, g_{m1}, g_{m2}, r_{01}, r_{02} are known.



2b51.

Find an expression for the small-signal gain. Assume that all transistors are in saturation and R1, R2, g_{m1}, g_{m2}, r_{01}, r_{02} are known.



3. RF CIRCUITS

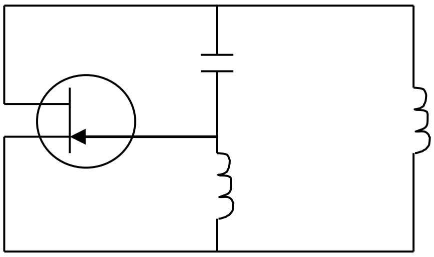
a) Test questions

3a1. Define super-heterodyne receiver's intermediate frequency if the input signal frequency is fs = 900 MHz, and heterodyne frequency is fh = 700 MHz.

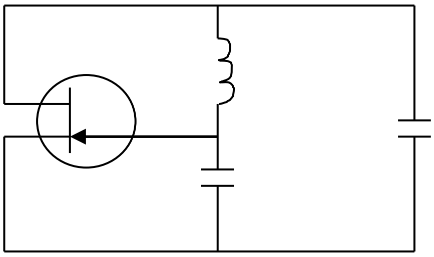
A. 200 MHz
B. 600 MHz
C. 1400 MHz
D. 1600 MHz
E. 1800 MHz

3a2. Which of the shown circuits is called "Inductive triple point"?

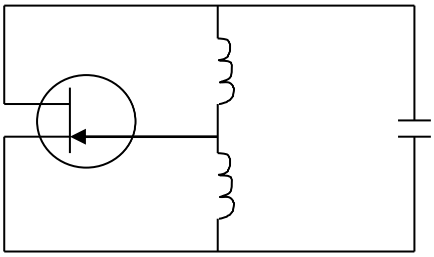
A.



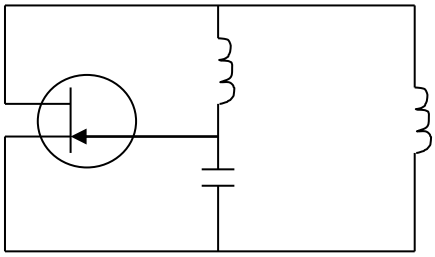
B.



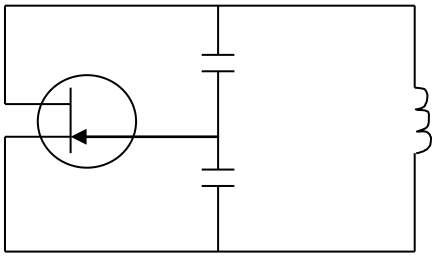
C.



D.



E.



3a3. Find the initial phase of second harmonic of the following signal:

$$s(t)=\sum_{n=1}^{2}\frac{2}{n}\cos\left[2\pi n\cdot 10^{6}t+\frac{\pi}{n}(-1)^{n+1}\right]$$

A. $-\pi$

B. $-\frac{\pi}{2}$

C. *0*

D. $\frac{\pi}{2}$

E. π

4. SEMICONDUCTOR PHYSICS AND ELECTRONIC DEVICES

a) Test questions

4a1. Which circuit based on operational amplifier has transfer function with hysteresis?

A. *Non-inverting amplifier*
B. *Inverting adder*
C. *Comparator without feedback*
D. *Comparator with positive feedback*
E. *Comparator with negative feedback*

4a2. Does semiconductor diode's I/V characteristics differ from I/V characteristics of ohmic resistance?

A. *Yes, it depends on the applied voltage direction and is nonlinear*
B. *Yes, it depends on the applied voltage direction and is linear*
C. *No, as the more direct voltage, the more is the current*
D. *Partially, as current exists irrespective of voltage direction*
E. *The correct answer is missing*

4a3. What parameters of semiconductor material are needed for transistor fabrication?

A. *Charge carriers' mobility and concentration*
B. *Charge carriers' concentration, minority charge carriers' life time, mobility*
C. *Charge carriers' concentration and diffusion coefficient*
D. *Charge carriers' concentration, diffusion coefficient, mobility, band gap*
E. *The correct answer is missing*

4a4. Which regions does the graph of drain current dependence on source-drain voltage for p-n junction field effect transistor consist of?

A. *Linear dependence, saturation*
B. *Linear dependence, saturation, breakdown*
C. *Linear dependence, transition, saturation, breakdown*
D. *Linear dependence, transition, breakdown*
E. *The correct answer is missing.*

4a5. How are the oxide layer capacitor C_0, the surface state capacitor C_{ss} and the differential capacitor of the surface charge layer connected between one another in a MOS structure?

A. *Css and C_0 parallel, and with Csc sequentially*
B. *Css and Csc parallel, and with C_0 sequentially*
C. *C_0 and Csc sequentially, and with Csc parallel*
D. *All capacitors are connected parallel to one another*
E. *The correct answer is missing.*

4a6. How does differential resistance of p-n junction change parallel to direct current increase?

A. *Does not change*
B. *Decreases*
C. *Increases*
D. *Increases, then decreases*
E. *The correct answer is missing*

4a7. How many times will diffusion capacitance of a bipolar transistor increase if its base length increases twice?

A. *Will not change*
B. *Will increase $\sqrt{2}$ times*
C. *Will increase 4 times*
D. *Will decrease twice*
E. *The correct answer is missing*

4a8. How does the p-n-p bipolar transistor's transfer factor depend on diffusion length of holes L_p?

A. *No dependence*
B. *Increase with the increase of L_p by $\beta = 1 - \frac{W}{2L_p}$ law*
C. *Increase with the increase of L_p by $\beta = 1 - \frac{1}{2}\left(\frac{W}{L_p}\right)^2$ law*
D. *Decreases*
E. *The correct answer is missing*

4a9. The light of what maximum wavelength can affect the current of silicon ($E_g = 1.1$ eV) photodiode?

A. $\lambda_{max} = 1130\,nm$

B. $\lambda_{max} = 550\,nm$

C. $\lambda_{max} = 1240\,nm$

D. $\lambda_{max} = 335\,nm$

E. The correct answer is missing

4a10. How is bipolar transistor's current gain expressed in common base circuit with the help of emitter effectiveness γ, transition coefficient β and collector's avalanche multiplication factor *M*?

A. $\alpha = \frac{\gamma\beta}{M}$

B. $\alpha = \gamma\beta M$

C. $\alpha = \frac{M}{\gamma}\beta$

D. $\alpha = \frac{\beta}{\gamma M}$

E. The correct answer is missing

4a11. Is operating temperature range of ICs, computers and other semiconductor devices conditioned by the used semiconductor material's band gap?

A. Yes, the more the band gap, the more temperature range

B. No, as concentration of minority charge carriers is independent from temperature

C. Conditioned partially as by increasing the temperature, carriers' mobility decreases

D. No, as band gap does not depend on temperature

E. The correct answer is missing

4a12. Which expression is wrong?

A. Diode subtypes are: point-junction diodes, stabilitrons, varicaps and tunnel diodes

B. In tunnel diodes reverse current for the same voltage is higher than direct current value

C. In varicaps with increase of voltage barrier capacitance increases

D. Schottky diodes operation is based on processes which take place in semiconductor-metal contact

E. The response time of Schottky diodes, therefore, frequency properties are conditioned by barrier capacitance

4a13. Field effect transistors, compared with bipolar transistors

A. Have small input resistance

B. Have small noise coefficient

C. The current is at the same time conditioned by electrons and holes

D. Provide current amplification

E. The performance is mainly conditioned by injection of minority carriers

4a14. Through which device is the electrical signal amplification implemented?

A. Resistor

B. Capacitor and inductor

C. Diode

D. Transistor

E. Photodiode

4a15. How many pins does the field effect transistor have?

A. 1 gate

B. 2 sources and 1 drain

C. 3 sources, 1 gates and 1 drain

D. 2 bases and 1 collector

E. 1 source, 1 gate and 1 drain

4a16. Is the gate of a field effect transistor isolated from its channel?

A. Yes

B. No

C. Partially and there is weak tunnel coupling

D. In saturation mode of field effect transistor most part of channel current flows through gate

E. The correct answer is missing

4a17. n – type Ge sample, which is anticipated for making a transistor, has 1.5 Ohm·cm specific resistance and $5.4 \cdot 10^3$ cm^3/Kl Holy coefficient. What does the charge carriers' concentration and their mobility equal?

A. $1.6 \cdot 10^{21}$ *m-3, 5* $m^2/V \cdot s$

B. $1.6 \cdot 10^{21}$ *m-3, 0.1* $m^2/V \cdot s$

C. $1.16 \cdot 10^{21}$ *m-3, 0.36* $m^2/V \cdot s$

D. $2 \cdot 10^{20}$ *m-3, 0.36* $m^2/V \cdot s$

E. The correct answer is missing.

4a18. By means of what semiconductor device can light influence be detected?

A. Posistor

B. Resistor

C. Photodiode

D. Capacitor

E. Inductor

4a19. Which materials' conductivity is higher?
A. *Dielectrics*
B. *Semiconductors*
C. *Metals*
D. *All have low* conductivity
E. *All have high* conductivity

4a20. How does the negative differential resistance current range change depending on the density of lightly degenerated n-region impurities in tunnel diode?
A. *Interval decreases when increasing density*
B. *Interval increases when increasing density*
C. *It is not conditioned by density of impurity*
D. *Interval increases when reducing density*
E. *All the conditions are true*

4a21. Generally, what is the response time of photodiode conditioned by?
A. The diffusion time of equilibrium carriers in the base
B. Their transit time through the layer of p-n junction
C. RC constant of diode structure
D. Only A and C
E. Conditions A, B, C

4a22. Which statement mentioned below is not true for ohmic contact?
A. *Electrical resistance of ohmic contact is small*
B. *Electrical resistance of ohmic contact does not depend on the current direction if the current value does not exceed the given value*
C. *Electrical resistance of ohmic contact does not depend on the current direction in case of any current value flowing through it*
D. *Most part of ohmic contacts is formed on the basis of n-n+ or p-p+ type contacts*
E. *All the answers are correct*

4a23. By increasing the lifetime of electrons 4 times, their diffusion length
A. *Increases 4 times*
B. *Increases twice*
C. *Does not increase*
D. *Reduces twice*
E. *The correct answer is missing*

4a24. What does the generation frequency depend on in Gunn diode?
A. *Mobility speed of field domain*
B. *Impurity density in semiconductor*
C. *Sample length*
D. *Dielectric permeability of material*
E. *All the answers are correct*

4a25. How can the cutoff voltage of MOS transistor change?
A. *By opposite voltage of substrate-channel junction, when substrate is higher ohmic than the channel*
B. *By opposite voltage of substrate-channel junction when substrate resistance is equal or smaller than the channel resistance*
C. *By voltage applied to the gate*
D. *By A and C*
E. *By B and C*

4a26. Which statement is wrong for unipolar transistors?
A. *In unipolar transistors, physical processes of current transport are conditioned by one sign carriers-electrons or holes*
B. *In unipolar transistors, physical processes of current transport are conditioned by the injection of minority carriers.*
C. *In unipolar transistors current control is carried out by the vertical electrical field*
D. *The surface channel unipolar transistor includes metal-dielectric-semiconductor structure*
E. *The correct answer is missing*

4a27. What is the high frequency property of Schottky diode conditioned by?
A. *Moving the majority carriers through diode*
B. *Excluding minority carriers' accumulation in diode*
C. *Value of Schottky barrier*
D. *Impurity density in a semiconductor*
E. *Only C and D*

4a28. Which of the below written statements is wrong for an integrated capacitor?
A. *An integrated capacitor represents IC element consisting of conductive electrodes (plates), divided by isolation layer*
B. *In ICs the role of an integrated capacitor is often performed by*

reverse-biased p-n junctions of a transistor structure

C. *The quality factor of an integrated capacitor is defined by the following:* $Q = 2\pi\, f\, RC$ *where* $f -$ *operating frequency,* $C -$ *capacitance of a capacitor,* $R -$ *resistance of a resistor sequentially connected with the transistor*

D. *The quality factor of an integrated capacitor characterizes loss of power at capacitive current junction*

E. *All the answers are correct*

4a29. Which of the below mentioned statements is wrong for electronic lithography?

A. *In this method the electron beams are used as a source of radiation*

B. *The method of electron beam lithography is based on non-thermal influence left by electron beam on resist*

C. *The ultraviolet beams fall on resist surface at electron beam lithography*

D. *It is possible to reduce diffraction effects by increasing the electron accelerating voltage in electron beam lithography*

E. *The correct answer is missing*

4a30. Which of the below mentioned statements is correct for a bipolar transistor in saturation mode?

A. *Emitter and collector junctions are forward-biased*

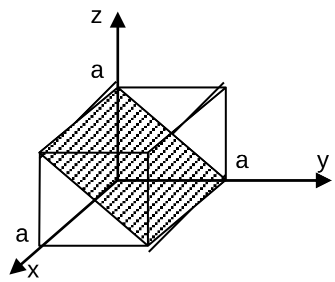
B. *Emitter junction is forward-biased, and collector junction –reverse-biased*

C. *Transistor base resistance in this mode is maximum, as emitter and collector junctions inject large number of free particles to base region*

D. *Free carriers' extraction takes place from transistor base being in this mode*

E. *The correct answer is missing*

4a31. What crystallographic plane is underlined in cubic lattice?



A. *(100)*

B. *(101)*

C. *(001)*

D. *(011)*

E. *(110)*

4a32. Due to what properties is silicon considered the main material of microelectronics?

A. *Exclusive combination of its band gap and electro-physical parameters*

B. *Its oxide stability and isolating properties*

C. *High development of technological methods related to it in different physical-chemical processes*

D. *The value of its natural resources*

E. *All the answers are correct*

4a33. What statement is wrong for metal-nitride-oxide semiconductor (NMOS) field effect transistor?

A. *In a such transistor, silicon nitride and silicon dioxide double structure serves as a subgate isolator*

B. *There are many deep levels (traps) for electrons in silicon nitride layer*

C. *The layer's thickness of silicon dioxide is selected such that it is not tunnel transparent*

D. *After removing the voltage on MNOS-field transistor's gate, the injected charge remains long trapped which corresponds to the existence of induced inversion layer.*

E. *The correct answer is missing*

4a34. If the density of semiconductor's defects is large,

A. *The lifetime of carriers will be large*

B. *The conductivity of semiconductor will decrease*

C. *The recombination speed will increase*

D. *The current will remain constant*

E. *The generation speed will increase*

4a35. The performance of tunnel diodes is larger than the one of p – n junction as

A. Injection level is large
B. Injection mechanism is different
C. Junction capacitance is small
D. Current is formed by electrons and holes
E. Potential barrier's height is small

4a36. What diode is called stabilitron?

A. Direct current of which exponentially increases with the voltage
B. Reverse current of which is saturated
C. Reverse branch of its the volt-ampere characteristic has a region very strict dependence of current on voltage
D. The volt-ampere characteristic of which has an N- type region
E. The correct answer is missing

4a37. Threshold voltage of a short channel MOS transistor is smaller than the one of a long channel MOS as

A. It occupies smaller area
B. The number of technological processes is small
C. Gate controls smaller number of charge
D. There are piled charges on the boundary of oxide-semiconductor junction
E. Intrinsic capacitance is large

4a38. In Gann diode, negative conductivity occurs

A. Due to ohmic property of contacts
B. When p-n junction is controlled by larger voltage
C. Due to field domain
D. Carriers' flight time is small
E. No answer is correct

4a39. To increase MOS transistor's drain conductance which statement below is wrong?

A. It is necessary to reduce channel length and increase its width
B. It is necessary to increase the thickness of subgate isolator
C. It is necessary to use dielectric with more dielectric permittivity
D. It is necessary to use as a transistor's substrate a semiconductor with more carrier's mobility
E. The correct answer is missing

4a40. How does base volume resistance affect on semiconductor's diode characteristic?

A. It leads to the sharp increase of the current
B. The direct current, depending on the voltage, increases slower than exponential law
C. Volt - ampere characteristic, starting with the smallest value of voltage, becomes ohmic
D. Negative differential conductance region appears on volt-ampere characteristic of the diode
E. The correct answer is missing

4a41. Carriers' mobility, depending on temperature, changes:

A. Increases linearly
B. Decreases exponentially
C. Remains constant
D. Changes nonlinearly
E. No answer is correct

4a42. The reduction of oxide layer's thickness in a MOS transistor leads to:

A. Increase of transistor's performance
B. Decrease of transistor's performance
C. Increase of intrinsic capacitance
D. Increase of leakage currents
E. Decrease of occupied area

4a43. Numbers of basic equivalent minimums of silicon and germanium conduction bands correspondingly are:

A. 6 and 6
B. 6 and 4
C. 6 and 8
D. 4 and 6
E. 2 and 4

4a44. The band gap of a semiconductor with the increase of magnetic field

A. Increases linearly
B. Increases exponentially
C. Decreases linearly
D. Decreases exponentially
E. Remains unchanged

4a45. Fermi level of full compensated semiconductor at 0K temperature is located on:

A. Middle of conduction band bottom and donor level
B. Middle of donor and acceptor levels
C. Middle of band gap
D. Donor level
E. Acceptor level

4a46. Two contacting semiconductors are in equilibrium if

A. Forbidden band gaps are equal
B. Fermi levels are equal
C. Free carrier concentrations are equal
D. Current carrier lifetimes are equal
E. Current carrier diffusion coefficients are equal

4a47. If Fermi and donor levels are equal, the probability of electron occupancy in donor level is

A. 1/2
B. 1
C. 2/3
D. 1/3
E. 0

4a48. Fundamental parameters of a semiconductor are

A. Electron effective mass
B. Electron and hole lifetimes
C. Electron and hole mobility
D. Resistivity
E. Coefficient of lattice thermal conductivity

4a49. p-n junction potential barrier under influence of absorbing light

A. Increases
B. Increases, then decreases
C. Decreases, then increases
D. Decreases
E. Remains unchanged

4a50. When p–n junction occurs, which part of it acquires i–type conductivity?

A. High ohmic part outside p-n junction
B. Contact domain of p– and n– parts
C. Deep domains of p– and n– parts
D. The layer of spatial charges the layer of p-n junction
E. Possible high ohmic part, adjacent to ohmic contact

4a51. When p–n junction occurs, which flow of carriers gives rise to potential barrier?

A. Diffusion of majority carriers of p– and n– domains
B. Drift of minority carriers of p– and n– domains
C. Two flows together
D. Only diffusion of electrons
E. Only drift of holes

4a52. In case of being connected by general base of a bipolar transistor, when injection is missing from the emitter, on what part does the voltage, supplying collector p–n junction, fall?

A. The part of load resistance, connected to collector.
B. The layer of drift charges of collector p–n junction.
C. Both A and B.
D. High ohmic part of collector contact.
E. The part outside spatial charges of a collector.

4a53. What is comparably high temperature stability of a field transistor conditioned by?

A. Reverse bias voltage of gate
B. Possibility of modulation of channel resistance
C. Output current conditioned by majority carriers
D. Both B and C
E. Quality of ohmic contacts

4a54. How does the drain current of a filed transistor change when increasing the temperature?

A. Increases on the account of getting rid of surface state electrons
B. Decreases due to decreasing carriers' mobility
C. Both A and B occur
D. Does not change
E. Increases together with output contact heating

4a55. What is the high performance of Schottky diode conditioned by?

A. Output operation of a semiconductor
B. Lack of minority carriers' accumulation in a semiconductor
C. Move of majority carriers conditioned by diode operation
D. Presence of charge capacitance
E. Output operation of a metal

4a56. Why is the lightdiode's radiation spectrum not strictly onewave?

A. Because radiation reunion of carriers occurs between two levels
B. Because radiation reunion of carriers occurs between electrons which are on one group of levels and holes which are in another group
C. Because spectral distribution of radiation, coming from diode changes
D. Because it is conditioned by injection of carriers

E. Because reunion is missing in p-n junction

4a57. When does a semiconductor amplifier, having positive feedback, become a generator?

A. When the mirrors, creating positive feedback, provide pure reflection

B. When amplification exceeds all the losses of radiation in the device

C. When radiation losses in unit length of active layer are minimum

D. When radiation is directed

E. When radiation is provided in the layer of p–n junction

4a58. If p-n junction with C_{dif} diffusion and $C_{ch\arg}$ charge capacitances is in equilibrium state, then

A. $C_{dif} = 0, C_{ch\arg} = 0$

B. $C_{dif} \neq 0, C_{ch\arg} \neq 0$

C. $C_{dif} \neq 0, C_{ch\arg} = 0$

D. $C_{dif} = 0, C_{ch\arg} \neq 0$

E. $C_{dif} = \infty, C_{ch\arg} \neq 0$

4a59. There is double heterojunction luminescent *AlGaAs - GaAs - AlGaAs* structure. Refraction index of *GaAs* is higher than refraction index of *AlGaAs*. What is the role of intermediate *GaAs microsize* layer for radiation?

A. Majority carriers

B. Ohmic contact

C. Waveguide

D. Reduction of radiation

E. Observation of radiation.

4a60. Which is the key advantage of double heterojunction luminescent structure towards single heterojunction luminescent structure?

A. Operates at higher bias voltage

B. Easier realized technologically

C. Provides high intensity of radiation by double injection

D. Provides high radiation losses

E. Provides chaos observation of radiation

4a61. What type of conductivity does strictly compensated semiconductor have?

A. Ion conductivity

B. Electronic conductivity

C. i-type conductivity

D. Hole conductivity

E. Has no conductivity

4a62. What type of radiation is there in radiating semiconductor structures?

A. Spontaneous

B. Chaotic

C. Compulsive

D. Spontaneous and compulsive

E. Multiwave

4a63. When does non-equilibrium electro conductance reach dynamic balance in a semiconductor, created by light?

A. When the increase of non-equilibrium carrier density, generated by light, occurs

B. When non-equilibrium hole density exceeds electrons

C. When the generation and reunion processes of non-equilibrium holes and electrons reach dynamic balance

D. When observing radiation energy is enough for moving valance electron to conductance region

E. When the semiconductor is in total vacuum

4a64. What is the high photosensitivity of a field phototransistor conditioned by?

A. Possibility to connect large input resistance

B. Gate photocurrent

C. Modulation of photogenerated carrier channel conductance, drain current gain

D. Environment to observe radiation

E. All the mentioned factors

4a65. What properties of p-n junction allow creating group technology for high efficiency ICs?

A. The capacitive property of p-n junction

B. Signal correction property by one p-n junction

C. Signal amplification property by two p-n junction

D. The property of p-n junction resistance

E. All the mentioned properties

4a66. What does radiation's quantum energy depend on?

A. Spectrum form of radiation

B. Intensity of radiation flow

C. Radiation frequency

D. Environment of observing radiation

E. All the mentioned factors

4a67. What does the abrupt heterojunction conductance band difference equal to?

A. The difference of work-function

B. The difference of dipole moments

C. The difference of semiconductors affinities

D. The difference *of band gap*

E. The difference of Fermi energy

4a68. The charge carriers' mobility in a double gate MOS is larger as

A. Threshold transconductance is large

B. Short channel effects are present

C. Oxide effective thickness is small

D. The perpendicular field coefficient is small in the channel

E. The channel is far from substrate

4a69. The electric field value in p-n junction at avalanche multiplication (impact ionization) regime is defined by:

A. Avalanche breakdown current in the given point

B. Avalanche breakdown current change rate at time

C. Avalanche breakdown voltage

D. The electron and hole ionization rates

E. The phase difference between current and voltage

4a70. The domain formation time in Gann diode:

A. Must be larger than Maxwell relaxation time

B. Must be defined by the value of applied field

C. Must equal to transit time

D. Must be larger than the lifetime of electrons and holes

E. Must be smaller than transit time

4a71. The charge carriers' mobility in the base of drift transistor is large

A. As the concentration of impurities is small

B. The base width is small

C. The emitter impurity concentration is high

D. The diffusion coefficient is large

E. None of the answers is correct

4a72. The tunnel diode high frequency operation is conditioned by:

A. The p-n doped impurity degree

B. Depletion layer width

C. p-n junction capacitance

D. J_{max}/J_{min} *ratio*

E. The value of excess current

4a73. What the depletion layer width near the drain in Shottky barrier controlled FETs is conditioned by?

A.The source-drain impurity concentration

B. The drain applied voltage

C The substrate legiration degree

D. The voltage difference between gate and channel drop voltage

E. The sum of gate voltage and channel voltage

4a74. What type of a semiconductor can be defined by thermal-compression methods if p=5n, and $\mu_n = 10\mu_p$?

A. Intrinsic type of conductance

B. p type

C. n type

D. Both p type and n type

E. None of the answers is correct

4a75. Can the conductance of a conductor be of p-type?

A. It can if the conductance band is almost occupied (the F–is high from the middle of band gap)

B. It cannot

C. The conductance of a conductor will be of n-type

D. Both p type and n type

E. None of the answers is correct

4a76. On the diffraction image of waves, redistribution of incident wave energy occurs (divided into parts). Is the electronic wave (de Broil wave) divided into parts during the diffraction of electrons?

A. Also divided into parts

B. Turns into phonon

C. Turns into the energy of crystalline lattice

D. None of the answers is correct

E. No, is not divided into parts as the electron, as a whole, appears in the diffraction image maximum

4a77. If the effective mass were gravitation characteristic, in what direction would the hole move in the Earth gravitation field?

A. Vertically upward

B. Wouldn't move

C. Would move chaotic

D. Vertically downward

E. None of the answers is correct

4a78. The energetic distance between the donor and acceptor levels is smaller than the band gap width ($E_d - E_a < ^1E$). Why is the probability of electron transition from the acceptor to donor (or the opposite) very small compared with the probability of band-band?

A. Because the donor levels are not free
B. Because the acceptor levels are not free
C. Because the width between the dopand-dopand is large
D. Because the number of free places in bands is large
E. None of the answers is correct

4a79. Complementary MOSFET is characterized by:.

A.The presence of only p-type channel
B.The presence of only n-type channel
C. The presence of p- and n-type channels
D. The absence of channel

4a80. Silicon thermal dioxide thickness grows:

A. Only on the silicon substrate surface
B. On the silicon substrate surface and in the near-surface region
C. Only in the silicon near-surface region
D. In the volume of silicon substrate

4a81. The buffer n^+ buried layer in the n-p-n-type bipolar transistor can be built in for:

A. To decrease the volume resistance of collector region
B. To increase the volume resistance of collector region
C. To increase collector-emitter junction resistance
D. To reduce collector-emitter junction resistance
E. To reduce the lifetime of minority charge carriers in collector region

4a82. What are the silicon thermal oxidation processes for limiting the oxidation rate?

A. Deposition of oxidant (O_2, H_2O) particles on Si surface
B. Oxidant diffusion through SiO_2 layer to the Si-SiO_2 interface
C. Oxidation chemical reaction with Si and origination of the new SiO_2 layer
D. By the A), and B) phases simultaneously
E. Diffusion of the reaction steam results into the Si external surface

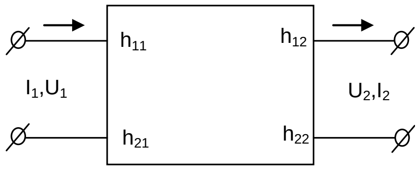
4a83. Ion-implantation doping advantages compared with diffusion process (mark the wrong answer).

A. Exact (precise) regulation of impurities distribution profile
B. A wider range of impurities
C. Small sideways
D. Low temperature of process
E. Profiles of deep distribution of impurities

4a84. The silicon thermal oxidation process control is performed by the following technological parameters (mark the wrong answer).

A. Oxidation temperature
B. Oxidation time
C. Velocity of the carrier gases
D. Steam concentration
E. Impurity concentration in the carrier gases

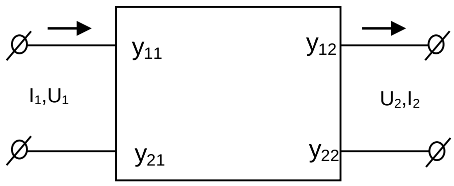
4a85. For different circuit applications, a bipolar transistor is presented in the form of quadruple, characterized by two current values I_1 and I_2 and two voltage values U_1, U_2.



the following are taken as input parameters for h-parameter system:

A. U_1, U_2
B. I_1, I_2
C. I_2, U_1
D. I_1, U_2
E. U_1, I_2

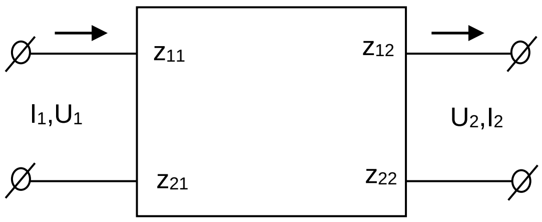
4a86. For different circuit applications, a bipolar transistor is presented in the form of quadruple, characterized by two current values I_1 and I_2 and two voltage values U_1, U_2.



the following are taken as output parameters for y-parameter system:

A. U_1, U_2
B. I_1, I_2
C. I_1, U_2
D. I_2, U_1
E. U_1, I_2

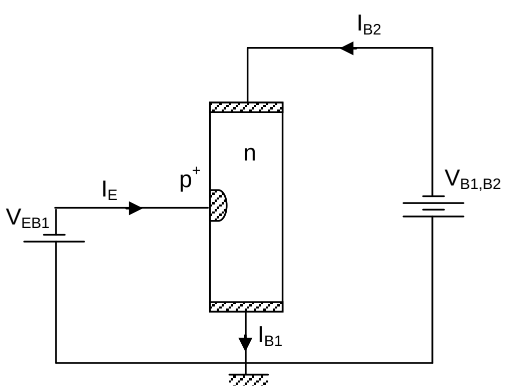
4a87. For different circuit applications, a bipolar transistor is presented in the form of quadruple, characterized by two current values I_1 and I_2 and two voltage values U_1, U_2.



the following are taken as input parameters for z-parameter system:

A. U_1, U_2
B. I_1, U_2
C. I_1, I_2
D. I_2, U_1
E. U_1, I_2

4a88. What is the reason for the occurrence of negative differential conductance region on the emitter current I_e dependence on base voltage V_{EB1} in case of a single junction transistor?



A. P^+ - n-junction breakdown
B. Strong injection of holes into base
C. Electron injection from ohmic B_1-contact
D. Impact ionization phenomena in the base
E. A. and C. answers are correct

4a89. Which are majority carriers in p – type semiconductors?

A. Electrons
B. Holes
C. Ions
D. Electrons and holes
E. Electrons, holes and ions

4a90. Which are majority carriers in n – type semiconductors?

A. Electrons
B. Holes
C. Ions
D. Electrons and holes
E. Electrons, holes and ions

4a91. What domains does a semiconductor diode consist of?

A. Only p
B. Only n
C. p and n
D. Only p+
E. Only n+

4a92. What types of carriers do intrinsic semiconductors have?

A. Electrons
B. Holes
C. Ions
D. Electrons and holes
E. Electrons, holes and ions

4a93. Which semiconductor material is most used in computers, electronic devices, integrated circuits?

A. Ge
B. Si
C. GaAs
D. InS
E. AlGaAs

4a94. By inserting what atom materials in silicon, n-type conductance can be obtained?

A. Univalent
B. Bivalent
C. Quadrivalent
D. Trivalent
E. Quinquivalent

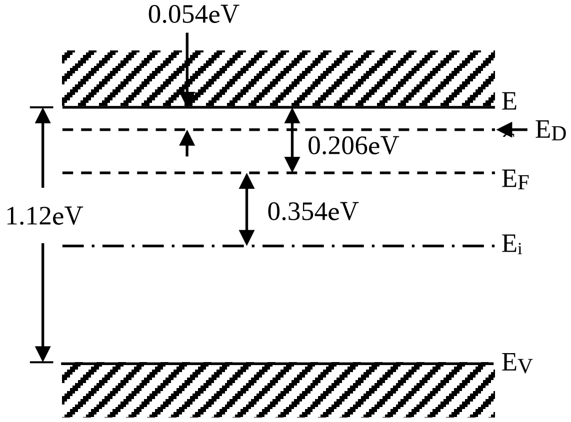
4a95. By inserting what atom materials in silicon, p-type conductance can be obtained?

A. Univalent
B. Bivalent

- C. *Quadrivalent*
- D. *Trivalent*
- E. *Quinquivalent*

4a96. The II phase of diffusion (deposition) provides:
- A. *High surface concentration and large depth of impurities*
- B. *High surface concentration and shallow depth of impurities*
- C. *Low surface concentration and large depth of impurities*
- D. *Low surface concentration and shallow depth of impurities*
- E. *Low surface concentration of impurities*

4a97. Figure shows the band structure of the following materials:

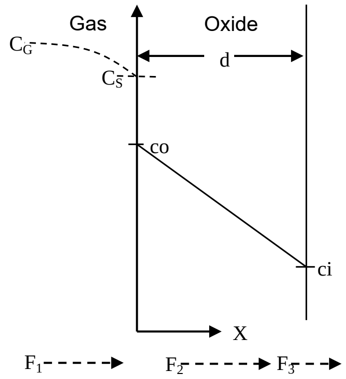


- A. *Metals*
- B. *n–type semiconductors*
- C. *p–type semiconductors*
- D. *Insulators*
- E. *i–type semiconductors*

4a98. The semiconductor diffusion process control is performed by the following technological parameters (mark the wrong answer).
- A. *Diffusion temperature*
- B. *Diffusion time*
- C. *Velocity of the carrier gases*
- D. *Steam concentration*
- E. *Impurity concentration*

4a99. What kind of structural defect is dislocation?
- A. *Shottky*
- B. *Linear structural*
- C. *Frenkel*
- D. *Surface structural*
- E. *Volume structural*

4a100. What are the silicon thermal oxidation processes (fluxes F1, F2, F3 in Figure) for limiting the oxidation rate?



- A. *Flux F_1 of oxidizing species transported from the gas phase to the gas-oxide interface*
- B. *Flux F_2 across the existing oxide toward the silicon substrate*
- C. *Flux F_3 reacting at the Si-SiO_2 interface*
- D. *Fluxes F_1 and F_3 simultaneously*
- E. *Fluxes F_1 and F_2 simultaneously*

4a101. What phenomena are not observed in extrinsic semiconductor under the influence of external high electric and magnetic fields?
- A. *Auger recombination*
- B. *Auger generation*
- C. *Tunneling ionization of impurity atom*
- D. *Electrons outer emission*
- E. *Band gap energy decreasing*

4a102. At induced radiation a radiated photon and a stimulating photon have similar
- A. *Frequencies and phases only*
- B. *Polarization and frequencies only*
- C. *Propagation direction only*
- D. *Wavelengths only*
- E. *All above mentioned*

4a103. The product of electron and hole concentrations in extrinsic semiconductor
- A. *Depends on Fermi level*
- B. *Is independent of temperature*
- C. *Is independent of impurity concentration*
- D. *Is independent of band gap energy*
- E. *Is independent of electron effective masse*

4a104. At low temperature range lattice thermal capacity of a metallic crystal with temperature increasing

A. *Decreases by exponential law*
B. *Increases by exponential law*
C. *Increases by linear law*
D. *Increases by cubic law*
E. *Decreases by linear law*

4a105. What is a potential well?

A. *Energetic state for which a certain minimum energy is required for the particle to escape it*
B. *Dimensional space which the particle can escape if acquires maximum energy*
C. *Limited space where the state energy of the particle is less than its maximum transfer energy*
D. *Limited space from all sides*
E. *All the answers are correct*

4a106. What is quantum tunneling?

A. *The process of particle transition from low to high energetic state*
B. *The process of passing particle through potential barrier when its energy is less than the height of barrier*
C. *The process when the particle changes its energetic state in potential well*
D. *The process when the particle moves above potential barrier*
E. *None of the above*

4a107. What is the result of the Schrödinger equation solution?

A. *Time-dependent potential energy of microparticle*
B. *Coordinate-dependent potential energy of microparticle*
C. *Probability of microparticle transitioning from potential well*
D. *Object extension level at some direction*
E. *Energetic spectrum of microparticle and probability density of microparticle detection at x point of space*

4a108. What is quantum phenomenon?

A. *Dependence of object properties on dimensions*
B. *Dependence of object properties on dimensions when object dimensions are equal to de Broglie wavelength at least in one direction*
C. *Quantization level of microparticle energy dependence on potential well parameters*
D. *Electron wave interference dependence on the boundary of nanoscale environment division*
E. *All the answers are correct*

4a109. What is superlattice?

A. *A system of closely distributed parallel quantum holes between which tunneling is possible*
B. *A system separated by macroenvironments*
C. *An environment with quantum dots*
D. *An environment with high density of quantum states*
E. *A. and B. are correct*

4a110. What is the advantage of double heterojunction lazers conditioned by?

A. *Occupation of dimensional energetic levels by charge carriers, injected by direct current*
B. *Dependence of valence and conduction region edges on x in case of nanoscale-thick active layer*
C. *Value of active layer refraction index*
D. *Spatial condensation of nonequilibrium charge carriers in intermediate active layer and their reunion conditioned by increase of radiation intensity*
E. *Potential barrier transitioning of microparticle with energy lower than barrier*

4a111. What processes are involved in the formation of nonequilibrium electroconduction in a semiconductor?

A. *Electron-hole pairs reunion, accompanying their photogeneration*
B. *Achieving maximum values of the nonequilibrium electron and hole densities in dynamic balance state*
C. *Exponential decrease of nonequilibrium charge carrier densities at switching off the light*
D. *Densities of nonequilibrium charge carriers remain constant after reaching dynamic balance*

while light exposure is constant

E. All the above mentioned simultaneously

4a112. What is the process of p-n junction barrier formation conditioned by?

A. Diffusion of majority carriers into opposite region

B. Drift of minority carriers

C. Enrichment of p-n junction by mobile charge carriers

D. Formation of p-n junction electrical field

E. All the above mentioned

4a113. The gradual channel approximation for the MOS transistor's model is conditioned by: (E_x is a vertical electric field component in the channel, E_y is a lateral electric field component, L – channel length, t_{ox} – gate oxide thickness)

A. $E_x << E_y$

B. $E_x >> E_y$

C. $E_y L = E_x t_{ox}$

D. $E_y L >> E_x t_{ox}$

E. $E_y t_{ox} = E_x L$

4a114. What does the gate-substrate workfunction of a MOS transistor depend on?

A. The gate material and the gate oxide thickness

B. The gate material and the oxide charge

C. The positive or negative bias applied to the gate electrod

D. The gate material and the substrate doping

E. The substrate doping and the electric field in the channel

4a115. The strong inversion condition for a MOS transistor model is determined as:

A. The energy band curve at the substrate surface is equal to doubled bulk potential

B. The carrier mobility is constant

C. The gate voltage is equal to the flat band voltage

D. The gate-substrate workfunction is equal to zero

E. The bulk potential is greater than 0.8 V

4a116. What kinds of capacitances are there in SPICE model of MOS transistor?

A. The depletion and diffusion capacitances of the gate – source and the gate – drain p-n junction

B. The overlap gate – source, gate – drain capacitances and the junction capacitances

C. The gate – substrate, the gate – source, the gate – drain and the gate – channel capacitances

D. The gate – substrate, the gate – source, the gate – drain capacitances and the depletion and diffusion capacitances of the gate – source and the gate – drain p-n junction

E. The overlap gate – source, gate – drain capacitances and the parasitic capacitances of the insulating regions

4a117. Calculate the small-signal transconductance of a bipolar transistor, if collector current I_C = 5,2 mA.

A. 5.2 A/V

B. 200 mA/V

C. 2 mA/V

D. 38.5 mA/V

E. 520 mA/V

4a118. How does the threshold voltage of an n-MOS transistor change, if the substrate bias varies from 0 V to 2 V? The strong inversion potential PHI = 0,7 V, the body effect coefficient GAMMA = 0,2 $V^{1/2}$.

A. Increases at 0.16 V

B. Decreases at 0.14 V

C. Increases at 0.23 V

D. Increases at 0.42 V

E. Decreases at 0.26 V

4a119. An NMOS transistor starts to conduct when:

A. The potential difference between the drain and the source terminals is higher than the threshold voltage V_t

B. The potential difference between the gate and the source terminals is higher than the threshold voltage V_t

C. The potential difference between the gate and the drain terminals is higher than the threshold voltage V_t

D. The potential difference between the drain and the base terminals is higher than the threshold voltage V_t

E. None of the above

4a120. The drain induced barrier lowering happens because of:

A. *High gate voltage in an NMOS device*
B. *High drain voltage that contributes in reducing the threshold voltage*
C. *The decrease in current in the channel due to high drain voltage*
D. *All of the above*
E. *None of the above*

4a121. The static power is affected by many factors in CMOS ICs, some of these factors are:

A. *Temperature, threshold voltage, and supply voltage*
B. *The activity factor at which the circuit is switching, supply voltage, and threshold voltage*
C. *The capacitive load of the circuit, switching activity, and supply voltage*
D. *The temperature, the switching activity, and the variability in the threshold voltage*
E. *None of the above*

4a122. The basic MOS capacitor in a MOSFET device is made from

A. *Gate, Oxide Insulator and Semiconductor*
B. *Gate, Drain and Source*
C. *Two parallel metal plates*
D. *Gate and Ground*
E. *None of the above*

4a123. Compared to BJT's, the input impedance of a MOSFET transistor is:

A. *Much smaller*
B. *Much bigger*
C. *About the same value*
D. *Slightly bigger than a typical BJT device*
E. *None of the above*

4a124. In n-channel MOSFET, if large electric field is applied at the gate, electron channel build up occurs directly underneath the semiconductor oxide layer. This process is called:

A. *Accumulation*
B. *Inversion*
C. *Depletion*
D. *Enhancement*
E. *None of the above*

4a125. In MOSFETs , the transconductance (gm) is usually:

A. *Bigger than a bipolar device*
B. *Smaller than a bipolar device*
C. *Equal to a bipolar device*
D. *The ratio of drain current over drain-source voltage*
E. *None of the above*

4a126. Electron drift current density is given by $J_n = en\mu_n E$, where μn is defined as:

A. *Drift velocity in cm/s*
B. *Electron Mobility in* $cm^2/V\cdot s$
C. *Carrier extrinsic concentration in* cm^{-3}
D. *Conductivity in* $(\Omega\cdot cm)^{-1}$
E. *None of the above*

4a127. Can an atom function either as donor or as acceptor in the same material?

A. *No*
B. *Yes*
C. *Yes, if the valence is equal to three*
D. *Yes, if the valence is equal to six*
E. *The correct answer is missing*

4a128. There is one negative ion on crystal surface. Which hole will the ion gravitate to with more power?

A. *Hole inside the crystal*
B. *Hole outside the crystal in the same distance from the surface*
C. *Hole outside the crystal in twice the distance from the surface*
D. *The correct answer is missing*
E. *All answers are correct*

4a129. The crystal thickness is d, the concentration of free electrons n. How much will the concentration be if the crystal thickness is reduced ten times.

A. *Will increase ten times*
B. *Will decrease ten times*
C. *Will not change*
D. *Depends only on the width of sample*
E. *Depends only on the length of sample*

4a130. What is the the principle reason of unsolvability of Shredinger stationary equation in general form?

A. *Lack of a simple mathematical apparatus*
B. *The problem of many simultaneously interacting particles by quantum theory is in principle unsolvable*
C. *Number of interacting particles is not a sufficient*
D. *Particles do not interact with each other.*
E. *All the answers are correct.*

4a131. In crystal having ε =16 dielectric transparency due to hole-phonon interaction, the energy of the hole is doubled. How many times will the energy of the hole change if the dielectric transparency is equal to 1 (ε =1)?

A. *Will increase sixteen times*
B. *Will reduce sixteen times*
C. *Will remain unchanged*
D. *The question does not make sense*
E. *All the answers are correct.*

4a132. Why not just for the conductor, but also for non degenerate semiconductor, thermodynamics is the energetic distance of output operation from Fermi level to vacuum? In a semiconductor, the Fermi level lies in the forbidden zone and ther could be no particle in that level.

A. *An electron can leave a semiconductor only from the conductive domain*
B. *An electron can leave a semiconductor only from the valence domain*
C. *An electron can leave a semiconductor from both conductive domain and immediately valence domain*
D. *The correct answer is missing*
E. *All the answers are correct*

4a133. What is the value of Fermi energy for phonon and why?

A. *Fermi energy is equal to the bandgap*
B. *Fermi energy is equal to zero*
C. *Fermi energy is equal to half of the bandgap*
D. *Fermi energy is close to the bottom of conductivity region*
E. *Fermi energy is close to the top of conductivity region*

4a134. What is the open circuit voltage of photodiode conditioned by?

A. *Diffusion of majority carriers*
B. *Long-wave radiation*
C. *Injection of majority carriers*
D. *Height of potential barrier*
E. *All the answers are correct*

4a135. When increasing the intensity of rays, how will its absorption depnsity change in solid state?

A. *Will increase*
B. *Will decrease*
C. *Will remain the same*
D. *According to spectral range*
E. *The correct answer is missing*

4a136. Mainly which noises are decisive in diodes?

A. *Thermal*
B. *Fligerian*
C. *Fractional*
D. *Generation-recombination*
E. *All the mentioned noises*

4a137. Which mode of electron motion is called ballistic?

A. *When it moves with finite long wire*
B. *When there are no defects in the environment*
C. *When the wire length is less than the electron free run length*
D. *When the diameter of wire cutoff is less than the electron free run length*
E. *When the last two conditions occur*

4a138. What is the potential barriers value of p-n junction conditioned by?

A. *Diffusion of majority carriers from p- and n-domains*
B. *Fermi level difference of p-and n-domains*
C. *Ratio of electrons and holes mobility*
D. *The first two*
E. *All the answers are wrong*

4a139. The change of which structural parameter increases the performance of MOS field transistor?

A. *The increase of substrate width*
B. *The decrease of surface of gate contact*
C. *The decrease of channel length*
D. *The decrease of subgate insulator's thickness*
E. *The last two factors*

4a140. When is the tunnel effect efficient?

A. *When the particle is in a potential hole with great depth*
B. *When the potential barrier is much larger than the particle's wavelength*
C. *When barrier width is comparable to De Broglie wavelength*

D. *When the energy in not quantized in potential hole*
E. *All the answers are correct*

4a141. In what case is broadband spectral sensitivity possible in heterojunction photodiodes?
A. *When the ray is absorbed by broadband semiconductor surface*
B. *When there is great input resistance*
C. *When the ray is absorbed by narrowband semiconductor surface*
D. *When carriers' mobility is great*
E. *All the answers are correct*

4a142. If a shallow (full ionized) donor concentration increases twice in an n-type semiconductor, the concentration of conduction electrons will
A. *Increase twice*
B. *Decrease twice*
C. *Increase more than twice*
D. *Decrease more than twice*
E. *Not change*

4a143. Characteristic length for the manifestation of quantum effects is
A. *Electron diffusion length*
B. *Electron free path*
C. *Electron De Broglie wavelength*
D. *Deby screening length*
E. *Lattice constant*

4a144. Photon gas is degenerated at
A. *Low temperature range*
B. *Very low temperature range*
C. *High temperature range*
D. *Very high temperature range*
E. *Any temperature range*

4a145. In the basics of degenerated and non-degenerated classification of an electron gas is the
A. *Pauli principle*
B. *Identity principle*
C. *Vegard's law*
D. *Detailed equilibrium principle*
E. *Heisenberg's uncertainty principle*

4a146. Which of the statements below are false for the varicap?
A. *Work of varicap is based on the phenomenon of the barrier capacitance of the p-n junction*
B. *Varicap works at forward bias of the p-n junction*
C. *Varicap capacitance depends on the applied voltage*
D. *Varicaps are used for the electrical tuning of resonant contours in the circuits*
E. *Varicap can operate at voltages less than a certain allowable voltages*

4a147. Which of the statements below is not true for stabilitron?
A. *Stabilitron is a semiconductor diode, the volt-ampere characteristic of which has a region of sharp dependence of current on voltage at the reverse branch of the characteristics.*
B. *The differential resistance of an ideal stabilitron in stability region of voltage is close to zero*
C. *Voltage of stability depends on the physical mechanism of breakdown of the diode*
D. *For stabilitrons with a a tunneling mechanism of breakdown, the voltage of stability, as a rule, is less than for stabilitrons with avalanche breakdown mechanism*
E. *Stabilitron is a semiconductor diode, the volt-ampere characteristic of which has a region of current saturation*

4a148. To increase the steepness of the characteristics of the FET, it is necessary to (which statement is not true)
A. *Reduce the length of the channel and increase its width*
B. *Reduce the thickness of the gate dielectric*
C. *Use dielectric with low permittivity*
D. *For substrate use semiconductor with high mobility of free charge carriers*
E. *Increase the voltage on the gate of the transistor*

4a149. What region is missing in the forward branch of volt-ampere characteristics of a diode thyristor?
A. *Region of high resistance, corresponding to the close state*

B. Region of low resistance, corresponding to the open state
C. Region with negative differential resistance of S-type
D. Direct current region
E. Region, not observed in the static volt-ampere characteristics of a thyristor

4a150. The equation for r_{ds} in triode mode operation using Shichman-Hodges MOSFET model is the following:

A. $r_{ds} = KP\frac{W}{L}*\frac{(U_{gs}-VTO)}{2}$

B. $r_{ds} = [\ KP\frac{W}{L}(U_{gs}-VTO)\ ]^{-1}$

C. $r_{ds} = [\ KP\frac{W}{L}*\frac{(U_{gs}-VTO)}{2}\ ]^{-1}$

D. $r_{ds} = KP^{-1}\frac{L}{W}$

E. $r_{ds} = KP\frac{W}{L}(U_{gs}-VTO)$

4a151. The specific contact resistance for the ohmic contact depends on:
A. Contact area
B. Substrate doping concentration
C. Contact potential difference φ_k
D. All the answers are correct
E. The correct answer is missing

4a152. Advantage of Schottky diode over conventional p-n-junction diode is in:
A. Smaller chip area
B. Smaller forward-bias voltage drop at the same current level
C. Smaller reverse-bias current
D. All the answers are correct
E. The correct answer is missing

4a153. Retrograde well doping distribution is important for:
A. Decreasing the IC cost
B. Suppressing the latch-up effect
C. Decreasing the IC chip area
D. All the answers are correct
E. The correct answer is missing

4a154. What is the occurrence of contact phenomena in semiconductors conditioned by?
A. Removal of electron from material
B. Substitution of free charge carriers by contact
C. Output operation of materials, creating contact
D. Mobility of free charge carriers
E. A. and B.

4a155. What is the difference of external and thermodynamic output operations of a material?
A. Fermi level and mix level difference
B. Valence band and vacuum level difference
C. Conductivity band bottom and vacuum level difference
D. Conductivity band bottom and Fermi level difference
E. All the answers are wrong

4a156. How does the domain diagram of near-surface region change at creating metal – isolator – n – semiconductor contacts when the operation of metal output is larger than the operation of semiconductor output?
A. The energy of electron increases in depletion layer when approaching the contact boundary
B. The energy of electron decreases in depletion layer when approaching the contact boundary
C. The energy of electron does not change in depletion layer when approaching the contact boundary
D. A. and B. are correct
E. None of the answers is correct

4a157. When is metal – semiconductor near-contact layer closed?
A. When in semiconductor near-contact layer the density of majority carriers is smaller than in volume
B. When in semiconductor near-contact layer the density of majority carriers is larger than in volume
C. When in semiconductor near-contact layer and in volume the densities of majority carriers are equal
D. When A. and B. occur
E. All the answers are wrong

4a158. What is the difference of p-n junction and closing contact of metal-semiconductor?
A. Properties of closing contact of metal-semiconductor can be controlled only

by semiconductor, whereas the one of p-n junction by p and n domains

B. It is practically impossible to create an ideal metal-semiconductor contact, and it is possible to create p-n contact

C. The current in metal-semiconductor contact is conditioned by majority carriers and piling of minority carriers does not occur, the opposite in the semiconductor

D. A. and B. are correct

E. A.,B. and C. are correct

4a159. What physical phenomena is in the base of semiconductor strainometer?

A. During semiconductor distortion, change in its specific resistance

B. During semiconductor distortion, change in mobility of charge carriers

C. During semiconductor distortion, increase of response time of charge carriers

D. During semiconductor distortion, change in diffusion length of charge carriers

E. All the answers are wrong

4a160. What is the frequency property of photoreceiver characterized by?

A. Photosensitivity dependence from frequency of radiation modulation

B. Photosensitivity dependence from pulse duration of radiation

C. Spectral sensitivity short channel boundary

D. A. and B. are correct

E. A.,B. and C. are correct

4a161. What are the components of a differential capacitor of MOS structure?

A. Geometrical capacitance of an isolator

B. Capacitance, driven by surface charges

C. Capacitance, driven by volume charges

D. A. and B. are correct

E. A.,B. and C. are correct

4a162. Which MOS device is likely to show the most leakage?

A. Low threshold voltage (Vth) device at 25ºC

B. High Vth device at 100ºC

C. Low Vth device at 100ºC

D. High Vth device at 25ºC

E. Not predictable

4a163. What is the thermodynamic output operation of material?

A. Impurity level and Fermi level difference

B. Top of the valence band and vacuum level difference

C. Fermi level and vacuum level difference

D. Bottom of conductance region and vacuum level difference

E. All the answers are correct

4a164. When is metal–semiconductor contact ohmic?

A. When near the contact, in thin layer of a semiconductor, in comparison to volume, the density of majority carriers is small

B. When the density of majority carriers in close to contanct layer of a semiconductor is high, in comparison to volume

C. When the density of majority carriers is the same everywhere

D. When A and C occur

E. When B and C occur

4a165. What is an optical subtractor?

A. A device to connect separate edges of optical cable

B. A device to modify optical signal

C. A register of optical signal power

D. A and B

E. All the answers are correct

4a166. What is the opposite branch of volt-ampere characteristics of a diode conditioned by?

A. Majority charge carriers

B. Minority charge carriers

C. Electrons and holes

D. Output operation of a semiconductor

E. All the answers are correct

4a167. What is optical pumping?

A. Process inverting the population in active laser environment

B. Means of extraction of laser bean

C. Mean for directing laser bean

D. A process of reunion of charge carriers

E. All the answers are wrong

4a168. What mechanisms of light energy absorption occur in optoelectronic devices?

A. Intrinsic absorption
B. Contact absorption
C. Excitonic absorption
D. Absorption by means of optical oscillation of atoms of crystal cell
E. All the listed mechanisms

4a169. What is information transfer in optron implemented by?

A. Quantums of radiation in conditions of input and output galvanic isolation
B. Electrons – in conditions of input and output galvanic isolation
C. Electric field
D. Electron hole pairs
E. All the answers are wrong

4a170. Why is the lightdiode's radiation spectrum not strictly onewave?

A. Because radiation reunion of carriers occurs between two levels
B. Because radiation reunion of carriers occurs between electrons which are on one group of levels and holes which are in another group
C. Because spectral distribution of radiation, coming from diode changes
D. Because it is conditioned by injection of carriers
E. Because reunion is missing in p-n junction

4a171. Semiconductors:

A. Are conductors at normal temperatures
B. Are conductors at low temperatures
C. Are dielectrics at normal temperatures
D. Are semimetals at low temperatures
E. Carry electric current in one direction only

4a172. Doping a semiconductor by donor impurities:

A. Fermi level shifts towards valence band
B. Fermi level is not changed
C. Fermi level shifts towards conduction band
D. The number of valence band holes is increased
E. The number of conduction band electrons is decreased

4a173. Atom vibration quantum in atomic crystal is called:

A. Exciton
B. Plasmon
C. Phonon
D. Polariton
E. Fermion

4a174. Momentum of electron which moves in crystal periodic field:

A. Is conservated
B. Has discrete values
C. Is independent of electric field
D. Varies in finite range
E. None of the above

4a175. Reciprocal capacitance of two parallel PCB wires in adjacent layers of multilayer devices depends on:

A. Dielectric permittivity of PCB wire
B. PCB wire width
C. PCB wire length
D. Dielectric layer thickness
E. All

4a176. t_i- pulse duration, the pulse time of which is t_1 . $t_1 < t_i$, in case of conducting by ℓ length PLC, the PCB wire is considered to be short if.

A. $\ell < t_1 \cdot c$
B. $\ell < t_h \cdot c$
C. $\ell < (t_1 + t_i) \cdot c$
D. $\ell < t_i \cdot c/\sqrt{\varepsilon}$
E. $\ell < t_1 \cdot c/\sqrt{\varepsilon}$

where c-light velocity in vacuum, ε – relative permittivity of dielectric.

4a177. Which of the PCB design issues is also an electronic design issue?

A. Calculation of PCB dimensions
B. Calculation of the mechanical strength

C. Calculation of permissible currents and voltages
D. Calculation of mechanical resonance frequency
E. None of the above

4a178. IC impermeability is estimated by:
A. Pressure value inside the body
B. Impermeability time constant
C. Electric field value inside the body
D. Power consumption
E. Supply voltage change

4a179. Which of the listed means is more efficient to protect against IC humidity?
A. Pointing the bodies
B. Varnishing the bodies
C. Impermeable body
D. Pumping air
E. Using dehumidifiers

4a180. Bipolar /p-n junctions/ transistor's emitter I_e , collector I_c and base I_b currents are related as follows:
A. $I_c = I_e + I_b$
B. $I_e = I_c + I_b$
C. $I_b = I_c + I_e$
D. $I_c = I_e + 2I_b$
E. $I_c = I_e - 2I_b$

4a181. Bipolar /p-n junctions/ transistor's base current transfer β and emitter current transfer α coefficients are related as follows:
A. $\beta = \frac{\alpha - 1}{\alpha}$
B. $\alpha = \frac{\beta - 1}{\beta}$
C. $\beta = \frac{\alpha}{\alpha - 1}$
D. $\beta = \frac{\alpha}{1 - \alpha}$
E. $\alpha = \frac{\beta}{\beta - 1}$

4a182. Barrier capacitance of semiconductor p–n junction occurs:
F. In case of direct connection
G. In case of reverse connection
H. Only in case of parallel connection
I. Only in case of series connection
J. Such capacitance does not exist

4a183. Select the statement which does not refer to a powerful MOS transistor:
A. the driver capability is weak
B. injection of the minority carriers is not present
C. thermoresistance is weak as a result of their self-heating
D. absence of the secondary breakdown
E. the effect of changing the input capacitance is characteristic

4a184. The following are not electrophysical properties of the powerful bipolar transistor domain:
A. Polarity of conductivity
B. Specific resistance
C. Mobility of charge carriers
D. Lifetime of charge carriers
E. Width of the domain

4a185. To improve the switching speed of PN diode it is necessary to
A. increase minority carrier lifetime
B. decrease minority carrier lifetime
C. decrease Maxwell relaxation time
D. increase carrier free path time
E. the true answer is absent

4a186. The external work function of a semiconductor depends on
A. surface crystallographic plane
B. surface states
C. Fermi level location
D. chemical nature of absorbed atoms
E. all the above-mentioned answers are true

4a187. In metal-semiconductor contact, what main processes of (carrier transmission) are there?
A. Over barrier transition
B. Quantum-mechanical tunneling through barrier
C. Reunion of charges in the layer with special charges
D. Hole injection from metal to semiconductor
E. All the mentioned processes occur simultaneously

4a188. When does the diffusion theory appear in Shotki barrier?
A. When the barrier height is much higher than thermal energy
B. When the dissipation of electrons during movement in depletion layer plays significant role

C. When the density of charge carriers in the beginning and in the end of the barrier does not depend on the current, i.e. coincides with its equivalent values
D. When the density of charge carriers in a semiconductor is small and degeneration is missing
E. When all the conditions are present

4a189. When does thermo-electronic emission occur by Schottky barrier?

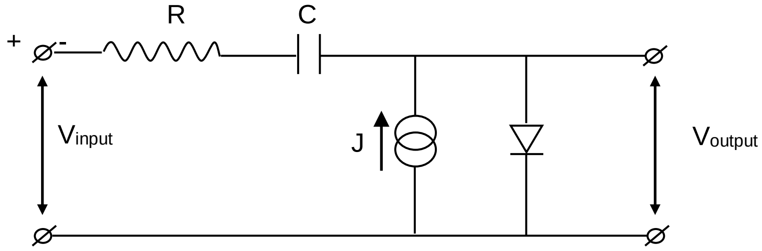
A. When the barrier height is much higher than thermal energy
B. When the domain of thermoelectronic emission is in in thermodynamic equilibrium
C. When the transition of total current does not violate that equilibrium
D. When condition A does not occur
E. When A., B. and C. occur simultaneously

b) Problems

4b1.

Semiconductor diode is often used in reducers as a variable resistor (see the circuit). In that case the diode's bias is given by means of J constant current source, and the connection between input and output signals is realized by the help of C capacitance, the reactive resistance of which is relatively smaller compared with R resistance.

Calculate and draw the dependence on J current expressed in decibels according to voltage signal depletion ($20\lg(V_{output}/V_{input})$), when the current ranges from 0.01 mA to 10 mA. Use $R=10^3$ Ohm in calculations, and diode saturation current $J_s=10^{-6}$ A.



4b2.

Calculate the capacitance of p-n junction that is characterized by linear distribution of impurities: $N_A - N_D = kx$, where $k = 10^{10}$ m^{-1}, $\varepsilon\varepsilon_0 = 200$ pF/m, junction area $A=10^{-7}$ m^2, the difference of contact potential Ψ= 0.3V, and the opposite deflection V= 5V.

4b3.

Field transistor's n –channel of p^+-n - junction is characterized by arbitrary distribution of channel width impurities $N_D(x)$. Show that the transconductance of a such transistor $\rho_m = \dfrac{\partial I_D}{\partial V_G}$ equals $\rho_m = \dfrac{2z\mu}{L}\left[Q(h_2) - Q(h_1)\right]$, where h_1 and h_2 are depletion layer widths at source and drain, accordingly, and $Q(y) = e\int_0^y N_D(y)dy$, z is channel width, L – its length, and $\mu = const$ - electron mobility.

4b4.

The semiconductor, the Holy constant of which equals $3.33 \cdot 10^{-4}$ m/Cl, and specific resistance $8.93 \cdot 10^{-3}$Ohm.m, is located in magnetic field, the induction of which equals 0.5 Tl. Define the Holy angle.

4b5.

On the photovoltaic cell, the integral sensibility of which is 100 uA/lm, 0.15 lm light flow falls. Resistor with 400 kOhm resistance is successively connected to the photovoltaic cell, the signal on which is given to the amplifier, which in its turn is controlled by 10 mA current and 220 V voltage controlling relay. Define the gain constant according to voltage and power.

4b6.

The ideal diode the opposite saturation current of which is 8 uA, is successively connected to 10 V emf and 1 kOhm resistor. At room temperature define diode's direct current and voltage drop on it.

4b7.

In a field transistor, the maximum value of channel current equals 2 mA, gate cutoff voltage - 5 V. Define channel current and slope of transistor characteristic in case of the following voltage values of the gate: a) -5 V, b) 0 V, c) -2,5 V.

4b8.

Silicon p-n junction is given. Define p-n junction layer's

a) d_p and d_n widths of both common *d* and *p* & *n regions*,

b) contact φ_c difference of potentials,

if the following is known: intrinsic charge density of silicon $n_i = 1{,}4 \cdot 10^{10}$ cm^{-3}, dielectric transparency of vacuum $\varepsilon_0 = 8{,}85 \cdot 10^{-14}$ F/cm, dielectric transparency of silicon $\varepsilon = 12$, electron charge $q = 1{,}6 \cdot 10^{-19}$ coulomb, Boltzmann constant $k = 1{,}38 \cdot 10^{-23}$ J/ ^{0}K, temperature $T = 300K$, conductances in n and p regions $\sigma_n = 10$ Ohm.cm and $\sigma_p = 5$ Ohm·cm, mobility of electrons and holes $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, $\mu_p = 500 \frac{cm^2}{V \cdot v}$:
Impurity atoms in the given temperature are considered fully ionized.

4b9.
Define silicon ideal p-n junction photodiode's
a) j_S density of saturation current,
b) open circuit $V_{o.c}$ voltage,

If the following is given: $n_i = 1{,}4 \cdot 10^{10}$ cm^{-3}, $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, $\mu_p = 500 \frac{cm^2}{V \cdot v}$, $kT = 0{,}026$ eV, $q = 1{,}6 \cdot 10^{-19}$ q, $N_d = 10^{15}$ cm^{-3}, $N_a = 5 * 10^{15}$ cm^{-3}, $L_n = 100$ um, $L_p = 60$ um, absorption coefficient $\alpha = 10^3$ cm^{-1}, base width $W = 100$ um, external quantum output $\beta = 0.7$, light sensitive area $S = 10^{-4}$ cm^2, intensity of absorbed rays[a] $\Phi = 10^{18} \frac{q}{cm^2 \cdot V}$. Assume that the impurity atoms are ionized.

4b10.
Field effect silicon transistor with n-type channel and contrary p-n junctions is given.
Define
a) h_1/h_2 ratio of h_1 and h_2 widths of the channel near the source and drain,
b) *cutoff voltage*,

if given: $\varepsilon = 12$, $\varepsilon_0 = 8{,}85 \cdot 10^{-14}$ F/cm, the voltage applied to p-n junction from the supply source of the drain, near the source $V_1 = 0{,}5$ V, near the drain $V_2 = 1$ V, the voltage applied to the gate V$_g$=0.5V, $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, $\rho_h = 5$ Ohm.cm, channel length $\ell = 10^{-2}$ cm, channel thickness $\alpha = 2{,}5 \cdot 10^{-4}$ cm, channel width $b = 10^{-2}$ cm.

4b11.
A field effect transistor with isolated gate is given which has built-in silicon n channel.
Define
a) C capacitance of the gate in depletion mode,
b) cutoff voltage V_{g0},

if given: thickness of isolator $d = 0{,}5 \cdot 10^{-4}$ cm, $\varepsilon = 12$, $\varepsilon_0 = 8{,}85 \cdot 10^{-14}$ F/cm, $\mu_n = 1300 \frac{cm^2}{V \cdot v}$, channel length $\ell = 10^{-2}$ cm, width $b = 10^{-2}$ cm, thickness $\alpha = 2 \cdot 10^{-4}$ cm, electron charge $q = 1{,}6 \cdot 10^{-19}$ cl, voltage applied to the gate |V$_g$|=3, voltage applied to the drain – 1V, density of energetic states in conducting band $N_C \approx 10^{19}$ cm^{-3}, position of Fermi level $E_C - E_F = 0{,}2$ V, thermal energy $kT = 0{,}025$ eV.

4b12.
The barrier capacitance of an abrupt p-n junction is 200pF, when 2V reverse bias is applied towards it. Wha t kind of reverse bias is required to apply in order to reduce its capacitance up to 50pF if the contact potential difference is $\varphi_k = 0.82$ V.

4b13.
The conductivity of n-type channel of a field effect transistor, controlled by p-n junction, is 32Ohm^{-1}m^{-1}. The channel width is w = 8 μm, when "gate-source" voltage equals zero. Find the "pinch-off" voltage of

transistor's channel if the mobility of electrons is 2000cm ^{2} /V.v, and the dielectric constant of the semiconductor equals 13.

4b14.
It is known that the electrical field in the short channel field effect transistor can reach up to several kV/cm, in case of which the carriers are "heated", and their mobility becomes dependent on the electric field strength ε. Considering that the dependence has the following form:

$$\mu = \frac{\mu_n}{1 + \frac{\varepsilon}{\varepsilon_c}}$$

(μ_n - low field mobility of electrons, ε_c -critical value of electrical field) find the drain current dependence on its and the gate's voltages. Also consider that the channel length, width and depth are given.

4b15.
Boron diffusion is provided from a "limited source" with the total amount of impurities $Q = 2{,}25 \cdot 10^{13}$ atom/cm^2 in $t = 2$ hour. Diffusion coefficient equals $D = 9{,}2 \cdot 10^{-13}$ cm^2/s. Diffusion is provided into the bulk silicon substrate with the impurity concentration $N_D = 1 \cdot 10^{16}$ atom/cm^3. Calculate the depth of p-n junction x_j in micrometers.

4b16.
Consider a $p^+ - n - p$ silicon transistor with doping levels of emitter, base and collector $N_{AE} = 5 \cdot 10^{18}$ cm^{-3}, $N_{DB} = 10^{16}$ cm^{-3}, $N_{AK} = 10^{15}$ cm^{-3}, base width $W = 1\ \mu$m, cross sectional area is 3 mm^2, and applied voltages are $U_{EB} = +0.5$ V, $U_{BK} = -5$V. Calculate the width of quasi-neutral part of the base, minority carriers' (holes) concentration near the emitter-base junction and total charge of minority carriers injected into the base (T=300K).

4b17.
Calculate the bipolar diffusion coefficient of current carriers in intrinsic GaAs at 300K if electron and hole mobilities are equal 8800cm^2/V.s and 400cm^2/V.s, correspondingly.

4b18.
Find the potential barrier's height existing for electrons in Schottky diode if the specific resistance of a semiconductor $\rho = 1$ $Om \cdot cm$, electrons' mobility 3900 $cm^2/V \cdot s$, gold work function $\varphi_{Au} = 5$ eV, semiconductor's electron affinity \` $\chi_{Ge} = 4$ eV, intrinsic concentration $n_i = 2.5 \cdot 10^{13}$ cm^{-3}, band-gap width $E_g = 0.66$ eV (T=300K).

4b19.
For an ideal p-n-p transistor, the current components are given by I_{ep}=3mA, I_{en}=0.01mA, I_{cp}=2.99mA, I_{cn}=0.001mA. Determine:

a) The emitter efficiency (γ),
b) The base transport coefficient (I_T),
c) The common-base current gain È$_0$ and I_{cB0}.

4b20.
In n-channel n$^+$-multicrystal S$_i$-S$_i$O$_2$-S$_i$ MOS transistor N_a=10^{17}cm^{-3}, (Q_{ox}/Q)=5*10^{11}cm^{-2}, calculate the threshold voltage V_T, if the oxide layer thickness is 5nm. What density of Bor ions is necessary to increase the threshold voltage up to 0.6V?

2ψ_B=0.84V, ε_{Si02}=3.9, ψ_S=-0.98V, ε_{Si}=11.9.

4b21.
Intrinsic Ge is in 3000 K temperature. How many percent will the specific conductance of the sample change if the temperature increases by 1%. Accept $\Delta E = 0.72 eV$.

4b22.

Given mobilities of electrons and holes $\left(\mu_n \text{ և } \mu_p\right)$– , find the concentration of charge carriers corresponding to minimal specific conductance.

4b23.

How will charge carrier’s lifetime in non-generated semiconductor change under the doped impurity concentration if it is known that T =3000K is constant, the mobility increases by 5%, and diffusion length decreases by 10 %?

4b24.

Using hydrogen atom model, calculate in semiconductor InSb crystal

a) donors’ ionization energy,

b) the radius of electrons in basic state,

c) the electron concentration density T = 4° K, when Nd = 1. 1014 cm^{-3}.

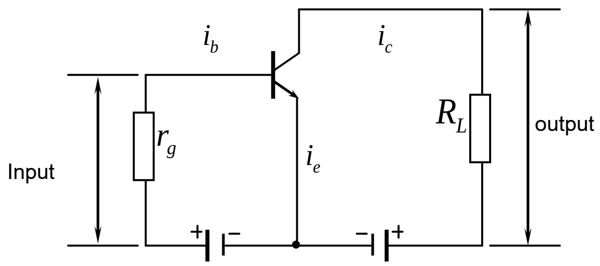
The radius of basic orbits is $r_H = 0.53\overset{o}{A},$ and bandgap of InSb Eg = 0.18eV, $\varepsilon_s = 17,\ m^* = 0.014 m_o,\ (m_o$ is free electron mass), $kT = 0.0258$ eV when T = 300 K, and ionization energy E_H = 13.6 eV.

4b25.

What number of electrons must pass from one metal to another for Vk=1V contact potential difference to occur between them when the width of dielectric between metals is d=10^{-9} m, $\varepsilon_o = 8.85 \cdot 10^{-14}$ F/cm. Compare the amount when there is metal-n type semiconductor contact for the same condition when in the surface of metal, concentration of electrons is $n_{sm} \approx 10^{25}$ c^{-2}, and in semiconductor $n_{ss} \approx 10^{10}$ cm^{-2}.

4b26.

A (n - p - n) transistor circuit connected by general emitter is shown. Calculate, according to power, amplification coefficient if $\alpha = 0.98,\ r_e = 20$ Ohm, $r_b = 500$ Ohm, $R_L = 30$ kOhm.



4b27.

In an intrinsic semiconductor electron concentration is 1.3×10^{16} cm^{-3} at 400K and 6.2×10^{15} cm^{-3} at 350K. Determine the forbidden band gap of material if it changes linearly via temperature.

4b28.

Determine the holes distribution in the n-type thin and long non-degenerated germanium wire in the case of point stationary injection of holes at point $x = 0$. Electric field intensity applied on the sample is $E = 5$ V/cm, temperature is $\mathrm{T} = 300$ K, hole diffusion length is $\mathrm{L_p} = 0.09$ cm.

4b29.

From the plane $x = 0$ of homogeneous half-infinite ($x \geq 0$) n-type semiconductor injected holes are stationary. Determine hole current density at x=0 point if $\Delta \mathrm{p}(0) = 10^{13}$ cm^{-3}, hole diffusion length is $\mathrm{L_p} = 0.07$

cm, hole diffusion coefficient is $D_p = 49$ cm^2/s, injection coefficient is $\xi = 0.4$. Non-equilibrium carrier drift is neglected.

4b30.

The N type silicon sample has 4mm length, 1,5mm width, 1mm hight and 80 Ohm resistivity. Determine the acceptor concentration of the sample if 0.12m^2/Vc and 0.025m^2/Vc are the electron and hole mobilities, respectively, 2.5×10^{16}m^{-3} is the intrinsic concentration of current carrier.

4b31.

In the photodetector by surface p-n junction, the width of active layer, creating photocurrent, is d=1um, F=10^{14}quantum/cm^2·s, by α = 10^4cm^{-1} and α = 10^3cm^{-1} absorption coefficients, double wave (λ_1 and λ_2) radiation ($h\nu \geq E_g$) are absorbed by photosensitive surface. Calculate the photocurrent ratio, created by those two wave absorption if photosensitive area is S = 10^{-4} cm^2, quantum output β =1, electron charge q=1.6·10^{-19}c.

4b32.

Define the performance of photodiode if volume charge layer width is d=10^{-4} cm, maximum speed of carriers' movement V_{max} = 5·10^6 cm/s, electron density in n-type base n = 5·10^{15}cm^{-3}, mobility μ_n = 1,3·10^3 cm^2/V·s, diffusion coefficient of minority carriers - holes D_p= 15,6 cm^2/v, Holes mobility in base μ_p = 600 cm^2/Vv, electron charge q = 1.6·10^{-19}c, base width w = 3·10^{-3}cm, photosensitive area S = 10^{-2} cm^2, dielectric permeability of semiconductor ε = 12, vacuum ε_0 = 8.86·10^{-14} f/cm.

4b33.

Define power density equivalent to photodiode noise if dark and light current sum $I=I_d+I_L$=5,1·10^{-7}A, frequency band Δf =1Hz, absorption radiation power P = 10^{-6} Vt, photocurrent I_E=5·10^{-7}A, photosensitive surface S = 10^{-2} cm^2, electron charge q = 1.6·10^{-19}c.

4b34.

Define channel width shrinkage through p-n junction at the drain of field transistor, when source-drain domain affects are missing, V=+0.5 V voltage has been applied to the drain, dielectric permeability of channel material ε=12, vacuum ε_0=8.86·10^{-14} f/cm, contact difference of potentials φ=0.7V, donors' density in and n-channel N_d=5·10^{14}cm^{-3}, electron charge q = 1.6·10^{-19}c.

4b35

Calculate the drain current of an NMOS Si transistor according to the following conditions: threshold voltage V_t=1 V, gate width W=10 μm, gate length L=1 μm, thickness of oxide layer t_{ox}=10 nm, V_{GS}=3 V and V_{DS}=5 V. For calculation, use square model, surface mobility is 300 cm^2/V and V_{BS}=0 V. Also calculate g_m transconductance.

4b36

Define the space charge, the values of Q_{sc} charge and C_{sc} capacity for the following values of ϕ_s surface potential: ϕ_s=0; ϕ_s= ϕ_0; ϕ_s=2ϕ_0, for p- type of the silicon, ρ_{si}=10 Om·cm, μ_n=1500 cm^2/V·sec, μ_p=600 cm^2/V·sec, ε_s=11.8, ε_0=8.85·10^{-14} F/cm, n_i=1.6·10^{10} cm^{-3}.

4b37.

Define the surface-state charge density Q_{ss} for p- type silicon N_a=10^{18} cm^{-3}, T=300 K, according to the following values of surface potential: ϕ_s=0; ϕ_s= ϕ_0; ϕ_s=2ϕ_0. Surface states are evenly distributed N_{ss}=2·10^{12} cm^{-2}·eV^{-1}. Compare the value of Q_{ss} with the appropriate charge of surface-state charge Q_{sc}. ε_0=8.85·10^{-14} F/cm, ε_s=11.8, n_i=1.6·10^{10} cm^{-3}.

4b38.

The density of donor in semiconductor which contains only donor impurity, is N_d, and their energy level is E_d. Find out the density of free electrons if the Fermi level coincides with E_d.

4b39.

Under the influence of light, homogenous distributed exceed charge carriers with the concentration of Δn occurred in semiconductor. The density of minority charge carriers is 2.5·10^{20} m^{-3}, and initial speed decrease of the density is 2.8·10^{24} m^{-3}·sec^{-1}.

Define:

a. The lifetime of minority charge carriers;
b. The value of Δn after 2 μsec when the light source had already been turned off.

4b40.

The mobility of electrons is 0.38 $m^2/V\cdot sec$ in the germanium sample, and the mobility of holes is 0.16 $m^2/V\cdot sec$. The Holy effect is not seen in this sample. Which part of the current is conditioned by holes?

4b41.
As the concentration of impurity has changed, the mobility increased by 5% in non-degenerate semiconductor at constant temperature T=300 K, and diffusion length increased by 10%. How did the lifetime of charge carriers change?

4b42.
The concentration of donors is $N_d=2\cdot 10^{20}$ m^{-3} in germanium sample. The effective mass of electron is $m^*=1.57m_0$ (m_0 is electron mass in vacuum). It can be considered that donor is dispersive center with $5\cdot 10^{-2}$ μm of radius. Find out the mean free path and time as well as electron mobility if T=300 K.

4b43.
For the InSb crystal $\mathrm{E_g}=0.23$ is the forbidden gap, $\varepsilon=17$ is the dielectric permittivity, $\mathrm{m}=0.015\mathrm{m_0}$ is the electron effective mass. Determine the minimal concentration of donors when impurity band is originated.

4b44.
In the silicon with 300K temperature electron mobility is $\mu=1500$ cm²/Vc and electron effective mass is $\mathrm{m}=0.32\mathrm{m_0}$. Determine the electric field when band-to-band impact ionization takes place.

4b45.
Determine the coefficient of temperature expansion of semiconductor forbidden gap, if the product of electron and hole effective mass equals $0.235\mathrm{m_0}$, intrinsic carriers' concentration equals 2×10^{16} cm^{-3} at $\mathrm{T_1}=500\mathrm{K}$ and 8×10^{12} cm^{-3} at $\mathrm{T_2}=280\mathrm{K}$.

4b46.
Determine the energy of electron ε that is reflected from the atomic (100) planes of the cubic crystalline lattice with constant $a=4\overset{o}{A}$ when the reflection angle is $\theta=45^o$.

4b47.
Find silicon photodiode's idle state voltage if the radiation with $\mathrm{F_0}=10^{18}\ \frac{qv}{cm^2\cdot s}$ intensity is observed in the active region of *p-n junction.* The external quantum output is 1, reflection coefficient 0. Electron and hole mobility equal $\mu_n=1300\,\frac{cm^2}{V\cdot v}$, $\mu_p=500\,\frac{cm^2}{V\cdot v}$ respectively, diffusion length of minority carriers $L_n=10^{-2}$ *cm*, $\mathrm{L_p}=6*10^{-3}$ *cm*, electron charge $\mathrm{q}=1{,}6\cdot10^{-19}$ *K*, thermal energy $\mathrm{kT}=0{,}026$ eV. Also given densities of majority carriers in *n* and *p* domains $p_p=N_a=10^{15}$ cm^{-3}, $\mathrm{n_n}=\mathrm{N_d}=5*10^{15}$ cm^{-3}, density of intrinsic charge $\mathrm{n_i}=\mathrm{p_i}=1.4*10^{10}$ cm^{-3}:

4b48.
Given silicon *p-n* junction. The position of Fermi level in n region is $E_C-E_F=0{,}2$ eV, and in p region it is $E_F-E_V=0{,}1$ eV. Density of energetic states in conductance and valence regions $N_C=2.8*10^{19}$ cm^{-3}, $N_V=1.02*10^{19}$ cm^{-3}. Also given intrinsic carriers' density in a silicon $n_i=p_i=1.6*10^{10}$ cm^{-3} and room temperature energy $kT=0{,}026\,eV$. Define the contact difference of p-n junction potentials.

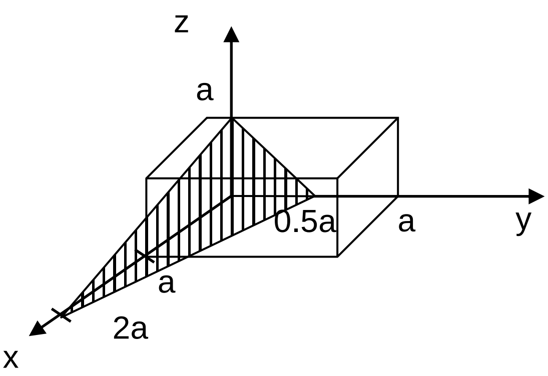
4b49.
Define the charge capacitance of silicon structure of two backward potential barriers if the depletion layers have symmetric distribution and contact edge. The total width of depletion layers $d=10^{-4}$ *cm*, and the area of *p-n junction* $S\approx10^{-4}$ cm^2. Accept the dielectric transparency of vacuum $\varepsilon_0=8.86\times10^{-12}$ *F/m*, and the one of Si $\varepsilon=12$.

4b50.

Barrier capacitance of p-n junction is C_1 = 100 pF for 2V backward bias voltage. What value will the capacitance take in case of decreasing *V* voltage twice? The height of potential barrier of *p-n* junction is φ = 0.6V.

4b51.

Determine Miller indices of the shaded plane in a cubic crystal.



4b52.

n-type silicon has the following sizes: length is 10mm, width is 2mm and thickness is 1mm. Mobilities for electron and hole are 0.12 and 0.05m^2/(V-s) respectively. The intrinsic carrier density is $n_i = 1.5 \cdot 10^{16}$ m^{-3} and the elementary charge is $q = 1.6 \cdot 10^{-19}$ C. Determine the donor impurities concentration N_d in the substrate when the resistance is R=150 Ω.

4b53.

Prove that semiconductor at the given temperature has minimum conductivity if the electron density is $n = n_i \sqrt{\mu_p / \mu_n}$. Here n and n_i are intrinsic densities and μ_p and μ_n are hole and electron motilities respectively.

4b54.

Conductivities of p and n regions for germanium p-n-junction are $\sigma_p = 10^4\ (\Omega \cdot m)^{-1}$ and $\sigma_n = 10^2\ (\Omega \cdot m)^{-1}$ respectively. Electron and hole mobilities are 0.39 and 0.19m^2/ (V-s), intrinsic carrier density is $n_i = 2.5 \cdot 10^{19}$ m^{-3} and elementary charge is $q = 1.6 \cdot 10^{-19}$ C.

Calculate the diffusion potential at T=300k.

4b55.

Silicon diode with saturation current $I_0 = 25\mu A$ operates at 0.1V forward voltage, when $T = 300k$. Determine the diode's DC resistance.

4b56.

In wet oxidation of silicon at 950^{0}C the following data are obtained:

t (hour)	0.11	0.30	0.40	0.50	0.60
do (oxide thickness in μm)	0.041	0.100	0.128	0.153	0.177

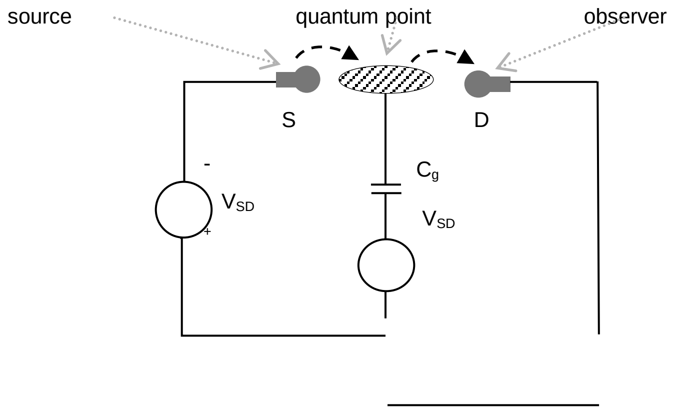
Show how to graphically determine the linear and parabolic rate constants from these experimental data.

4b57.

Boron diffusion is provided from a "limited source" with the total amount of impurities $Q = 2{,}25 \cdot 10^{13}$ atom/cm^2 in $t = 2$ hour. Diffusion coefficient equals $D = 9{,}2 \cdot 10^{-13}$ cm^2/s. Diffusion is provided into the bulk silicon substrate with the impurity concentration $N_D = 1 \cdot 10^{16}$ atoms/cm^3. Calculate the depth of p-n junction x_j in micrometers.

4b58.

The nanostructure of field transistor type consists of quantum point which is connected to two current conductors by tunnel current – electron's source and observer (Figure).



When VSD voltage is applied between the source and the observer, current starts to flow through the net which is conditioned by the tunnel junction of electrons from the source into the quantum point, and then from the quantum point to the observer.
The second electrode of the transistor - gate, Cg is connected to the quantum point by capacitive link and it is possible to control the current that flows through the source-quantum point – observer by the applied Vg voltage.
Considering that the quantum point is r=10nm radius, and the cut set of current source and observer are of the same type, estimate, due to Coulomb blockade, how much it is necessary to change the gate voltage such that from the source to the quantum point after one electron tunnel junction, the second, the third and other electrical tunnel junctions are possible, due to which I-V dependence will look as Coulomb degree.

4b59.

Considering the silicon photodiode as an ideal photoreceiver (i.e. by an internal quantum output equal to one) find current and voltage values in its output when the receiver operates in the mode of photocurrent on one hand, and photoelshu on the other hand. The photoreceiver operates in a room temperature T=300K, light P =10mVt power λ=0,8 um wavelength monochromatic light. It is known that backward bias current of the diode is I0=10nA.

4b60.

In p-n-p bipolar transistor base, donor mixtures are distributed nonhomogeneously - exponentially c $N_D = N_0 \, exp\left(-\frac{x}{L_0}\right)$, where L_0 is the length characterizing that distribution, W is the width of the base, and L_0<W. Estimate the tenseness of an internal electrical field in the base as well as the ratio of drift and diffusion times of moving through the hole base.

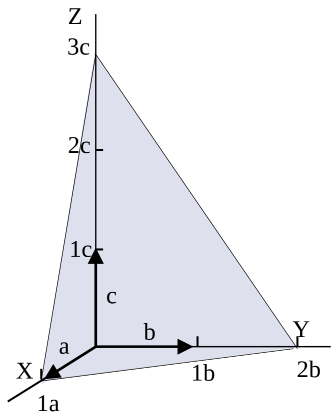
4b61.

At the moment of time t=0, voltage pulse is applied on the gate of metal-insulator-semiconductor /MIS/ - structure and as a result, it transitioned from equilibrium to unequilibrium state. Assuming that the transition into a new equilibrium state and the filling of surface potential well by minority carriers occurs through thermal generation of charge carriers through the centers, located in the middle of the semiconductor bandgap, find the relaxation time of MIS-structure in case of a constant gate charge. It is known that the speed of thermal generation is equal to ni / 2 τ_0, where ni is the intrinsic concentration of charge carriers, and τ_0 is the lifetime of minority carriers.

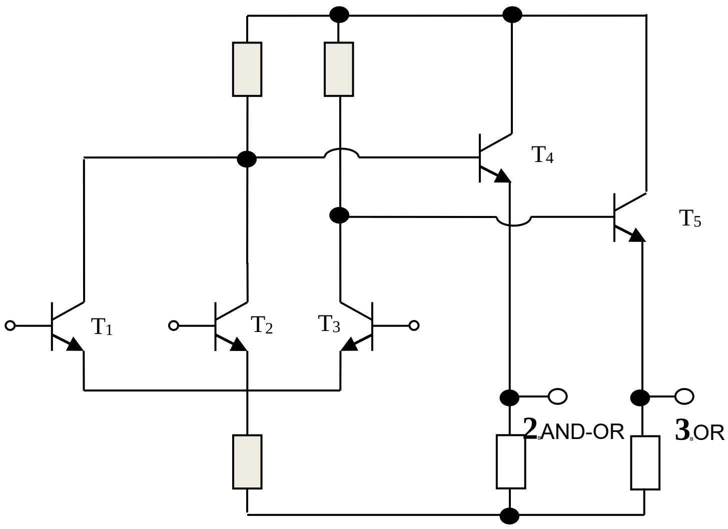
4b62.
At the moment of time t=0, voltage pulse is applied on the gate of metal-insulator-semiconductor - structure and as a result, it transitioned from equilibrium to unequilibrium state. Assuming that the transition into a new equilibrium state and the filling of surface potential well by minority carriers occurs through thermal generation of charge carriers through the centers, located in the middle of the semiconductor bandgap, find the relaxation time of MIS-structure in case of a constant gate voltage. It is known that the speed of thermal generation is equal to ni / $2\tau_0$, where ni is the intrinsic concentration of charge carriers, and τ_0 is the lifetime of minority carriers.
4b63.
Find the differential resistance of silicon p^+-n-p^+ transistor collector junction if N_A>>N_D, $N_D=10^{15}$ cm^{-3}, L_p=0.1 μm, base width W=30 μm, collector voltage U_k=5V, emitter current I_e=1mA, dielectric permittivity of semiconductor ε=11,8.
4b64.
Estimate the maximum temperature when $n-Si\ \left(N_d=10^{-15}cm^{-3}\right)$ can be used as a material with clearly expressed semiconductor features in semiconductor devices. For Si it is known that $E_g=1{,}11eV$, $m_{dn}^*=1{,}08\,m_0$, $m_{dp}^*=0{,}56\,m_0$.

4b65.
CsCl crystal lattice constant is a=4,11*10^{-10} m. Define d_{110}, d_{111} and d_{132} inter-surface distances.

4b66.
Find Miller indices of the shaded plane in a cubic crystal.



4b67.
The electrical schematic diagram of an emitter-coupled logic gate is shown. Prove at least how many isolation regions are necessary to form in the bulk semiconductor substrate for all the elements of the gate during its preparation.

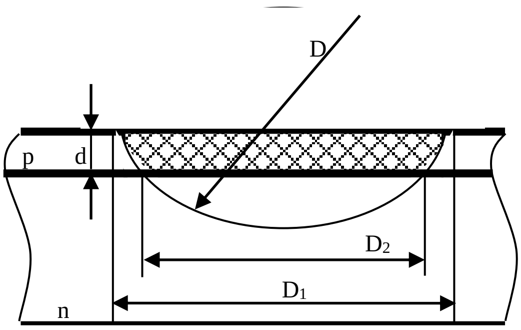


4b68.

The crystal resistance from PbS in 20^0C is 10^4 Ohm. Find its resistance in 80^0C. PbS bandgap is equal to 0.6 eV.

4b69.

Define P-N junction depth d, if during measurement by spherical metallographic section method D_1=3 mm; D_2= 2 mm and D=60 mm.



4b70.

Determine the angle between crystalline planes one of which has (121) Miller's symbols and the other plane passes though points A(5/8,3/8,7/8), B(7/8,5/8,3/8) and C(7/8,1/8,7/8).

4b71.

At T=0K Fermi energy in aluminum crystal is 11.63 eV. Calculate the number of free electrons per atom if aluminum lattice constant is 0.4 nm.

4b72.

Determine decay law of non-equilibrium carriers concentration in n-semiconductor if after turn off a source of band-to-band generation at instance t=0 the recombination temp is described by $R = \alpha_n(np - n_i^2)$ law, where $\alpha_n = const.$

4b73.

Determine frequency dependence of dielectric permittivity of plasma with free electron concentration n.

4b74.

On the background of noise, the photoreceiver is capable to register a ray with $F_1 = 10^5$qu/sm^2.s minimum intensity. From photosensitive surface, what maximum x_1 deepness and $d = x_1 - x_2$ width can the active region have to provide absorption of the remaining (10^5-1) quanta in the end of absorption, if the absorption coefficient of the wave is $\alpha = 10^6$ sm^{-1}, surface intensity is $F_0 = 10^{16}$ qu/sm^2.s. x_2 is the maximum penetration deepness of quanta with (F^0 – 1) number. In x_2, F_2 = 1 qu/sm^2.s.

4b75.

Given λ_1 = 294 nm and λ_2 = 299 nm length waves with α_1 = 2015894 sm^{-1} and α_2 = 1764193 sm^{-1} absorption coefficient respectively. The intensity of λ_2 is $F_{02} = 10^{16}$ qu./sm^2.s. Define the F_{01} intensity of λ_1 so that its intensity is $F_1(x_1)=2\ F_2(x_1) = 2.10^5$ qu/sm^2.v in x_1 penetration deepness of λ_2 (where λ_2 has recordable $F_2(x_1)=10^5$ qu/sm^2.v threshold intensity).

4b76.

Define the permittivity coefficient of rectangular potential barrier for electron (D_e) and proton (D_p) if the barrier width is d = 0,2 nm, the shortage of energy to overcome the barrier is $E^0 - E = 1$ eV, electron and proton masses are m_e= 9,1.10^{-31}kg, m_p= 1,67.10^{-27}kg, Plank constant $\hbar =$ 1,054.10^{-34} J.s, pre-exponential multiplier is D_0 = 0,2. 1eV = 1.6.10^{-19} J.

4b77.

A semiconductor is lit by rectangular pulse light. $\Delta\delta_{st}$ stationary photoconductance, occurred due to it, is characterized by stationary density of photogenerated electrons and holes ($\Delta n_{st}=\Delta p_{st} = 10^{10}$sm^{-3}).

At t_1 moment of time, after how much t_2-t_1 time when the light is switched off, $\Delta\delta_{st}$ stationary photoconductance will decrease twice if the lifetime of nonequilibrium charge carriers is $\tau = 10^{-6}$v, low $\Delta n \ll n_0+p_0$ level of lighting occurs, where n_0 and p_0 are equilibrium densities of electrons and holes.

4b78.

In Aluminum net, about 0.75 Ev energy is required to have a free place. How many free places are received to one atom of silicon in case of thermodynamic equilibrium if the temperature T_1 = 300ºK or T_2 = 600ºK.

4b79.

Show that in the conductor the probability that the electron can be found δ amount down from Fermi level is equal to the probability that the electron cannot be found δ amount upper from Fermi level.

4b80.

Show that for a simple two-dimensional square network, the free electron kinetic energy in the corner of the first zone of Brilluen is twice greater than in the middle of the edge side.

4b81.

In the conductor, find v_F Fermi velocity of electrons, accepting that there is one electron in elementary cell.

$E(\vec{k}) = E_o \cos k_x a$, where $E_o = 0.5$ Ev, and the net constant $a = 3\overset{o}{A}$.

4b82.

In a semiconductor with only donor impurity, the donor concentration is N_d, and their energy level is E_d. Find the concentration of free electrons, if the Fermi level coincides with E_d.

4b83.

A part of Germanium, doped with weak donors up to 10^{16} cm^{-3} is under the light effect, due to which 10^{15}cm^{-3} extra electrons and holes are generated. Calculate Fermi quasienergy with respect to the intrinsic energy and compare with Fermi energy in case of the lack of light.

4b84.

Consider p-n-p type transistor, doped 10^{18}cm^3 in the emitter and 10^{17}cm^3 in the base respectively. The width of quazi-neutal domain in the emitter is equal to 1 mkm and 0.2 mkm in the base respectively.

Note that μn = 1000 cm^2 N – s and μp = 300 cm^2 N – s. The lifetime of minority carriers in the base is equal to 10ns.

Calculate the efficiency of the emitter, the transfer coefficient of the base as well as the current coefficient of the base in active mode.

4b85.

Compute the mean free length of free electrons of natrium at room temperature if at that temperature the specific electroconductance is 2.3·10^7 Ohm^{-1} · m^{-1}, and the concentration of free electrons 2.5 · 10^{28} m^{-3}.

4b86.

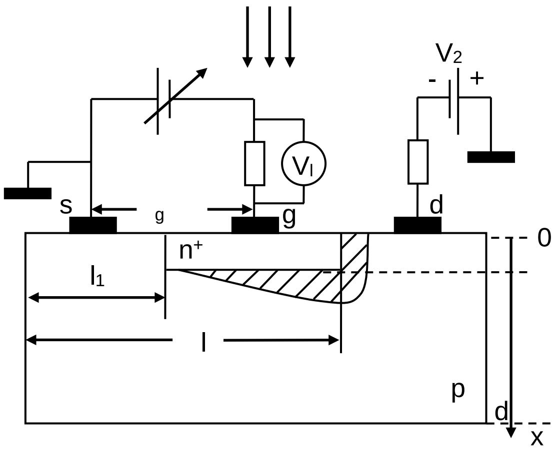
Get the dependence of relative $C(V)/C(0)$ change of charge capacitance of non-symmetric p-n junction from the applied external voltage when forward bias voltage changes from 0 to 0.5V. The potential value of the barrier of p-n junction is $\varphi_b = 0.6$ V. $C(V)$ is the capacitance of V voltage, and $C(0)$ in case of the lack of voltage.

4b87.

Given silicon FET by *p-n* junction (figure). The forward bias voltage, applied to the gate, eliminates the depletion layer in the beginning of *p-n* junction (w width of which is determined by $N_a = 5*10^{14}$ *cm³* density of impurities in the channel). It is assumed that along the channel, the negative potential, created by source drain voltage in the end of the l_1 length (in the beginning of *p-n* junction) is zero. How should the V potential be in the end of l length, so that in that point:

1. w width of depletion layer is equal to 100nm,
2. Depletion layer closes the channel with $d - d_n =$ 200nm width.

Accept the dielectric permittivity of a semiconductor is ε = 12, the one of vacuum ε_0 = 8.86·10^{-14} *f/cm*, the potential value of the barrier is $\varphi_b = 0.6$ V.



4b88.

Two λ_1 and λ_2 waves are absorbed in homogenous silicon with α_1 = 8·10^5 cm^{-1} and α_2 = 10^6 cm^{-1} absorption coefficient values respectively. The intensity of the first wave *is* F_{01}= 10^{15}qv./cm^2·v. How should the F_{02} intensity of the second wave be for them to have the same intensity in x = 0.5 mkm depth of absorption.

4b89.

Find the drift length of non-equilibrium holes in n- Si for T = 300K when the electric field tension is E = 10 V/cm, and the length of holes diffusion is L_p = 1.5·10^{-2} cm. kT = 0.025 Ev.

4b90.

A silicon p-n junction is initially biased at 0.60 V at T = 300 K, $eV/k_BT > 1$. Assume the temperature increases to T = 310 K. Calculate the change in the forward-bias voltage required to maintain a constant current through the junction.

4b91.

For the electron gas with concentration n at $T = 0$ temperature, determine the average kinetic energy of the electron with m mass.

4b92.

Holes are injected from plane $x = 0$ of long ($x \geq 0$) and non-degenerate n type semiconductor. Determine the distribution of steady-state excess hole concentration as a function of *x* when applied electric field is 8 V/cm; T= 300K, hole diffusion length is 0.04 cm.

4b93.

GaAs bulk material fabricated for the estimation of Hall-effect has dimensions d_x =0.5 mm, d_y=3mm, and d_z=10mm. The electric current is I_x=5 mA, the bias voltage is V_x=2.5 V, and the magnetic field is B=B_z =0.1 T.

The Hall voltage was measured to be V_H = −3.0 mV. Calculate the majority carrier mobility and the conductance. What is the conductivity type?

4b94.

Avalanche photodiode has a multiplication coefficient M = 20 at a wavelength of λ = 1.5mkm. The sensitivity of the photodiode at this wavelength is equal to R = 0.6 A/W, when the photon flux is $r_p=10^{10}$ photon/s. Calculate the quantum yield and the output photocurrent.

4b95.

At the surface of n-Si ($N_D=10^{16}$ cm^{-3}) at the value of the surface potential $\psi_S = 2\varphi_0$, where $\varphi_0 = \frac{E_F - E_i}{e}$ ($e\varphi_0$ - distance from the Fermi level to the center of the bandgap), a triangular potential well is formed in which the spectrum of heavy holes is quantized. Find the total number of two-dimensional holes in the first subband at T = 77K.

4b96.

The silicon transistor of n^+-p- n type has the effectiveness of an emitter γ=0.999, transfer coefficient through the base α_T=0.99, the thickness of the neutral base region W_b = 0.5 um, the concentration of impurities in the emitter $N_D=5{*}10^{19}$cm^{-3} , in the base $N_A=10^{16}$cм$^{-3}$, and in the colelctor - $N_D=5{*}10^{15}$cм$^{-3}$. Determine the threshold voltage on the emitter, at which the device ceases to be controlled and the puncture occurs. Calculate transit time through the base and the cutoff frequency.

4b97.

For what value of the voltage on metal electrode the flat-band condition is established in the p-type semiconductor of MOS structure, if the work function difference of the metal and semiconductor is equal to $\Delta\varphi_{m/p}$, the charge on the surface states is Q_{ss}, and the specific capacitance of the dielectric layer - C_{ox}.

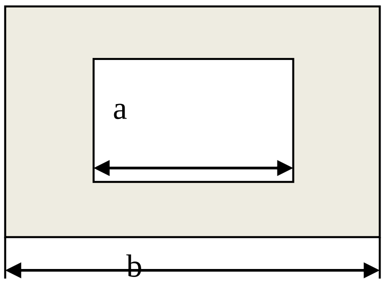
4b98.

Calculate n-MOSFET channel depletion layer width in strong inversion mode if substrate bias is V_{bs}=0 and -2V; substrate doping concentration in the channel region is $N_b=10^{16}$ cm^{-3}.

Additional data for calculation: T=300K; Si-substrate; φ_t=25.8 mV; $n_i=1.5\cdot10^{10}$ cm^{-3}; $\varepsilon\cdot\varepsilon_0$ = 1.1 pF/cm; e =$1.6\cdot10^{-19}$ C.

4b99.

Estimate the width and the length of a square annular NMOS transistor.



Gate geometry for square annular NMOS transistor.

4b100.

Calculate the zero-bias junction capacitance $C_j(0)$ for abrupt p-n junction. The doping density of the n-type region is $N_D = 10^{20}$ cm^{-3}, the doping density of the p-type region is $N_A=10^{16}$cm^{-3}. The junction area is S=1.5um x 1.5 um.

4b101.

Determine the type of die (core-limited or pad-limited) if the total cell area equals 49 mm^2, the total number of pads N_P is 128, the width of pad W_P equals 100 um and the minimum spacing between adjacent pads S_P is 100 um.

4b102.

Thickness of a field effect transistor's isolator with isolated gate is 2 nm, length of built-in silicon n-channel is $\ell = 30$nm, width $b = 20$nm, thickness a=10nm, and electron density $n = 10^{17}$ cm^{-3}.

How much will change specific electro conductance of the channel if V_{g1}=2V voltage, applied to the gate, increases by 1V. Mobility of electrons is $\mu_n = 1300$cm²/V·s, electron charge $q = 1{,}6 \cdot 10^{-19}$ Cl. Stationary density change of electrons $\Delta n = 10^{18}$ cm⁻³.

4b103.
Define the photocurrent density of silicon photoresistance with 1um thickness of base when the surface intensity of intrinsic wave, absorbed in it is 10^{18} quantum/cm².s. Wave absorption coefficient is 10^4cm⁻¹, quantum output β = 1, reflection coefficient R = 0,7. Electron charge $q = 1{,}6 \cdot 10^{-19}$ Cl.

4b104.
How many times will the ideal Schottky diode's current density change while the temperature increases by 50C from T= 300k, when the Schottky's barrier height is 0,78 eV and does not change. V=1V direct voltage is applied. The electron's charge is $q = 1{,}6 \cdot 10^{-19}$ Cl. Boltzmann constant is k=0,86·10^{-4}eV/degree.

4b105.
The silicon asymmetric p-n junction with its unit surface is given. The donors' density at n-base is 10^{15} cm⁻³. Find the value of donors' density's change when the relevant charge capacitance change arises while applying 0,2 V reverse voltage. Vacuum's dielectric permittivity is ε_0= 8,86·10^{-12} F/m, and Si is ε = 12: Electron's charge $q = 1{,}6 \cdot 10^{-19}$ Cl. In case of the absence of voltage, the contact difference of the potentials is φ_h = 0,6 V.

4b106.
Determine the thermal equilibrium electron and hole concentrations in an n-type silicon at $T = 300K$ in which concentration of shallow donors is 4×10^{16}cm⁻³. The intrinsic carrier concentration is assumed to be $n_i = 1{,}5 \times 10^{10}$cm⁻³.

4b107.
Calculate the thermal-equilibrium electron and hole concentrations in compensated silicon at $T = 300K$ in which concentration of shallow donors and acceptors are $N_d = 2 \times 10^{15}$cm⁻³ and $N_a = 3 \times 10^{16}$cm⁻³, respectively. The intrinsic carrier concentration is assumed to be $n_i = 1{,}5 \times 10^{10}$cm⁻³.

4b108.
A silicon device with an n-type material is to be operated at T = 500 K. At this temperature the intrinsic carrier concentration must contribute no more than 10 percent of the total electron concentration. Determine the minimum donor concentration required to meet this specification. Take into account that silicon band-gap energy is $E_g = 1{,}12$ eV, electron and hole effective density-of-states mass is $0{,}32 m_0$ and $0{,}53 m_0$, respectively.

4b109.
$\mathbf{a}_1 = 5\hat{\mathbf{x}}$, $\mathbf{a}_2 = 2\hat{\mathbf{y}}$ and $\mathbf{a}_3 = \hat{\mathbf{z}}$ are the three basic vectors of a rhombic lattice whose lengths are expressed by angstroms. Determine sizes, volume and form of Brillouin first zone.

4b110.
Find the concentrations of charge carriers that correspond to the minimum value of resistivity of a semiconductor if given electrons' $\mu_n$and holes' μ_p mobilities.

4b111.
The density of donor in semiconductor which contains only donor impurity, is N_d, and their energy level is E_d. Find out the density of free electrons if the Fermi level coincides with E_d.

4b112.
How many free electrons and holes will emerge in a crystal in case of absorbing 10^{-4} J light energy by 2000 H wavelength? What amount of charge will pass through the external chain of the crystal if the applied electric field is capable of bringing all free electrons to electrodes. Quantum output is 1.

4b113.
Find Fermi speed of electrons in a conductor, accepting that there is one electron in an elementary cell. What is more:

$$E(\vec{K}) = E_0 \cos K_x a$$

where E_0 – equal to 0,5 eV, and the net constant: $a = 3h$.

4b114.

Both sources (ultraviolet with 400 nm wavelength, infrared with 700 nm wavelength) have 40 watt power. Which source delivers more photons per second?

4b115.

The photoconductivity red limit of intrinsic silicon corresponds to $\lambda_0 = 0{,}92\ \mu m$ wavelength. Determine the resistivity temperature coefficient of silicon at room temperature.

4b116.

The dark resistivity of silicon at room temperature is 0,5 Ωm. It is 0,4 Ωm for silicon under illumination. After $\Delta t = 10^{-2}$ s turn off illumination, the resistivity equals 0,42 Ωm. Determine the average lifetime of free electrons and holes.

4b117.

How many times should the intrinsic semiconductor resistivity vary if the semiconductor is doped by shallow acceptor impurities with $N_a = 2n_i$ concentration? Assume the ratio of electron and hole mobility is $b = \mu_n/\mu_p$.

4b118.

For aluminum, the work function is 4,28 eV, the mass density is 2,7 gr/cm^3, the molar mass is 27 gr/mol. Determine the potential energy of free electron in aluminum crystal if electron mass is $m = m_0$.

4b119.

The following semiconductors are given: Si, GaAs, GaP and GaN. Note which semiconductors are transparent, translucent and opaque visible for light (λ=0,4 - 0,7um), if it is known that E_{Si}=1,12 eV, E_{GaAs}=1,42 eV, E_{GaP}=2,26 eV and E_{GaN}=3,44 eV.

4b120.

Calculate the temperatures for which p-n junctions, made of Ge, Si and GaN, lose their corrective properties. For all cases accept N_a=N_d=10^{15}cm^{-3}, bandgap widths do not depend on temperature and are equal to 0,66, 1,12 and 3,44 eV respectively. The intrinsic semiconductor concentration in room temperature is n_i(Ge)=2*10^{13}cm^{-3}, n_i(Si)=10^{10}cm^{-3} and n_i(GaN)=10^{-9}cm^{-3}.

4b121.

Given a silicon $n^+ - p - n$ type transistor, moreover, N_{de}=10^{19} cm^{-3}, N_{ab}=3*10^{16} cm^{-3} and N_{dc}=5*10^{15} cm^{-3}. Find the maximum voltage of reverse bias of base-collector junction in room temperature (300 K), in case of which the base width is equal to zero. The base width (the distance between the quasi neutral borders of junctions) is equal to 0,5 um, while the intrinsic semiconductor concentration is
10^{10}cm^{-3}.

1b122.

Given a silicon p-n photodiode, the transition area of which is equal to 2cm^2. Acceptor and donor impurity concentrations are respectively equal to N_a=1,7*10^{16}cm^{-3} and N_d=5*10^{19}cm^{-3}, and intrinsic concentration of semiconductor 10^{10}cm^{-3}, lifetime of charge carriers respectively equals τ_n=10us and τ_p=0,5us, diffusion coefficients are equal to D_n=9,3cm^2/s and D_n=2,5cm^2/s, lightning current I_l=95mA. Find the open circuit voltage of that photodiode and the maximum power in room temperature (300K).

4b123.

A silicon MOS capacitance oxide thickness d = 10nm, concentration of acceptor impurities N_a=5*10^{17}cm^{-3}. Define the voltage value, needed near semiconductor-oxide surface, in case of which

a. semiconductor surface will become intrinsic semiconductor

b. semiconductor surface will become sharp inverse

Dielectric constant of semiconductor and oxide are respectively equal to 11,9 and 3,9. Temperature is 296K.

4b124.

Wave resistance of an interconnect composed of two parallel leads on opposite sides of a double-sided PCB is $z_{01} = \frac{120}{\sqrt{\varepsilon}}\frac{h}{w}$, while for a wired interconnect of two parallel wires with diameter d and spacing D wave resistance is $z_{02} = \frac{256}{\sqrt{\varepsilon}}\ell g \frac{2D}{d}$. Let D=5 and ε be the same for the two environments. Find the h/w ratio for which at the point of via between these two interconnects signal reflection is absent.

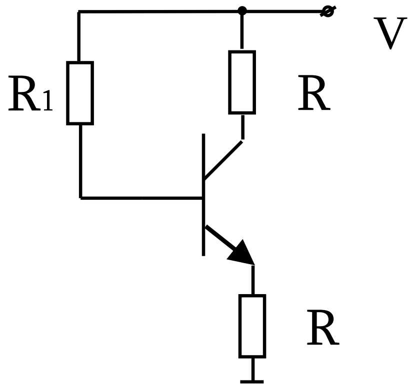
4b125.

It is known when forward voltage drop of diode is greater than thermal potential $U_d \gg \varphi_T$, then the diode current is expressed by: $I_d = I_0 e^{U_d/\varphi_T}$ formula.

Show that in the marked domain, differential R_d resistance of diode is inversely proportional to the current value.

4b126.

In the presented circuit, transistor's $\beta = 24$, base-emitter voltage drop 0,75V, $R_1 = 1000\mathrm{Ohm}$, $R_2 = 40\mathrm{Ohm}$, $R_3 = 200\mathrm{Ohm}$. Find the value of voltages of emitter, base and collector.



4b127.

Diameter (D) of a constant isolated cylindrical resistor is a 2mm, length (ℓ) is a 15mm, thickness (d) of deposited resistive tantalum film is 5mkm, specific resistance is $12 \cdot 10^{-8}$ Ohm · m.

Calculate the resistance of the resistor and variations of a resistance in percentage if the allowed variations of ℓ is 10%.

4b128.

In anisotropic crystal, the electron energy as a function of wave vector components is given in the following form: $E = \alpha_x k_{x^2} + \alpha_y k_{y^2} + \alpha_z k_{z^2}$, α_x, α_y and α_z are constants. Write the equation of motion of electrons corresponding to Newton's equation.

4b129.

Prove that in a level that is higher in δ dimension than the Femi level, the probability of the likelihood of electron is equal to the probability of the likelihood of electron not being a level that is lower in δ dimension than the Femi level.

4b130.

The emission energy of an electron out of tungsten is 4.17 eV, and out of cesium 1,81 eV. Calculate the wavelength threshold values for these materials (red line).

4b131.

At room temperature $(300^0 C)$, the mobilities of electrons and holes in monocrystal of silicon are respectively 0,16 and 0,04 $m^2/V \cdot sec$. Find diffusion coefficients of electrons and holes in the same temperature.

4b132.

It is established that if external alternating bias with amplitude $V_a = 0.5$ V is applied to the abrupt PN junction, the maximal capacitance of junction is equal to 2 pF. Determine built-in junction potential Φ_0 and the magnitude of minimal capacitance of junction if in the absence of an applied bias the junction capacitance is equal to 1 pF.

4b133.

Determine the number of lines in roentgenogram for a simple cubic lattice with lattice constant $a = 2.86 \cdot 10^{-8}$ cm if investigations are carried out under radiation with $\lambda = 1.789 \cdot 10^{-8}$ cm wavelength.

4b134.

At low temperature the cutoff (threshold) wavelength of external photoelectrical effect of intrinsic semiconductor is $\lambda_1 = 536$ nm, the cutoff (threshold) wavelength of photoconductivity is $\lambda_1 = 0.95$ mkm. Determine semiconductor conduction band bottom (E_c) location comparatively to vacuum.

4b135.

For direct current mode, the voltage V=0,15 V is applied to the semiconductor diode. The diode`s saturation current is I_o=15 µA. Determine the static resistance R_0 and differential resistance R_d of the diode at room temperature T=300 K. Use the following values of constants: electron charge **e**=1,6x10^{-19} C and Boltzmann constant k=1,38x10^{-23} J/K.

4b136.

The barrier capacitance of the diode is 250 pF when the V=1V reverse voltage was applied. Calculate the range of the capacitance change when the reverse voltage changes from 0 to 10V. Accept the built-in potential is equal to 0,81V. For capacitance calculations, use the following expression C= a/(V + φ_{cont})$^{1/2}$.

4b137.

At the certain direct voltage the ideal P-n junction current is I_1 at room temperature T=300K . At what direct voltage:

a) current will raise five-fold (I_2= 5I_1)?
b) the direct current will exceed the saturation current I_0 by 100-fold (I_2= 100I_o)?

4b138.

The specific resistance of n-Si is 60 Ohm·cm. Determine the p_n density of holes in 300^{0}K if the electron mobility is µ = 1300 cm^2/V·v, the electron charge q = 1,6 · 10^{-19} K, the intrinsic charge density is n_i = 1,6 · 10^{10} cm^{-3}.

4b139.

Find $\frac{R_R}{R_F}$ coefficient of flat diode correction by a constant current where R_R, R_F - inverse and direct variation resistances in case of constant currents, when forward bias voltage is $V_F = 1V$ and the constant current $I_s = 10^{-6} A$. The current is of diffusion. The applied direct and inverse voltages are ±0,5V. The thermal energy is kT = 0,026 eV, q = 1,6 · 10^{-19} K.

5. SEMICONDUCTOR TECHNOLOGY

a) Test questions

5a1. What is the number of photomasks defined by during the fabrication of the given integrated circuit?

A. Photomask wearability

B. Number of simultaneously processing semiconductor wafers

C. Number of topological layers formed on the wafer

D. Minimum of feature size

E. Production volume

5a2. What semiconductor material has the maximum band gap?

A. Si

B. Ge

C. GaAs

D. SiC

E. The correct answer is missing

5a3. The performance of a MOS transistor can be increased by:

A. Increasing the temperature

B. Decreasing the temperature

C. Changing the channel doping level

D. Decreasing thickness of dielectric layer

E. Increasing the gate voltage

5a4. Based on what semiconductor is it possible to make p-n junctions having higher operating temperatures?

A. Ge, Eg=0,66 eV

B. Si, Eg=1,12 eV

C. GaAs, Eg=1,45 eV

D. SiC, Eg= 3,1 eV

E. The correct answer is missing

5a5. The best resolution to form a topological pattern is

A. X-ray lithography

B. Electron beam lithography

C. Photolithography

D. Chemical lithography

E. All the answers are correct

5a6. What kind of p-n junction can be produced by epitaxial technology?

A. Linearly graded p-n junction

B. p-n junction by exponent function

C. Abrupt p-n junction

D. All the answers are correct

E. The correct answer is missing

5a7. Operating frequency of bipolar transistors can be increased by

A. Increasing emitter effectiveness

B. Decreasing base width

C. Applying collector large voltages

D. Decreasing base impurity level

E. Increasing signal frequency

5a8. Charge capacitance is larger than diffusion

A. Because it does not depend on the frequency

B. In reverse-biased mode of *p-n junction,*

C. In forward-biased mode of p-n junction

D. Because it depends on the value of applied voltage

E. Because it depends on the value of current

5a9. p-n junction current in reverse-biased mode can be reduced by:

A. The reduction of the density of impurities

B. The reduction of temperature

C. The reduction of contact potentials' difference

D. The reduction of applied voltage

E. The size reduction of p and n regions

5a10. Which semiconductor will have higher concentration of intrinsic carriers in the given temperature, for example T=300K?

A. Ge, Eg=0,66 eV

B. Si, Eg=1,12 eV

C. GaAs, Eg=1,45 eV

D. SiC Eg= 3,1eV

E. All the answers are correct

5a11. Diffusion first step (drive in) realization provides:

A. High surface density and large diffusion depth of impurities

B. High surface density and small diffusion depth of impurities

C. Low surface density and large diffusion depth of impurities

D. Low surface density and small diffusion depth of impurities

E. Low surface density of impurities

5a12. In semiconductor crystals dislocations are classified as:

A. Schottky defects

B. Linear structural defects

C. Frenkel defects

D. Surface structural defects

E. Volume structural defects

5a13. Epitaxial growth technology of layers allows receiving:

A. Linearly graded p-n junction

B. p-n junction by exponent function

C. Abrupt p-n junction

D. p-n junction by arbitrary function

E. p-n junction by quadratic function

5a14. Zone-melting method advantage of silicon monocrystal growth over Chokhralsi method is conditioned by:

A. Absence of quartz melting tube

B. Low level of thermal gradient

C. High speed of monocrystal growth

D. Low temperature of the process

E. Presence of inexpensive equipment

5a15. For a diffusion from the infinite source the diffusion depth x_j depends on diffusion time t by the following expression:

A. $x_j \sim t$

B. $x_j \sim t^{1/2}$

C. $x_j \sim t^2$

D. $x_j \sim t^3$

E. $x_j \sim exp(t)$

5a16. The saturation of drain current on the output characteristic of p-n junction FET is determined by:

A. Self-restriction effect if drain current increase

B. Velocity saturation of channel majority carriers caused by drain voltage

C. Density Impurities in the channel

D. A and B

E. All the answers are correct

5a17. What is diode's I-V characteristic linearity conditioned by:

A. Ohmic contacts of diode

B. Crystal structure of output material

C. Contact potential difference of p-n junction

D. Density of impurities in the base

E. Width of output material band gap

5a18. The oxide layer of a MOS transistor is formed by the following method:

A. Chemical

B. Ion implantation

C. Epitaxial deposition

D. Thermal oxidation

E. Diffusion

5a19. When a diode is forward biased, which carriers create current?

A. Ions of impurity atoms

B. Surface charges

C. Majority carriers

D. Minority carriers

E. Free electrons of the base

5a20. Temperature of diffusion process in silicon IC technology is

A. Less than 800^0C

B. higher than 1500^0C

C. In $1100\ldots1300^0C$ range

D. Independent of temperature

E. All the answers are correct

5a21. The current-voltage characteristic of p-n junction

A. Is linear

B. Is strictly non linear

C. Forward current value smaller than reverse current

D. Reverse current value higher than forward current

E. Independent of temperature

5a22. In case of which connection does the bipolar transistor provide simultaneous amplification of current, voltage and power?

A. Common collector

B. Common base

C. Common emitter

D. When the transistor is used by separated base

E. When emitter and base are short connected

5a23. What is the load resistance of a bipolar transistor look like connected by common base?

A. Larger than the resistance of collector p-n junction

B. Smaller than the resistance of collector p-n junction

C. Larger than the resistance of emitter p-n junction

D. Equal to base resistance

E. Equal to the resistance of input contact

5a24. For an intrinsic semiconductor the electron concentration is 10^{14} cm^{-3}. What is the hole concentration?

A. Higher than 10^{14} cm^{-3}

B. Less than 10^{14} cm^{-3}

C. Equal to electron concentration

D. All the answers are correct

E. All the answers are wrong

5a25. Semiconductor structures of A_3B_5 (GaAs, InP, InAs, GaSb) type are made by:

A. Heteroepitaxal growth method

B. Diffusion method

C. Homoepitaxal growth method

D. Ion Implantation method

E. Vacuum deposition method

5a26. Speed of silicon thermal oxidation is limited by:

A. Speed of surface adsorption of oxidants (O_2, H_2O)

B. Speed of diffusion oxidants through the SiO_2 layer to Si-SiO_2 interface

C. Speed of oxidation reaction with silicon

D. Speed of diffusion of gas results of silicon surface reaction

E. All the answers are correct

5a27. Thickness of silicon dioxide d is dependent on duration t of high-temperature oxidation by the following expression:

A. $d \sim t^{1/2}$

B. $d \sim t$

C. $d \sim t^2$

D. $d \sim t^3$

E. $d \sim \exp(t)$

5a28. What is the technology roadmap of photolithography process?

A. Photoresist coating - alignment - development - exposure - etching

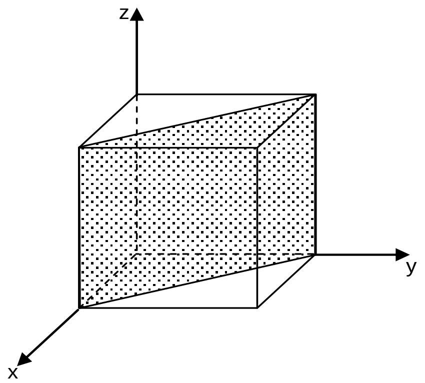
B. Photoresist coating - development - alignment - exposure - etching

C. Photoresist coating - alignment - exposure - etching - development

D. Photoresist coating - exposure - alignment - etching - development

E. Photoresist coating - alignment - exposure - development - etching

5a29. What crystal plane is shaded in cubic crystal?



A. (001)

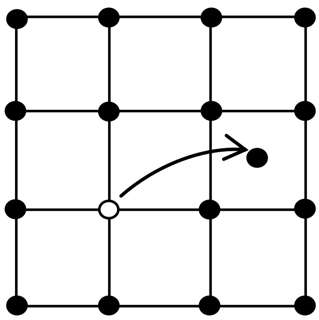
B. (100)

C. (101)

D. (110)

E. (111)

5a30. What structural defect is figured?



A. Shottky defect

B. Linear structural defect

C. Frenkel defect

D. Surface structural defect

E. Volume structural defect.

5a31. Sub-collector n+ buried layer in n-p-n bipolar transistor structures is intended for:

A. Reducing the bulk resistance of lateral collector

B. Increasing the bulk resistance of lateral collector

C. Increasing the transient resistance of collector-emitter

D. Reducing the transient resistance of collector-emitter

E. Reducing the minority-carrier lifetime in collector

5a32. To obtain n-type semiconductor silicon in microelectronic processing the following are used as an impurity:

A. Elements of fifth group of periodic table

B. Elements of forth group of periodic table

C. Elements of third group of periodic table

D. Elements of first group of periodic table

E. Elements of sixth group of periodic table

5a33. To obtain p-type semiconductor silicon in microelectronic processing the following are used as an impurity:

A. Elements of forth group of periodic table

B. Elements of sixth group of periodic table

C Elements of third group of periodic table

D. Elements of fifth group of periodic table

E. Elements of second group of periodic table

5a34. In IC technology the photolithographic process is meant for:

A. Forming the picture of topological layer on the substrate surface

B. Getting thin metallic films on the substrate surface

C. Getting thin dielectric films on the substrate surface

D. Getting thick oxide films on the substrate surface

E. Getting thin metallic and dielectric films on the substrate surface

5a35. In bipolar semiconductor ICs the electric coupling between layers of the multilevel metalization is realized by:

A. Diffusion structures

B. Metallic through holes

C. Electric coupling between layers is absent

D. External metallic conductors

E .The correct answer is missing

5a36. In bipolar semiconductor ICs the resistors are formed:

A .in terms of base region

B. In terms of emitter region

C. In terms of base- emitter junction

D. A and B answers are correct

E. A, B and C answers are correct

5a37. The design rules for ICs:

A. Are used to design applications specific integrated circuits

B. Define the minimal sizes of the elements and spacing between them during layout design

C. Are non-dependent on level of manufacturing process

D. Are created by designer using design expertise

E. The correct answer is missing

5a38. In real p-n junctions beyond the defined value of the reverse voltage the reverse current:

A. Sharply decreases

B. Slowly decreases

C. Sharply rises

D. Slowly rises

E. Remains practically constant

5a39. In semiconductor ICs to form the doped regions with required type and conductance in the substrate the following methods are used:

A. Diffusion and ion implantation

B. Ion implantation and thermal oxidation

C. Ion etching and diffusion

D. Diffusion and thermal oxidation

E. The correct answer is missing

5a40. For the real p-n junction the main breakdown mechanisms are:

A Thermal, tunnel and avalanche

B. Tunnel, mechanical and thermal

C. Thermal, radiation and chemical

D. Avalanche, and electron-beam

E. Thermal, electrochemical and tunnel

5a41. For a MOS structure transistor the minimal thickness of the oxide layer is limited by:

A. Capabilities of the manufacturing technology

B. Values of the unwanted tunnel currents

C. Critical electric field strength

D. Defects concentration

E. All the answers are correct

5a42. To compensate the radiation defects after the ion implantation doping the following processes are necessary:

A. The additional doping with the donor impurities

B. The additional doping with the acceptor impurities

C. Thermal treatment in $(600....800)^0C$ *range*

D. Thermal treatment in $(1300....1500)^0C$ *range*

E. The mechanical planarization of the crystal surface

5a43. In case of IC scaling by $\alpha > 1$ factor the power density changes in the following way:

A. Decreases by α *time*

B. Increases by α *time*

C. Remains constant

D. Increases by α^2 *time*

E. Decreases by α^2 *time*

5a44. As a MOS-resistor forming region in MOS IC, the following are used:

A. Transistor’s channel

B. Transistor’s source

C. Transistor’s drain

D. Gate's insulator

E. Metal gate

5a45. To reduce the resistivity of the polisilicon in IC technology the following is performed:

A. Impurities additional doping and silicide process

B. Ion etching and impurities additional doping

C. Silicide process and ion etching

D. Surface oxidation and ion etching

E. Silicide process and thermal oxidation

5a46. For an n-type silicon the donor impurity concentration is $N_d = 10^{16}$ cm^{-3}. What kind and which concentration of impurity will be used to form p-n junction in this sample?

A. Boron with $N > 10^{16}$ cm^{-3}

B. Boron with $N < 10^{16}$ cm^{-3}

C. Boron with $N = 10^{16}$ cm^{-3}

D. Phosphorus with any concentration

E. Phosphorus with $N > 10^{16}$ cm^{-3}

5a47. For a p-type silicon the acceptor impurity concentration is $N_a = 10^{15}$ cm^{-3}. What kind and which concentration of impurity will be used to form p-n junction in this sample?

A. Phosphorus with $N = 10^{15}$ cm^{-3}

B. Phosphorus with $N < 10^{15}$ cm^{-3}

C. Phosphorus with $N > 10^{15}$ cm^{-3}

D. Boron with any concentration

E. Boron with $N > 10^{15}$ cm^{-3}

5a48. The main limitations to reduce the feature sizes of the nanoscale integrated circuits are:

A. Physical

B. Technological

C. Thermal

D. Statistical

E. All the answers are true

5a49. For contemporary integrated circuits the signal time delay in the first place is defined by:

A. Gates time delay

B. Interconnecting layers time delay

C. Signals frequency range

D. Structure of the package

E. None of the above

5a50. The impurity maximum concentration in the ion implanted layers is controlled by:

A. Ion energy

B. Ion angle of incidence

C. Impurity doping dose

D. Doping temperature

E. Thermal process temperature

5a51. As compared to the diffusion process, the ion implantation is realized at:

A. Higher temperatures

B. Lower temperatures

C. Same temperatures

D. Presence of concentration gradient

E. By neutral atoms flux

5a52. The basic manufacturing method to form the layout pattern of contemporary integrated circuits is:

A. Ionic lithography

B. Electron-beam lithography

C. Subwavelength lithography

D. Electromechanical lithography

E. Molecular lithography

5a53. In VLSI technology the "dry" etching method is realized by:

A. Neutral atoms flux

B. Accelerated ions flux

C. Mechanical polishing

D. Chemical-mechanical polishing

E. Chemical solution

5a54. The basic requirement to the interlayer dielectric material in the VLSI multilayer interconnection structure is:

A. High dielectric permittivity

B. High specific conductivity

C. High mechanical strength

D. Low dielectric permittivity

E. Dielectric layer is not used

5a55. What is mainly used in MOS integrated circuits as a circuit resistor:

A. High doped source region

B. High doped drain region

C. Gate dielectric region

D. Transistor channel region

E. Resistive elements are not used

5a56. Design for manufacturability can be defined as:

A. Checking all physical, electrical, and logical errors, after the chip comes back from fabrication

B. Checking the chip before fabrication for operation at stress conditions such as low voltage, high

temperature, and process variation

C. Checking the chip before fabrication for the correct functionality under nominal conditions

D. Designing techniques that allow the designer to test the chip after fabrication

E. None of the above

5a57. Signal propagation delay in IC, is mostly determined by:

F. Delay of MOS transistors

G. Delay of interconnects

H. Structure of IC package

I. The correct answer is missing

J. The answers A,B and C are correct

5a58. To increase the gate specific capacitance of a MOS transistor it is necessary to:

A. Use dielectric films with low permittivity

B. Decrease the thickness of dielectric film

C. Increase operation voltages

D. Increase the area of the gate

E. The correct answer is missing

5a59. To increase the gate specific capacitance of a MOS transistor it is necessary to:

A. Increase the thickness of dielectric film

B. Use high permittivity (high-k) dielectric films

C. Decrease the area of the gate

D. Increase operation voltages

E. The correct answer is missing

5a60. The large-scale industry application of electron beam lithography to produce IC elements is limited by:

A. Extremely slow process

B. Poor efficiency process

C. Equipment complexity

D. More expensive facilities

E. All the answers are correct

5a61. In the current IC manufacturing process the ion implantation is used to perform the following technological operations:

A. Ion cleaning of the surface of semiconductor substrate

B. Ion etching of thin films and substrates

C. Adjusting transistor's threshold voltage

D. Forming channel-stop layers

E. All the answers are correct

5a62. The advanced technologies to form layout pattern of ICs are:

A. Electron-beam lithography

B. Immersion lithography

C. Optical proximity correction (OPC) technology

D. Phase shift mask (PSM) technology

E. All the answers are correct

5a63. In the IC manufacturing process the chemical-mechanical-polishing (CMP) technology is used:

A. To reduce the thickness of semiconductor substrate

B. *For chemical activation of the substrate surface*

C. *For planarization of the substrate surface prior to lithography process*

D. *To form vias in the structure of multilevel metallization structure*

E. *All the answers are correct*

5a64. The intrinsic silicon is doped simultaneously with donor and acceptor impurities with the concentrations $N_d=10^{18}$ cm^{-3} and $Na=10^{17}$ cm^{-3} respectively. What are the type of conductivity and active concentration of the silicon?

A. *n-type,* $N_{active} = 10^{17}\ cm^{-3}$

B. *n-type,* $N_{active} = 9x10^{17}\ cm^{-3}$

C. *n-type,* $N_{active} = 10^{18}\ cm^{-3}$

D. *p- type,* $N_{active} = 5x10^{17}\ cm^{-3}$

E. *Intrinsic conductivity,* $N_{active} = 0$

5a65. The basic requirement to the interlayer dielectric material in the VLSI multilayer interconnection structure is:

A. *High dielectric permittivity*

B. *Possible low dielectric permittivity*

C. *Dielectric layer is not used*

D. *High specific conductivity*

E. *Low specific resistance*

5a66. The specific surface resistance (sheet resistance) of the semiconductor region is defined

A. *Only by the specific resistance of the semiconductor material*

B. *By the specific resistance of the semiconductor material and the thickness of the region*

C. *Only by the width of the semiconductor region*

D. *Only by the thickness of the semiconductor region*

E. *Only by the geometric dimensions of the semiconductor region*

5a67. In industrial planar technology of integrated circuits the “dry” etching process is performed by:

A. *Neutral atoms flux*

B. *Accelerated ions flux*

C. *Active chemical solutions*

D. *Atoms chemical activation*

E. *Focused electron beam*

5a68. An important characteristics of industrial planar technology of integrated circuits is the following:

A. *Use of high purity materials and chemical reagents*

B. *Priority of group technologies*

C. *Main technological processes are implemented in “clean rooms”*

D. *High yield*

E. *All the answers are correct*

5a69. The current- voltage (I-V) characteristic of the semiconductor diode is:

A. *linear*

B. *nonlinear*

C. *quadratic*

D. *homogeneous*

E. *None of the above*

5a70. One of the answers is not an isolation method for IC semiconductor technology:

A. *Diode isolation*

B. *p-n junction isolation*

C. *Dielectric insulation*

D. *Composite insulation*

E. *Electromechanical insulation*

5a71. In the channel region of the short channel MOS integrated transistor the mobility of the carriers:

A. *Increases when the drain-source voltage* V_{ds} *is increased*

B. *Decreases when the drain-source voltage* V_{ds} *is increased*

C. *Not dependent on drain-source voltage* V_{ds}

D. *Has constant value*

E. *None of the above*

5a72. The threshold voltage of the short channel integrated MOS transistor :

A. *Does not depend on the channel length*

B. *Depends on the channel length*
C. *Has constant value*
D. *Decreases when the channel length is increased.*
E. *None of the above*

5a73. The maximal acceptable value of applied reverse voltage of the semiconductor diode is limited by:
A. *Diode barrier capacitance*
B. *Diode diffusion capacitance*
C. *Breakdown voltage*
D. *Value of supply voltage*
E. *Structure of package, first of all*

5a74. For the short channel MOS integrated transistor the integral feature is:

A. *Phenomena, specified by hot electrons may be ignored*
B. *Threshold voltage value does not depend on the channel length*
C. *Threshold voltage value depends on the channel length*
D. *Mobility of the carriers does not depend on the value of V_{ds} voltage*
E. *Mobility of the carriers in the channel region has constant value.*

5a75. For the n-type silicon the donor impurity concentration is $N_d = 10^{17}$ cm^{-3}. Using the ion implantation method the sample is doped by the boron impurity with $N_a = 10^{18}$ cm^{-3}: What is the type of conductivity and active concentration of the sample?
A. *n –type, $N_{act} = 10^{18}$ cm^{-3}*
B. *n –type, $N_{act} = 9x10^{17}$ cm^{-3}*
C. *p –type, $N_{act} = 10^{18}$ cm^{-3}*
D. *p –type, $N_{act} = 9x10^{17}$ cm^{-3}*
E. *Intrinsic conductivity*

5a76. For the p-type silicon the acceptor impurity concentration is $N_d = 10^{17}$ cm^{-3}. Using the ion implantation method the sample is doped by the phosphorus impurity with $N_a = 10^{18}$ cm^{-3}: What is the type of conductivity and active concentration of the sample?
A. *p –type, $N_{act} = 10^{18}$ sm^{-3}*
B. *p –type, $N_{act} = 9x10^{17}$ cm^{-3}*
C. *n –type, $N_{act} = 10^{18}$ cm^{-3}*
D. *n –type, $N_{act} = 9x10^{17}$ cm^{-3}*
E. *Intrinsic conductivity*

5a77. In contemporary integrated circuits, the diameter of silicon wafer already reaches:
A. *100 mm*
B. *200 mm*
C. *300 mm*
D. *450 mm*
E. *600 mm*

5a78. The silicon crystal has been doped by phosphorus atoms of $8x10^8$ atom/cm^3 concentration. What would be the conductivity type of silicon at room temperature, if the intrinsic concentration is equal to $1,8x10^{10}$ atom/cm^3.
A. *Intrinsic conductivity*
B. *Metal conductivity*
C. *n- type conductivity*
D. *p- type conductivity*
E. *The correct answer is missing*

5a79. Overall, the increase in temperature leads to the following action of semiconductor specific resistance:
A. *Increase*
B. *Decrease*
C. *Remains unchanged*
D. *Depends on the type of semiconductor conductivity,*
E. *Depends on the geometrical dimensions of the semiconductor*

b) Problems

5b1.

For a silicon p-n junction the specific resistances of p and n-regions are 10^{-4} Ohm·m and 10^{-2} Ohm·m correspondingly. Calculate the contact potential of the junction at a room temperature when T=300K if the mobility of holes and electrons are 0,05 m^2 V^{-1} s^{-1} and 0,13 m^2 V^{-1} s^{-1}. The intrinsic concentration at a room temperature equals $1,38x10^{16}$m^{-3} .

5b2.

Calculate the density of electrons and holes in a p-Ge at a room temperature if the sample specific conductance equals 100 S/cm, mobility of holes is 1900 cm^2 V^{-1} s^{-1}, and $n_i=2,5x10^{13}$ atom/cm^3.

5b3.

The silicon sample is doped with a donor impurity $N_d = 10^{17}$atom/cm^3. The sample length equals 100μm, width 10 μm, and thickness 1 μm. Calculate the resistance and sheet resistance.

5b4.

What thickness of SiO_2 layer is required to fabricate a MOS capacitor with a specific capacity of 100nF/cm^2 (ε_{SiO2}=3,8x8,85x10^{-14} F/cm).

What oxidation process (wet or dry) would be used to grow the gate high quality oxide?

5b5.

The gate capacitance of the MOS transistor equals C. The capacitor structure is scaled by the factor $\alpha = 2$. How will the gate capacitance change?

5b6.

Semiconductor's band gap width Eg = 0.7eV and the temperature does not change when T_1 = 250 K changes to T_2 = 300 K. V=0.4V forward bias voltage is applied to the p-n junction created in it. Define j_2/j_1 change of current density in the mentioned range of temperature change if in case of T_2 = 300 K, kT = 0.026eV.

5b7.

How will the channel of a p-n junction field effect transistor change when the drain voltage is V=+0.1 V if the dielectric transparency of semiconductor ε = 12, and for vacuum $\varepsilon_0 = 8.86 \cdot 10^{-12}$ F/m, contact difference of potentials φ_k=0.6V, electron charge q=1.6*10^{19} K, and donor density in n channel $N_d = 10^{15}$ cm^{-3}. Ignore the effects of source-drain and gate-drain domains.

5b8.

Calculate the drain current of a silicon n-MOSFET for the following conditions: V_t = 1 V, gate width W = 10 μm, gate length L = 1μm and oxide thickness t_{ox} = 10 nm. The device is biased with V_{GS} = 3 V and V_{DS} = 5 V. Use the device quadratic model, a surface mobility of 300 cm^2/V-s and V_{BS} = 0 V.

5b9.

For a silicon n-channel MOS FET the source- drain distance is 1μm and the doping levels are $N_d = 10^{20}$ cm^{-3}. The substrate doping is $N_a = 10^{16}$ cm^{-3}. Assume that the source and substrate are grounded. At what V_D voltage on the drain the deplation widths of source and drain p-n junctions will meet (punch-through effect)?

5b10.

The donor impurity concentration in the silicon substrate changes linearly N=kx [cm^{-3}], where k= 8 x 10^{18} cm^{-4} and x is a distance. Calculate electrons diffusion current density when the electric field is absent. Electrons mobility at room temperature (T=300 K) is 1200 cm^2/V·s.

5b11.

For a silicon n^+ - p - n bipolar transistor the base width is W_B=0,6um, the doping levels of emitter, collector and base are N_{de} =10^{19} cm^{-3}, N_{dc} =$5x10^{16}$ cm^{-3} and N_{ab}=$5x10^{15}$ cm^{-3}respectively. Define the collector critical voltage, when the device becomes uncontrolled (punch-through in the base region). Assume T=300 K and intrinsic concentration is n_i=$1,5x10^{10}$ cm^{-3}.

5b12.

The intrinsic silicon wafer is doped with donor N_d = 10^{17} cm^{-3} and acceptor N_a =10^{16} cm^{-3} impurities simultaneously. What is the silicon polarity of conductivity ? Calculate the specific conductivity of the sample at room temperature T= 300 K. The electrons mobility at room temperature is 1400 $cm^2/V \cdot s$, and electron charge is $1,6x10^{-19}$ C.

5b13.

Estimate the time delay in a n^+ polysilicon interconnect for the following conditions: the line length l=1mm, width b=1 μm, the sheet resistance of polysilicon $\rho_\square$=200 Ω/□, and the specific capacity of the line to the substrate C_0=60 aF/μm ^{2}.

5b14.

Estimate the time delay in the metal interconnect (metal 1) for the following conditions: the line length l=1mm, width b=200 nm, the metal sheet resistance $\rho_\square$=0,1 Ω/□, and the specific capacity of the line to the substrate C_0=23 aF/μm ^{2}.

5b15.

Consider a one-sided silicon p-n diode with N_d = 10^{16} cm^{-3} and N_a = 10^{18} cm^{-3}. Calculate the p-n junction barrier layer capacitance for applied reverse voltages U_1= 0 V and U_2= -5 V. Assume the contact potential of p–n junction at room temperature is 0,7 V, relative permittivity of silicon ε_{Si}=11,8, dielectric constant ε_0= $8,85x10^{-14}$F/cm and the junction area S_{p-n} = 10^{-5} cm^2.

5b16.

In the IC structure the polysilicon interconnect line is formed on the surface of the thick oxide layer and passed above the high doped n^+ region. Calculate the signal time delay for the conditions:

line length l= 50μm, line width w=0,5μm, sheet resistance ρ=500Ω/sq, oxide layer thickness t_{ox}=0,2μm, dielectric permittivity ε_{ox}=3,9.

5b17.

The MOS structure transistor is scaled by the α factor. How will the transistor's power consumption, power density, time delay and switching energy change using the constant electric field scaling approach?

5b18.

The semiconductor resistor is formed on the basis of MOS transistor's n-well. The resistor's length is 50 μm and width is 2,5μm. Estimate the resistance change value over temperature range of 0^0C to 100^0C. The sheet resistance of the n-well resistor at room temperature (27^0C) is 300 Ω/sq and temperature coefficient is 0,0024 1/ °C.

5b19.

The diffusion resistor is formed in the emitter n^+ region of the bipolar transistor. The emitter layer thickness is h=0,1 μm and doping level is $10^{19}$$cm^{-3}$. Calculate the resistance of the basic region for the conditions:

length l= 10 μm, width w= 0,5 μm, electron mobility μ_n=1400 $cm^2/V \cdot s$.

5b20.

For a silicon semiconductor sample the donor impurity concentration N_d changes linearly from 10^{18} cm^{-3} to $5x10^{17}$ cm^{-3}, when the coordinate change is ΔX=3 mkm. Calculate the diffusion current density in the sample when the electrical field is absent. The electrons mobility at room temperature is μ = 1200 $cm^2/V·s$ and the thermal potential is φ_t = 0,026 V.

5b21.

The optical properties of photolithography system are described by the Rayleigh equations. Estimate the R resolution and F focus depth of the optical system. Accept that wavelength λ=193 nm, numerical aperture N_A=0,65 and coefficients k_1=0,3 and k_2=0,5. Discuss the possibility to increase the resolution using the immersion lithography technology.

5b22.

For a silicon n-channel MOS transistor the channel width is W = 5 mkm, channel length is L = 0,3 mkm, oxide thickness is t_{ox} = 15 nm and threshold voltage is V_t = 0,7 V. The device is biased with V_{GS} = 1,5 V and V_{DS} = 3 V. Calculate the drain current using the quadratic model. A surface mobility of electrons is 500 $cm^2/V·s$ and V_{BS} = 0 V. Calculate the channel resistance for the same conditions.

5b23.

Calculate the temperature when the resistance of the silicide polysilicon increases by 50% compared to room temperature (t=27°C). The silicide polysilicon temperature coefficient of resistance is 0,0033 1/°C.

5b24.

Indicate that under the specific temperature the semiconductor sample has minimal specific conductivity (σ), when the electrons **n** concentration is determined with expression $n=n_i (\mu_p/\mu_n)^{0,5}$, where n_i is the intrinsic concentration of the the charge carriers, and μ_n and μ_p are accordingly electrons and holes mobility.

5b25.

Germanium semiconductor diode is operating at U=0,1V direct voltage and under T= 300K temperature. The diode's saturation current is I_o=20 mkA.

Determine:

A. Diode's R_o resistance towards the constant current;

B. Differential r_d resistance.

5b26.

5V voltage is applied on n-type silicon sample the length of which is l=1 cm. Calculate the electron's flight time over the length of the sample, when the specific resistance is = 10 Ohm.cm and electrons' concentration is $n=10^{21}$ m^{-3}.

5b27.

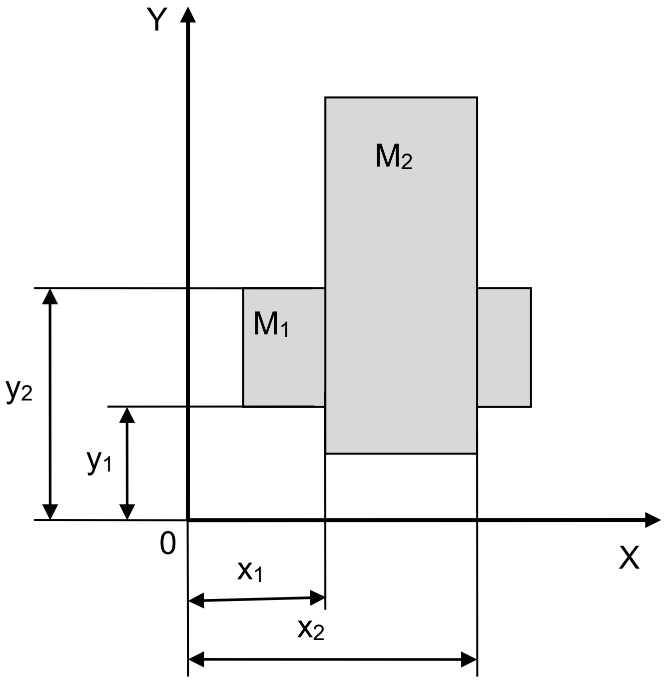
How should V_{GS1} voltage applied to the MOS transistor's gate change so that the transistors' channel differential resistance increases by 50 %. Note that V_{GS1}= 1,0 V and the threshold voltage is V_t = 0,3 V. Use the following expression for the MOS transistor's current:

$$I_{DS} = 0,5\mu C_{ox}(W/L)(V_{GS} - V_t)^2 .$$

5b28.

M_1 and M_2 fragments, which belong to different metal layers of IC, are shown in the figure. The inter-layer parasitic effective capacitance, present between metal layers is 0,2 Ff/um^2. Topological sizes of metal fragments with their deviations are given.

x_1=10 um$\pm$0,1 um
x_2=20 um$\pm$2 %
y_1=8 um$\pm$0,1 um
y_2=15 um$\pm$4%



It is required to calculate the nominal value and absolute deviations of parasite capacitance of M_1 and M_2 metal fragments' overlap. Calculate with hundredth accuracy.

5b29.
It is necessary to design a polysilicon based rectangular resistor with R= 10 kOhm and dissipated power P= 0,5 mW. Estimate the length and width of the resistive region. The sheet resistance of the polysilicon layer and specific power are $\rho_{\square}$=2 kOm/$\square$ and P_o=P/S $\leq$ 1W/mm^2 respectively.

5b30.
The diffusion resistor with R= 5 kOhm and dissipated power P= 1 mW is formed on the basis of base region of the bipolar transistor. Estimate the length and width of the main resistive region for the following conditions: the sheet resistance of the base region is $\rho_{\square}$=400 Om/$\square$ and the maximum value of the specific power not exceeding P_o=P/S $\leq$1 W/mm^2

5b31.
Estimate the flight time of charge carriers in nMOS transistor with induced channel in case of the following conditions:
Channel length L=100 nm, V_{DS} voltage is 3 V, the charge carriers' mobility in the channel is μ=600 cm^2/V x s.
What limits the speed of a real transistor?

5b32.
There is a rectangular silicon sample with n- type conductance, the length of which is l=6mm, width b=3mm and thickness h=1 mm. Calculate the current density passing through the sample if the voltage applied across the sample is 4V. Accept the electron concentration in a semiconductor is n=10^{21}m^{-3}, mobility μ=0,14m^2/V x s, and the electron charge e=1,6x10^{-19} Cl.

6. NUMERICAL METHODS AND OPTIMIZATION

a) Test questions

6a1. Fragmentation consecutive algorithm, compared with iteration algorithm, has:

A. More accuracy
B. Higher performance
C. Less accuracy
D. More machine time
E. B and C together

6a2. Which is the inverse polynomial of X^4+X+1?

A. X^3+X+1
B. X^4+X+1
C. X^4+X^2+1
D. X^4+X^3+1
E. The correct answer is missing

6a3. Which of the given intrinsic description forms more accurately describes an electrical circuit?

A. The graph of commutation schema
B. Complex list
C. Adjacency matrix
D. A and B equally
E. B and C equally

6a4. The following problem of linear programming:

$$2x_1+3x_2 \to \max$$
$$\begin{cases} 7x_1+6x_2 \le 42 \\ -x_1+5x_2 \le 15 \\ x_1 \ge 0,\ x_2 \ge 0: \end{cases}$$

A. Does not have solution
B. Has one solution
C. Has two solutions
D. Has solutions with infinite set
E. Has unlimited solutions

6a5. In case of which values of parameter λ the following problem has infinite set of solutions?

$$f(X)=\lambda x_1+x_2 \to \min_{X\in D},$$
$$D:\begin{cases} x_1+2x_2 \ge 2, \\ x_1-4x_2 \le 2, \\ 6x_1+5x_2 \le 30, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. 2
B. 1/2
C. 1
D. 1/4
E. 1/8

6a6. In case of which values of λ_1,λ_2 parameters the following problem has one solution?

$$f(X)=\lambda_1 x_1+\lambda_2 x_2 \to \min_{X\in D},$$
$$D:\begin{cases} x_1+2x_2 \ge 2, \\ x_1-4x_2 \le 2, \\ 6x_1+5x_2 \le 30, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. $\lambda_1=1, \lambda_2=4$
B. $\lambda_1=1/2, \lambda_2=1$
C. $\lambda_1=2, \lambda_2=4$
D. $\lambda_1=4, \lambda_2=8$
E. $\lambda_1=1, \lambda_2=2$

6a7. In case of what values of λ parameters the following problem does not have a solution?

$$f(X) = x_1 + x_2 + x_3 \to \max_{X\in D},$$
$$D:\begin{cases} x_1 + x_3 = 2, \\ x_1 + 2\lambda x_2 + x_3 = 0, \\ x_1 \ge 0, x_2 \ge 0, x_3 > 0: \end{cases}$$

A. 0
B. 5
C. 1
D. 1/2
E. 2

6a8. In case of what values of b_{21} and b_{22} elements

$$A=\begin{bmatrix} 2 & 0 & 1 \\ 0 & 1 & 2 \\ 4 & 2 & 0 \end{bmatrix},\ B=\begin{bmatrix} 1 & 2 \\ b_{21} & b_{22} \\ 0 & 1 \end{bmatrix}$$

matrix system will not be fully controllable?

A. $b_{21}\ne 0, b_{22}=0$
B. $b_{21}=0, b_{22}=0$
C. $b_{21}\ne 0, b_{22}\ne 0$
D. $b_{21}=0, b_{22}\ne 0$
E. The correct answer is missing

6a9. In case of which values of b_{11} and b_{12} elements

$$A=\begin{bmatrix} 1 & 0 & 2 \\ 2 & 1 & 0 \\ 0 & 2 & 4 \end{bmatrix},\ B=\begin{bmatrix} b_{11} & b_{12} \\ 1 & 2 \\ 2 & 0 \end{bmatrix}$$

matrix system will not be fully controllable?

A. $b_{11}=0, b_{12}=0$

B. $b_{11}=1, b_{12}=2$
C. $b_{11}=2, b_{12}=0$
D. $b_{11}=1, b_{12}=0$
E. $b_{11}=0, b_{12}=1$

6a10. In case of which values of c_{11} and c_{12} elements

$$A=\begin{bmatrix}2&0&1\\1&2&0\\1&1&1\end{bmatrix},\ C=\begin{bmatrix}c_{11}&c_{12}&0\\1&2&3\end{bmatrix}$$

matrix system will not be fully observable?

A. $c_{11}=0, c_{12}=0$
B. $c_{11}\neq0, c_{12}=0$
C. $c_{11}=0, c_{12}\neq0$
D. $c_{11}\neq0, c_{12}\neq0$
E. The correct answer is missing

6a11. In case of what values of b_{11}, b_{21} and b_{31} elements

$$A=\begin{bmatrix}2&1&0\\1&2&1\\2&1&1\end{bmatrix},\ B=\begin{bmatrix}b_{11}&0\\b_{21}&2\\b_{31}&1\end{bmatrix}$$

matrix system will not be normal system?

A. $b_{11}=0, b_{21}=0, b_{31}=0$
B. $b_{11}=0, b_{21}\neq0, b_{31}=1$
C. $b_{11}\neq0, b_{21}=0, b_{31}=2$
D. $b_{11}=1, b_{21}=1, b_{31}=1$
E. $b_{11}=2, b_{21}\neq1, b_{31}=0$

6a12. For the given game model: for which values of p and q the expression $(i_0,j_0)=(2,2)$ is the best strategy?

$$\begin{bmatrix}1&q&6\\p&5&10\\6&2&3\end{bmatrix}$$

A. $p\le5$ *and* $q\ge5$
B. $p\le5$ *and* $q\le5$
C. $p\ge5$ *and* $q\le5$
D. $p\ge5$ *and* $q\ge5$
E. The correct answer is missing

6a13. For the given game model, for which values of n and m $(i_0,j_0)=(2,2)$ is the best strategy?

$$\begin{bmatrix}0&m&5\\n&4&9\\5&1&2\end{bmatrix}$$

A. $n\le4$ *and* $m\ge4$
B. $n\le4$ *and* $m\le4$
C. $n\ge4$ *and* $m\le4$
D. $n\ge4$ *and* $m\ge4$
E. The correct answer is missing

6a14. For the given game model, in case of which values of p and q $(i_0,j_0)=(2,2)$ will be the best strategy?

$$\begin{bmatrix}4&6&3\\15&11&q\\2&p&9\end{bmatrix}$$

A. $p\ge11$ *and* $q\le11$
B. $p\le11$ *and* $q\le11$
C. $p\ge11$ *and* $q\ge11$
D. $p\le11$ *and* $q\ge11$
E. The correct answer is missing

6a15. For the given game model, for which values of n and m, $(i_0,j_0)=(2,2)$ is the best strategy?

$$\begin{bmatrix}5&m&10\\n&8&14\\10&6&7\end{bmatrix}$$

A. $n\le8$ *and* $m\ge8$
B. $n\le8$ *and* $m\le8$
C. $n\ge8$ *and* $m\le8$
D. $n\ge8$ *and* $m\ge8$
E. The correct answer is missing

6a16. What is the form of $u_{1opt}(t)$ -Ý, $u_{2opt}(t)$ if

$$I=\int_0^T u_2^2(t)dt\to\min_{u_1(t),u_2(t)},$$

$$\begin{pmatrix}\dot x_1(t)\\\dot x_2(t)\end{pmatrix}=\begin{bmatrix}1&2\\0&1\end{bmatrix}\cdot\begin{pmatrix}x_1(t)\\x_2(t)\end{pmatrix}+\begin{bmatrix}0&1\\1&1\end{bmatrix}\cdot\begin{pmatrix}u_1(t)\\u_2(t)\end{pmatrix},$$

$$c(u_1(t),u_2(t))=u_1^2(t)+u_2^3(t)\le0,$$

whereas $\psi_1(t)$ and $\psi_2(t)$ are conjugated variables, and μ - is a special multiplier.

A. $u_{1opt}(t)=-\frac{1}{2}\cdot\frac{\psi_2(t)}{\mu},\ u_{2opt}(t)=\frac{1\pm\sqrt{1+12(\psi_1(t)+\psi_2(t))}}{6\mu}$

B. $u_{1opt}(t)=\psi_1(t)+\psi_2(t),\ u_{2opt}(t)=\frac{1}{2\mu}(\psi_1(t)-\psi_2(t))$

C. $u_{1opt}(t)=\frac{\psi_1(t)}{\mu},\ u_{2opt}(t)=\psi_1(t)\cdot\psi_2(t)$

D. $u_{1opt}(t) = \psi_1(t), u_{2opt}(t) = \frac{\psi_1(t)}{\psi_2(t)} \cdot \mu$

E. *The correct answer is missing*

6a17. Which is the system of complement variables if

$$I = \int_0^T u^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 1 \\ 2 \end{pmatrix} \cdot u(t).$$

A. $\dot{\psi}_1(t) = -\psi_1(t) + \psi_2(t),\ \dot{\psi}_2(t) = = \psi_1(t) - \psi_2(t)$

B. $\dot{\psi}_1(t) = \psi_1(t) \cdot \psi_2(t),\ \dot{\psi}_2(t) = \frac{\psi_1(t)}{\psi_2(t)}$

C. $\dot{\psi}_1(t) = -\psi_1(t) \cdot \psi_2(t),\ \dot{\psi}_2(t) = -\frac{\psi_1(t)}{\psi_2(t)}$

D. $\dot{\psi}_1(t) = -2 \cdot \psi_1(t) - \psi_2(t),\ \dot{\psi}_2(t) = = -\psi_1(t) - 2 \cdot \psi_2(t)$

E. *The correct answer is missing*

6a18. What is the form of $u_{opt}(t)$ if

$$I = \int_0^T x_1^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 2 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} \cdot u^2(t),$$

$$c(x_1(t)) = x_1^2(t) + x_1(t) \le 0,$$

whereas $\psi_1(t)$ and $\psi_2(t)$ are conjugated variables, and μ - is a special multiplier.

A. $u_{opt}(t) = \frac{\psi_1(t)}{\mu + \psi_2(t)}$

B. $u_{opt}(t) = \frac{\psi_2(t)}{\mu + \psi_1(t)}$

C. $u_{opt}(t) = \psi_1(t) + \frac{\psi_2(t)}{\mu}$

D. $u_{opt}(t) = -2 \cdot (1 + 2x_1(t)) \cdot \frac{\mu}{\psi_2(t)}$

E. *The correct answer is missing*

6a19. What category is $c(x_1(t)) = x_1^2(t) + x_1(t) \le 0$ limitation if

$$I = \int_0^T x_1^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 2 & 2 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} \cdot u^2(t).$$

A. *1st category*

B. *2nd category*

C. *3rd category*

D. *4th category*

E. *7th category*

6a20. If j-th component of optimal solution of dual canonic problem of linear programming equals zero (y_j=0), then direct problem's appropriate limitation is:

A. > 0

B. < 0

C. $= 0$

D. ≥ 0

E. *The correct answer is missing*

6a21. If j-th component of optimal solution of dual canonic problem of linear programming doesn't equal zero ($y_j \ne 0$), then direct problem's appropriate limitation is:

A. > 0,

B. $= 0$,

C. < 0,

D. $= 8$,

E. *The correct answer is missing*

6a22. For the solution of canonic problem of linear programming which condition must take place (n is the number of variables of direct problem, and m is the number of limitations)?

A. $x_i^{\text{direct}} = -(sd)_{m+i}^{\text{dual}}$

B. $x_i^{\text{direct}} = (sd)_{n+i}^{\text{dual}}$

C. $x_i^{\text{direct}} = -(sd)_{n+i}^{\text{dual}}$

D. $x_i^{\text{direct}} = (sd)_{m+i}^{\text{dual}}$

E. *The correct answer is missing*

6a23. Which condition is valid for the optimal solution of canonical problems of linear programming (n-is the number of variables of direct problem and m-is the number of limitations)?

A. $y_i^{\text{dual}} = (sd)_{n+i}^{\text{direct}}$

B. $y_i^{\text{dual}} = -(sd)_{n+i}^{\text{direct}}$

C. $y_i^{\text{dual}} = -(sd)_{m+i}^{\text{direct}}$

D. $y_i^{\text{dual}} = (sd)_{m+i}^{\text{direct}}$

E. *The correct answer is missing*

6a24. In case of which value of a_{33} cell

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 2 & 2 & 4 \\ 1 & 0 & a_{33} \end{bmatrix}$$

matrix can be reduced to diagonal form?

A. $a_{33} = 1$,

B. $a_{33} = 2$,

C. $a_{33} \ne 1$,

D. $a_{33} \ne 1$ *or* $a_{33} \ne 2$,

E. *The correct answer is missing*

6a25. P_2 coefficient of characteristic polynomial $P_0 \cdot \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$ of the following matrix

$$A = \begin{bmatrix} 2 & 0 & 0 \\ 1 & 1 & 2 \\ 1 & 0 & 3 \end{bmatrix}$$

equals
A. +11
B. 6
C. -11
D. 0
E. -6

6a26. What does $\Psi^T(t) \cdot \Psi(t)|_{t=2}$ equal if it is known that

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 0 & -1 & 2 \\ 1 & 0 & 3 \\ -2 & -3 & 0 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix}, \begin{matrix} x_1(0)=1, \\ x_2(0)=2, \\ x_3(0)=0, \end{matrix}$$

and $\Psi(t) = (\psi_1(t), \psi_2(t), \psi_3(t))^T$ is complement variable vector?
A. -5
B. -3
C. 0
D. 3
E. 5

6a27. What does $X^T(t) \cdot X(t)|_{t=3}$ equal if it is known that

$$\begin{pmatrix} \dot{\psi}_1(t) \\ \dot{\psi}_2(t) \\ \dot{\psi}_3(t) \end{pmatrix} = \begin{bmatrix} 0 & 2 & -1 \\ -2 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \cdot \begin{pmatrix} \psi_1(t) \\ \psi_2(t) \\ \psi_3(t) \end{pmatrix}, \begin{matrix} \psi_1(0)=2, \\ \psi_2(0)=1, \\ \psi_3(0)=3, \end{matrix}$$

and $X(t) = (x_1(t), x_2(t), x_3(t))^T$ is the variable vector of the state?
A. 6
B. 8
C. 11
D. 14
E. 17

6a28. The reminder of the division of the polynomial $15x^4 - 14x^3 + 8x^2 - 7x - 2$ by the binomial $x - 1$ is:
A. 3
B. 4
C. 0
D. -8
E. -2

6a29. What point belongs to the graph of the function $f(x) = 3x^4 - 2x + 1$?
A. (5,-1)
B. (0,3)
C. (-1,6)
D. (1,4)
E. (-2,-1)

6a30. What value does the derivative of the function $f(x) = x(x-1)(x-2)(x-3)(x-4)(x-5)$ have in the point $x = 0$?
A. -200
B. -120
C. -50
D. 100
E. 150

6a31. What number is the eigenvalue of the matrix $A = \begin{pmatrix} 5 & 1 \\ 2 & 4 \end{pmatrix}$?
A. 5
B. 2
C. -1
D. 3
E. 8

6a32. For what value of α parameter $M = \begin{pmatrix} 3 & 7 & 1 \\ 2 & -3 & 0 \\ 1 & \alpha & 1 \end{pmatrix}$ matrix does not have inverse?
A. 3
B. 0
C. -2
D. 10
E. 15

6a33. For what value of a parameter $f(x) = \begin{cases} \dfrac{\sin 3x}{x}, x \neq 0 \\ a, x = 0 \end{cases}$ function will be continuous?
A. 0
B. 1
C. -1
D. 4
E. 3

6a34. Arrange the following integrals in ascending order.

$$I_1 = \int_1^2 \frac{dx}{\sqrt{x}+1} \quad I_2 = \int_1^2 \frac{2\sin x}{\sqrt[3]{x}}dx$$

$$I_3 = \int_1^2 \frac{dx}{x+e^x}$$

A. I_3, I_1, I_2
B. I_2, I_3, I_1
C. I_1, I_2, I_3
D. I_2, I_1, I_3
E. I_1, I_3, I_2

6a35. How many real roots does $f'(x)=0$ equation have where $f(x)=(x-1)(x-2)(x-3)(x-4)(x-5)$

A. 4
B. 3
C. 2
D. 1
E. 0

6a36. For what value of a_{22} element $A=\begin{bmatrix} 2 & 0 & 0 \\ 1 & a_{22} & 0 \\ 2 & 1 & 1 \end{bmatrix}$ matrix can be reduced to diagonal form?

A. $a_{22}=2$
B. $a_{22}=1$
C. $a_{22}\neq 1$
D. $a_{22}\neq 2$ *and* $a_{22}\neq 1$
E. *The correct answer is missing*

6a37. For what values of c_{11} and c_{21} elements $A=\begin{bmatrix} 3 & 0 & 0 \\ 0 & 2 & 0 \\ 0 & 0 & 1 \end{bmatrix}$, $C=\begin{bmatrix} c_{11} & 1 & 0 \\ c_{21} & 1 & 2 \end{bmatrix}$ matrix system will not be fully observable?

A. $c_{11}\neq 0$, $c_{21}=0$
B. $c_{11}=0$, $c_{21}=0$
C. $c_{11}=0$, $c_{21}\neq 0$
D. $c_{11}\neq 0$, $c_{21}\neq 0$
E. *The correct answer is missing*

6a38. What category is

$c(x_1(t))=x_1^2(t)+x_1(t)\leq 0$ limitation if

$$I=\int_0^T x_1^2(t)dt\to\min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix}=\begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix}\cdot\begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix}+\begin{pmatrix} 0 \\ 2 \end{pmatrix}\cdot u^3(t).$$

A. *1st category*
B. *3rd category*
C. *4th category*
D. *2nd category*
E. *5th category*

6a39. For what values of b_{31} and b_{32} elements $A=\begin{bmatrix} 2 & 0 & 1 \\ 1 & 2 & 0 \\ 0 & 1 & 3 \end{bmatrix}$, $B=\begin{bmatrix} 1 & 2 \\ 2 & 0 \\ b_{31} & b_{32} \end{bmatrix}$ matrix system will not be fully controllable?

A. $b_{31}=1$, $b_{32}=2$,
B. $b_{31}=2$, $b_{32}=0$,
C. $b_{31}=0$, $b_{32}=0$,
D. $b_{31}=1$, $b_{32}=0$,
E. $b_{31}=0$, $b_{32}=1$,

6a40. What is the view of $u_{1opt}(t)$, $u_{2opt}(t)$ if

$$I=\int_0^T (u_1^2(t)+u_2^2(t))dt\to\min_{u_1(t),u_2(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix}=\begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}\cdot\begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix}+\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}\cdot\begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix},$$

A. $u_{1opt}(t)=\psi_1(t)+\psi_2(t)$, $u_{2opt}(t)=$ $=\psi_1(t)-\psi_2(t)$
B. $u_{1opt}(t)=\psi_1(t)\cdot\psi_2(t)$, $u_{2opt}(t)=\dfrac{\psi_1(t)}{\psi_2(t)}$
C. $u_{1opt}(t)=\dfrac{\psi_2(t)}{\psi_1(t)}$, $u_{2opt}(t)=0$
D. $u_{1opt}(t)=\dfrac{1}{2}(\psi_1(t)+\psi_2(t))$, $u_{2opt}(t)=$ $=\dfrac{1}{2}\psi_2(t)$
E. *The correct answer is missing*

6a41. Which statement is correct?

A. *Direct and dual problems have the same number of variables*
B. *The objective functions of direct and dual problems have the same value*
C. *Direct and dual problems have the same number of limitations*
D. *None*
E. *All the answers are correct*

6a42. For what value of a_{22} element $A=\begin{bmatrix} 2 & 0 & 0 \\ 2 & a_{22} & 0 \\ 2 & 2 & 1 \end{bmatrix}$ matrix can be reduced to diagonal form?

A. $a_{22}=2$
B. $a_{22}=1$
C. $a_{22}\neq 1$
D. $a_{22}\neq 2$ *or* $a_{22}\neq 1$
E. *The correct answer is missing*

6a43. For what values of c_{11} and c_{21} elements $A=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 2 & 0 \\ 0 & 0 & 3 \end{bmatrix}$, $C=\begin{bmatrix} c_{11} & 2 & 0 \\ c_{21} & 3 & 2 \end{bmatrix}$ matrix system will not be fully observable?

A. $c_{11}\neq 0$, $c_{21}=0$
B. $c_{11}=0$, $c_{21}=0$
C. $c_{11}=0$, $c_{21}\neq 0$
D. $c_{11}\neq 0$, $c_{21}\neq 0$
E. *The correct answer is missing*

6a44. What is $X^T(t)\cdot X(t)_{|t=3}$ equal to, if known that

$$\begin{pmatrix}\dot\psi_1(t)\\ \dot\psi_2(t)\\ \dot\psi_3(t)\end{pmatrix}=\begin{bmatrix}0 & 2 & -1\\ -2 & 0 & 1\\ 1 & -1 & 0\end{bmatrix}\cdot\begin{pmatrix}\psi_1(t)\\ \psi_2(t)\\ \psi_3(t)\end{pmatrix},\quad \begin{matrix}\psi_1(0)=0,\\ \psi_2(0)=1,\\ \psi_3(0)=3,\end{matrix}$$

and $X(t)=(x_1(t),x_2(t),x_3(t))^T$ is conjugate variable vector?

A. 0
B. 2
C. 6
D. 10
E. 14

6a45. Which is the conjugate variable system if

$$I=\int_0^T u^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix}\dot x_1(t)\\ \dot x_2(t)\end{pmatrix}=\begin{bmatrix}1 & 3\\ 3 & 1\end{bmatrix}\cdot\begin{pmatrix}x_1(t)\\ x_2(t)\end{pmatrix}+\begin{pmatrix}2\\ 1\end{pmatrix}\cdot u(t)?$$

A. $\dot\psi_1(t)=-\psi_1(t)-3\psi_2(t),\ \dot\psi_2(t)=$
$=-3\psi_1(t)-\psi_2(t)$

B. $\dot\psi_1(t)=-\psi_1(t)+\psi_2(t),\ \dot\psi_2(t)=$
$=\psi_1(t)-\psi_2(t)$

C. $\dot\psi_1(t)=\psi_1(t)\cdot\psi_2(t),\ \dot\psi_2(t)=\dfrac{\psi_1(t)}{\psi_2(t)}$

D. $\dot\psi_1(t)=-\dfrac{\psi_2(t)}{\psi_1(t)},\ \dot\psi_2(t)=\psi_1(t)\cdot\psi_2(t)$

E. *The correct answer is missing*

6a46. What does $\Psi^T(t)\cdot\Psi(t)_{|t=2}$ equal to if known that

$$\begin{pmatrix}\dot x_1(t)\\ \dot x_2(t)\\ \dot x_3(t)\end{pmatrix}=\begin{bmatrix}0 & 1 & -1\\ -1 & 0 & 2\\ 1 & -2 & 0\end{bmatrix}\cdot\begin{pmatrix}x_1(t)\\ x_2(t)\\ x_3(t)\end{pmatrix},\quad \begin{matrix}x_1(0)=1,\\ x_2(0)=2,\\ x_3(0)=-3,\end{matrix}$$

and $\Psi(t)=(\psi_1(t),\psi_2(t),\psi_3(t))^T$ is the conjugate variable vector?

A. 14
B. 10
C. 6
D. 2
E. 0

6a47. P_3 coefficient of characteristic polynomial $P_0\cdot\lambda^3+P_1\cdot\lambda^2+P_2\cdot\lambda+P_3=0$ of the following matrix

$$A=\begin{bmatrix}1 & 0 & 0\\ 2 & 3 & 1\\ 2 & 0 & 4\end{bmatrix}$$

equals

A. 12
B. 5
C. 4
D. 3
E. 1

6a48. For which values of b_{11}, b_{21} and b_{31} elements $A=\begin{bmatrix}1 & 2 & 0\\ 2 & 1 & 1\\ 1 & 1 & 2\end{bmatrix}$, $B=\begin{bmatrix}b_{11} & 1\\ b_{21} & 2\\ b_{31} & 3\end{bmatrix}$ matrix system will not be normal system?

A. $b_{11}\neq 0,\ b_{21}=0,\ b_{31}\neq 0$
B. $b_{11}=0,\ b_{21}=0,\ b_{31}\neq 0$
C. $b_{11}=0,\ b_{21}=0,\ b_{31}=0$
D. $b_{11}=1,\ b_{21}=0,\ b_{31}=2$
E. $b_{11}=2,\ b_{21}=1,\ b_{31}=0$

6a49. How many real roots has the equation $\dfrac{df}{dx}(x)=0$ for the function $f(x)=x^6-6x^4+x+2$?

A. 0
B. 1
C. 2
D. 3
E. 4

6a50. Calculate the integral $\int_1^4 |x-2|dx$.

A. 3
B. 2.5
C. 2
D. 1.5
E. 1

6a51. For which α the rank of matrix $A=\begin{pmatrix}\alpha & 1 & 1\\ 1 & \alpha & 1\\ 1 & 1 & \alpha\end{pmatrix}$ is equal to 2?

A. -2
B. 0
C. 1
D. 3
E. All the answers are correct

6a52. How many significant digits of $lg 2$ should be taken for determination of the roots of equation $x^2-2x+lg2=0$ with 4 digit accuracy?

A. 2
B. 4
C. 6
D. 8
E. 10

6a53. Assume $M=\begin{pmatrix}2 & 4\\ 1 & 2\end{pmatrix}$. The equality $M^6=kM$ holds if k is:

A. 2^6
B. 2^8
C. 2^{10}
D. 2^{12}
E. 2^{14}

6a54. From the given points A, B, C, D which one is the closest to $y = 3x + 2$ line?

A. A(1,2)
B. B(3,2)
C. C(0,-1)
D. D(-1,-2)
E. C and D answers are correct

6a55. Find $\lim\limits_{n\to\infty}\sum\limits_{k=1}^{n}\dfrac{1}{n\left(1+\dfrac{k}{n}\right)}$

A. 1
B. ln2
C. 0.5
D. 0
E. The correct answer is missing

6a56. Assume $f(x) = e^x \cos 2x$. What second degree polynomial gives the best approximation of function f in the neighborhood of 0?

A. $P_2 = 1 + 0.2x + x^2$
B. $P_2 = 1 + x - 1.5x^2$
C. $P_2 = 1 - 2.5x + 3x^2$
D. $P_2 = 2 - x + 3x^2$
E. The correct answer is missing

6a57. Assume $f\left(x + \dfrac{1}{x}\right) = x^2 + \dfrac{1}{x^2}$ for all $x \neq 0$. In that case f function is defined by the following expression:

A. $x^2 - 2$
B. $2x^2 + 1$
C. $x^2 + 4$
D. $4x - x^2$
E. $3x + x^2 + 1$

6a58. For $f(x) = \begin{cases} e^x, & x > 0 \\ a + x, & x \le 0 \end{cases}$ function to be constant, α constant value must equal

A. 2
B. 1
C. 0
D. -1
E. -2

6a59. What does $\lim\limits_{n\to\infty}\sqrt[2n]{1 + x^{2n}}$ limit equal?

A. $|x| + 1$
B. $min(2, |x|)$
C. $max(1, |x|)$
D. 1
E. $2|x|$

6a60. In case of what β

$$\begin{cases} x_1 + x_2 + x_3 = 0 \\ x_1 + \beta x_2 + x_3 = 0 \\ x_1 + x_2 + 2x_3 = 0 \end{cases}$$

system has more than three solutions?

A. 4
B. 3
C. 2
D. 1
E. 0

6a61. Find $\lim\limits_{n\to\infty}\int\limits_0^{\infty}\dfrac{dx}{x^n + 1}$ limit

A. 1
B. 2
C. 3
D. 4
E. 5

6a62. Assume random value distribution function is given by $F(x) = A(B + arctg\,2x)$ formula. Define A and B constant values.

A. $A = 1,\ B = 0.5\pi$
B $A = \pi^{-1},\ B = 0.5\pi$
C. $A = (2\pi)^{-1},\ B = \pi$
D. $A = \pi^{-1},\ B = 1$
E. $A = 2\pi^{-1},\ B = \pi$

6a63. Assume *A* matrix looks as follows:

$$A = \begin{pmatrix} 0.2 & 5 \\ \alpha & 0.1 \end{pmatrix}$$

What value of α of $\bar{x} = A\bar{x}$ system can be solved by sequential approximation method?

A. 2
B. 1
C. 0
D. -1
E. -2

6a64. Which of $A(3,5)$, $B(2,6)$, $C(-1,1)$, $D(2,0)$, $E(5,0)$ points is the nearest to $y = 3x + 1$?

A. A
B. B
C. C
D. D
E. E

6a65. Arrange the integrals in ascending order:

$$I_1 = \int\limits_0^1 e^{-x^2}dx,\ I_2 = \int\limits_0^1 xe^{-x^2}dx,\ I_3 = \int\limits_0^1 e^{-x^2}\sin x dx$$

A . I_1, I_2, I_3
B . I_3, I_2, I_1

C. I_2, I_1, I_3

D. I_3, I_1, I_2

E. I_2, I_3, I_1

6a66. For what value a the function

$$f(x) = \begin{cases} e^{2x}, & x > 0 \\ 1 + ax^2, & x \le 0 \end{cases}$$

will be continuously differentiable?

A. 2
B. 1
C. 0
D. -1
E. None

6a67. Find the limit $\lim\limits_{n\to\infty} \sqrt[2n]{1+x^{2n}}$

A. $|x|+1$

B. $min(2,|x|)$

C. $max(1,|x|)$

D. 1

E. x

6a68. For what value β $\begin{cases} x_1 + x_2 + 3x_3 = 2 \\ x_1 + x_2 + x_3 = \beta \\ x_1 + x_2 + 2x_3 = 0 \end{cases}$ the system has a solution?

A. -2
B. -0.5
C. 1
D. -1
E. 0

6a69. Find the limit $\lim\limits_{n\to\infty} \int_0^2 \frac{x^n - x^{-n}}{x^n + x^{-n}} dx$.

A. 1
B. 2
C. -2
D. 0
E. -1

6a70. For what values of the constants A, B the distribution function of the variate may be given by the formula $F(x) = A + B arcctg\, 2x$?

A. $A = 0,\ B = -\pi^{-1}$

B. $A = \pi^{-1},\ B = 0.5\pi$

C. $A = (2\pi)^{-1},\ B = \pi$

D. $A = \pi^{-1},\ B = 1$

E. There are no such values

6a71. For what values α all eigenvalues of the matrix A are real $A = \begin{pmatrix} 2 & -1 \\ \alpha & 1 \end{pmatrix}$?

A. -1
B. 1
C. 4
D. 7
E. 10

6a72. There are five points on the plane: $A(3,5)$, $B(2,6)$, $C(-1,1)$, $D(2,0)$, $E(3,-2)$. For what point the distance from the parabola $y = x^2 - 1$ will be minimal?

A. A
B. B
C. C
D. D
E. E

6a73. For what value of a_{22} element

$$A = \begin{bmatrix} 3 & 0 & 0 \\ 2 & a_{22} & 0 \\ 2 & 2 & 1 \end{bmatrix}$$

matrix can be reduced to diagonal form?

A. $a_{22} = 3$

B. $a_{22} \ne 3,\ a_{22} \ne 1$

C. $a_{22} = 1$

D. $a_{22} \ne 1$

E. The correct answer is missing

6a74. For what values of b_{31} and b_{32} elements

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 1 & 2 & 0 \\ 0 & 1 & 3 \end{bmatrix},\quad B = \begin{bmatrix} 3 & 2 \\ 1 & 2 \\ b_{31} & b_{32} \end{bmatrix}$$

matrix system will not be fully controllable?

A. $b_{31}=0$ $b_{32}=0$
B. $b_{31}=2$, $b_{32}=0$
C. $b_{31}=1$, $b_{32}=0$
D. $b_{31}=0$, $b_{32}=1$
E. $b_{31}=1$, $b_{32}=2$

6a75. Which is the conjugate variable system if

$$I = \int_0^T u^2(t)dt \to \min_{u(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 1 & 2 \\ 2 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 1 \\ 2 \end{pmatrix} \cdot u(t).$$

A. $\dot{\psi}_1(t) = -\psi_1(t) + \psi_2(t),\ \dot{\psi}_2(t) = = \psi_1(t) - \psi_2(t)$

B. $\dot{\psi}_1(t) = -\psi_1(t) - 2\psi_2(t),\ \dot{\psi}_2(t) = = -2\psi_1(t) - \psi_2(t)$

C. $\dot{\psi}_1(t) = \psi_1(t) \cdot \psi_2(t),\ \dot{\psi}_2(t) = \frac{\psi_1(t)}{\psi_2(t)}$

D. $\dot{\psi}_1(t) = -\frac{\psi_2(t)}{\psi_1(t)},\ \dot{\psi}_2(t) = = \psi_1(t) \cdot \psi_2(t)$

E. The correct answer is missing

6a76. P_3 coefficient of characteristic polynomial $P_0 \cdot \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$ of the following matrix

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 2 & 3 & 1 \\ 2 & 0 & 2 \end{bmatrix}$$

equals:

A. 5
B. 1
C. 4
D. 3
E. 6

6a77. For what values of c_{11} and c_{21} elements

$$A = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 3 & 0 \\ 0 & 0 & 4 \end{bmatrix}, \; C = \begin{bmatrix} c_{11} & 4 & 0 \\ c_{21} & 1 & 2 \end{bmatrix}$$

matrix system will not be fully observable?

A. $c_{11} \neq 0$, $c_{21}=0$
B. $c_{11}=0$, $c_{21} \neq 0$
C. $c_{11} \neq 0$, $c_{21} \neq 0$
D. $c_{11}=0$, $c_{21}=0$
E. The correct answer is missing

6a78. What is $X^T(t) \cdot X(t)\big|_{t=3}$ equal to, if known that

$$\begin{pmatrix} \dot\psi_1(t) \\ \dot\psi_2(t) \\ \dot\psi_3(t) \end{pmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 2 \\ 1 & -2 & 0 \end{bmatrix} \cdot \begin{pmatrix} \psi_1(t) \\ \psi_2(t) \\ \psi_3(t) \end{pmatrix}, \; \begin{matrix} \psi_1(0)=0, \\ \psi_2(0)=1, \\ \psi_3(0)=2, \end{matrix}$$

and $\Psi(t) = (\psi_1(t), \psi_2(t), \psi_3(t))^T$ is conjugate variable vector?

A. 2
B. 5
C. 6
D. 14
E. 0

6a79. What is $\Psi^T(t) \cdot \Psi(t)\big|_{t=2}$ equal to, if known that

$$\begin{pmatrix} \dot x_1(t) \\ \dot x_2(t) \\ \dot x_3(t) \end{pmatrix} = \begin{bmatrix} 0 & 2 & -1 \\ -2 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix}, \; \begin{matrix} x_1(0)=3, \\ x_2(0)=1, \\ x_3(0)=0, \end{matrix}$$

and $\Psi(t) = (\psi_1(t), \psi_2(t), \psi_3(t))^T$ is conjugate variable vector?

A. 2
B. 14
C. 10
D. 6
E. 0

6a80. For which values of b_{11}, b_{21} and b_{31} elements

$$A = \begin{bmatrix} 1 & 2 & 0 \\ 2 & 1 & 2 \\ 1 & 2 & 1 \end{bmatrix}, \; B = \begin{bmatrix} b_{11} & 1 \\ b_{21} & 3 \\ b_{31} & 2 \end{bmatrix}$$

matrix system will not be normal system?

A. $b_{11} \neq 0$, $b_{21}=0$, $b_{31} \neq 0$
B. $b_{11}=0$, $b_{21}=0$, $b_{31} \neq 0$
C. $b_{11}=0$ $b_{21}=0$ $b_{31}=0$
D. $b_{11}=1$, $b_{21}=0$, $b_{31}=2$
E. $b_{11}=2$, $b_{21}=1$, $b_{31}=0$

6a81. For what value of β parameter

$$M = \begin{bmatrix} 2 & 4 & 1 \\ 0 & \beta & 2 \\ 1 & 3 & 2 \end{bmatrix}$$

matrix does not have inverse M^{-1}?

A. 4/3
B. 1
C. 2
D. 4
E. 3

6a82. For what value of β parameter P_3 coefficient of characteristic polynomial $P(\lambda)=\lambda^3+P_1\lambda^2+P_2\lambda+P_3=0$ of the following matrix equals 1?

$$M = \begin{bmatrix} 1 & 2 & \beta \\ 2 & 3 & 1 \\ 1 & 4 & 2 \end{bmatrix}$$

A. 2
B. 4
C. 1
D. 3
E. 5

6a83. What equals A_{5x5} matrix's characteristic polynomial coefficient of the term which contains λ if $\lambda_1=1$, $\lambda_2=1$, $\lambda_3=2$, $\lambda_4=-1$, $\lambda_5=-2$ are the eigenvalues of A_{5x5}?

A. 2
B. 4
C. 1
D. -4
E. 3

6a84. What does A_{4x4} determinant of matrix equal if $\lambda_1=2$, $\lambda_2=-1$, $\lambda_3=3$, $\lambda_4=0$ are the intrinsic numbers of A_{4x4} matrix?

A. -1
B. 2
C. 4
D. 3

E. 0

6a85. The following linear programming problem has:

$$L = x_1 + 1.5x_2 \to \max_{x_1,\, x_2} \ ,$$

$$\begin{cases} c_1(x) = 3.5x_1 + 3x_2 \le 21 \\ c_2(x) = 2x_1 + 10x_2 \le 10 \\ c_3(x) = x_1 \ge 0,\ c_4 = x_2 \ge 0 \end{cases}$$

A. One solution
B. Two solutions
C. Unlimited solutions
D. Solutions with infinite set
E. Does not have a solution

6a86. Which is the nonlinear programming solution of the following Lagrange problem?

$$L = x_2^2 + (x_1 - 1)^2 \to \max_{x_1, x_2},$$

$$c_1(x) = x_1^2 + x_2^2 - 1 = 0:$$

A. L_{max}=6
B. L_{max}=4
C. L_{max}=7
D. L_{max}=-3
E. L_{max}=5

6a87. Which is the nonlinear programming solution of the following Kuhn-Tucker problem?

$$L(x) = x_2 \to \min_{x_2},$$

$$c_1(x) = x_1^2 + x_2^2 - 1 \le 0,$$

$$c_2(x) = -x_1 + x_2^2,$$

$$c_3(x) = x_1 + x_2 \ge 0:$$

A. L_{min}=1
B. L_{min}=2
C. L_{min}=3
D. L_{min}=4
E. L_{min}=$-\sqrt{2}/2$

6a88. For which values of b_{11}, b_{22} and b_{31} elements

$$A = \begin{bmatrix} 1 & 2 & 0 \\ 0 & 1 & 2 \\ 2 & 1 & 1 \end{bmatrix}, \qquad B = \begin{bmatrix} b_{11} & 0 \\ 0 & b_{22} \\ b_{31} & 1 \end{bmatrix}$$

matrix system will not be a normal system?

A. b_{11}=0, b_{22}=0, b_{31}=0
B. b_{11}=1, b_{22}=0, b_{31}=1
C. b_{11}=0, b_{22}=1, b_{31}=1
D. b_{11}=0, b_{31}=0, b_{22} is an arbitrary number
E. b_{11}=1, b_{22}=1, b_{31}=1

6a89. For what value of α parameter, P_2 coefficient of characteristic polynomial $P(\alpha) = det[A - \lambda E] = \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$ of the matrix $A = \begin{bmatrix} 1 & 2 & 0 \\ 2 & \alpha & 1 \\ 0 & 1 & 2 \end{bmatrix}$ equals zero?

A. 1
B. -3
C. 4.5
D. 3
E. -1

6a90. For what value of β parameter, $M = \begin{bmatrix} 0 & 1 & 2 \\ \beta & 2 & 1 \\ 1 & 2 & 3 \end{bmatrix}$ matrix is splitting

A. 1
B. 2
C. 3
D. 4
E. 5

6a91. What equals A_{4x4} matrix's characteristic polynomial coefficient of the term which contains λ^3 if λ_1=2, λ_2=1,λ_3= -1,λ_4= -2 are the eigenvalues of A_{4x4}?

A. 2
B. 1
C. -1
D. -2
E. 0

6a92. What does A_{5x5} determinant of matrix equal if λ_1=1,λ_2=2,λ_3=3,λ_4=4,λ_5=5 are the intrinsic numbers of A_{5x5} matrix?

A. 12
B. 120
C. 1.2
D. 0.12
E. 0

6a93. Which is linear programming solution of the following problem?

$$L = x_1 + x_2 \to \max_{x_1, x_2},$$

$$C_1(x) = 7x_1 + 6x_2 \le 42,$$

$$C_2(x) = x_1 + 5x_2 \le 5,$$

$$C_3 = x_1 \ge 0,$$

$$C_4 = x_2 \ge 0.$$

A. 5
B. 1
C. 0
D. 4
E. 2

6a94. Which is the nonlinear programming solution of the following Lagrange problem?

$$L = x_1 + x_2^2 - 1 \to \max_{x_1, x_2},$$
$$C_1(x) = x_1^2 + x_2^2 - 1 = 0:$$

A. 0.75
B. 0.125
C. 0
D. 0.5
E. 0.25

6a95. From matrices

$$A_1 = \begin{bmatrix} 2 & 4 \\ 6 & 8 \end{bmatrix}, \quad A_2 = \begin{bmatrix} 0 & 1 \\ 2 & 4 \end{bmatrix}, \quad A_3 = \begin{bmatrix} 1 & 0 \\ 2 & 3 \end{bmatrix}$$

to which one corresponds

$$\phi(t) = \begin{bmatrix} e^t & 0 \\ (-e^t + e^{3t}) & e^{3t} \end{bmatrix}$$

fundamental matrix?

A. A_3
B. A_2
C. A_1
D. All the answers are correct
E. The correct answer is missing

6a96. It is known that for the problem of some linear optimal performance, the function of optimal control is

$$U_{opt}(t) = sign\left(\psi_1(0) \cdot \frac{t^2}{2} - \psi_2(0) \cdot t + \psi_3(0)\right),$$

where $(\psi_1(0), \psi_2(0), \psi_3(0))^T$ is the vector of initial values of complement variables. How many constancy range can $U_{opt}(t)$ have?

A. 1 or 2
B. 1 or 2 or 3
C. 2 or 3
D. 1 or 3
E. The correct answer is missing

6a97. For what value of α parameter P_1 coefficient of characteristic polynomial $P(\alpha) = det[A - \lambda E] = \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$ of the following matrix equals 1?

$$A = \begin{bmatrix} 1 & 2 & 0 \\ 2 & \alpha & 1 \\ 0 & 1 & 2 \end{bmatrix}$$

A. 1
B. -2
C. 4.5
D. 3
E. -1

6a98. For what value of β parameter,

$$M = \begin{bmatrix} 0 & 1 & 1 \\ \beta & 2 & 1 \\ 1 & 2 & 3 \end{bmatrix}$$ matrix is splitting?

A. 1
B. 2
C. 3
D. -1
E. 5

6a99. What equals A_{4x4} matrix's characteristic polynomial coefficient of the term which contains λ^2 if $\lambda_1=2$, $\lambda_2=1$, $\lambda_3=-1$, $\lambda_4=-2$ are the eigenvalues of A_{4x4}?

A. 2
B. 1
C. -5
D. -2
E. 0

6a100. What does A_{5x5} determinant of matrix equal if $\lambda_1=1$, $\lambda_2=2$, $\lambda_3=3$, $\lambda_4=-2$, $\lambda_5=-1$ are the intrinsic numbers of A_{5x5} matrix?

A. 12
B. 120
C. 1.2
D. 0.12
E. 0

6a101. Which is the solution of the following linear programming problem?

$$L = x_1 + x_2 \to \min_{x_1, x_2},$$
$$C_1(x) = 7x_1 + 6x_2 \le 42,$$
$$C_2(x) = x_1 + 5x_2 \le 5,$$
$$C_3 = x_1 \ge 0,$$
$$C_4 = x_2 \ge 0$$

A. 5
B. 1
C. 0
D. 4
E. 2

6a102.

Calculate the integral $I = \int_{-1}^{2} x[x]dx$. Here $[x]$ is an integer part of x (the greatest integer number is not more than the real number x (floor function))

A. 1.5
B. 2
C. 2.5
D. 3
E. 3.5

6a103. Calculate the function $f(x) = \lim_{n\to\infty} \frac{e^{nx}}{1+e^{nx}}$.

A. $f(x) = \begin{cases} 1, & x > 0 \\ 0.5, & x = 0 \\ 0, & x < 0 \end{cases}$

B. $f(x)=\begin{cases}1, & x>0\\ 0, & x=0\\ 1, & x<0\end{cases}$

C. $f(x)=\begin{cases}0, & x>0\\ 0.5, & x=0\\ 0.5, & x<0\end{cases}$

D. $f(x)=\begin{cases}1, & x>0\\ 1, & x=0\\ 0, & x<0\end{cases}$

E. $f(x)=\begin{cases}0.5, & x>0\\ 0.5, & x=0\\ 0, & x<0\end{cases}$

6a104. Calculate $\lim\limits_{n\to\infty}\sin\left(\pi\sqrt{n^2+1}\right)$

A. –1
B. 1
C. 0.5
D. –0.5
E. 0

6a105. Let $f_1(x)=\dfrac{x}{\sqrt{1+x^2}}$. Let's denote $f_2(x)=f(f(x))$, $f_3(x)=f(f(f(x)))$. For arbitrary natural number n there is $f_n(x)=f(f(\ldots f(x)\ldots))$. Calculate $\lim\limits_{n\to\infty}f_n(-2)$.

A. –3
B. –2
C. –1
D. 0
E. 1

6a106. What point belongs to the bounded domain with $y=x^2$ and $y=x+6$ boundary functions?

A. (–3,0)
B. (–2,1)
***C.** (–1,2)*
D. (2,1)
E. (3,0)

6a107. For what values of a and b the function

$$f(x)=\begin{cases}x^3+a, & x>2\\ bx+8, & x\le 2\end{cases}$$

is continuously differentiable?

A. $a=10,\ b=20$
B. $a=24,\ b=12$
C. $a=14,\ b=26$
D. $a=16,\ b=28$
E. $a=18,\ b=30$

6a108. The sequence $x_0=4$ and $x_{n+1}=\sqrt{x_n+2}$ is given. Find the limit of this sequence.

A. –1
B. 0
C. 1
D. 2
E. 3

6a109. Calculate the integral $I=\int\limits_1^{22}(x-[x])^2dx$.

Here $[x]$ is an integer part of number x, meaning the greatest whole number not exceeding x.

A. 6
B. 7
C. 8
D. 9
E. 3.5

6a110. Calculate a and b for which

$$\lim_{x\to\infty}\left(\sqrt{9x^2+ax}-bx\right)=1.$$

A. 6,3
B. 5,4
C. 4,6
D. 3,7
E. 8,8

6a111. What values may the rank of a matrix with 3 rows and 4 columns have?

A. 3
B. 4
C. 1,2,3,4
D. 0,1,2,3,4
E. 0,1,2,3

6a112. How many real roots does the equation $f'(x)=0$ have, where $f(x)=(x-1)(x-2)^2(x-3)^3$?

A. 2
B. 3
C. 4
D. 5
E. 6

6a113. Let $A=\begin{pmatrix}1&1&0\\0&1&1\\0&0&1\end{pmatrix}$. Calculate $\lim\limits_{x\to\infty} n^{-2}A^n$.

A. $\begin{pmatrix}0{,}1&0{,}3&0.5\\0&0{,}1&0{,}3\\0&0&0{,}1\end{pmatrix}$

B. $\begin{pmatrix}0&0{,}3&0.5\\0&0&0{,}3\\0&0&0\end{pmatrix}$

C. $\begin{pmatrix}0&0&0.5\\0&0&0\\0&0&0\end{pmatrix}$

D. $\begin{pmatrix}0&0&0.5\\0&0&0\\1&0&0\end{pmatrix}$

E. $\begin{pmatrix}0&0&0.5\\0{,}4&0&0\\0&0{,}4&0\end{pmatrix}$

6a114. For what values of a and b the function

$$f(x)=\begin{cases}ax^3+8, & x>1\\ 3x+b, & x\le 1\end{cases}$$

is continuously differentiable on a real axis?

A. $a=0,\ b=5$
B. $a=1,\ b=6$
C. $a=2,\ b=7$
D. $a=3,\ b=8$
E. $a=4,\ b=9$

6a115. For the given game model, for what values of p and q,(i_0,j_0)=(2,2) will be the best strategy?

$$\begin{bmatrix}4&6&7\\12&11&q\\6&p&8\end{bmatrix}$$

A. $p\ge 11$ *and* $q\le 11$
B. $p\le 11$ *and* $q\ge 11$
C. $p\le 11$ *and* $q\le 11$
D. $p=11$ *and* $q<11$
E. All the answers are wrong

6a116. For the given game model, for what values of n and m,(i_0,j_0)=(2,2) will be the best strategy?

$$\begin{bmatrix}0&m&5\\n&4&9\\5&1&2\end{bmatrix}$$

A. $n\le 4$ *and* $m\ge 4$
B. $n\le 4$ *and* $m\le 4$
C. $n\ge 4$ *and* $m\le 4$
D. $n\ne 4$ *and* $m\le 4$
E. All the answers are wrong

6a117. For the given game model what is the payoff of game?

$$\begin{bmatrix}2&5&4\\10&8&7\\4&6&1\end{bmatrix}$$

A. v=7
B. v=5
C. v=6
D. v=8
E. v=4

6a118. For the given game model what is the payoff of game?

$$\begin{bmatrix}1&4&6\\7&5&10\\6&2&3\end{bmatrix}$$

A. v=7
B. v=5
C. v=6
D. v=8
E. v=4

6a119. For the given game model what is the best strategy?

$$\begin{bmatrix}2&5&4\\10&8&7\\4&6&1\end{bmatrix}$$

A. (i_0,j_0)=(2,3)
B. (i_0,j_0)=(1,3)

C. $(i_0,j_0)=(1,1)$
D. $(i_0,j_0)=(2,1)$
E. $(i_0,j_0)=(3,2)$

6a120. In linear programming maximization problem, insertion of additional constraints cannot:
A. *Increase the optimal value of efficiency function*
B. *Decrease the optimal value of efficiency function*
C. *leave the same*
D. *B and C are correct*
E. *None of the above*

6a121. In linear programming minimization problem, insertion of additional constraints cannot:
A. *Increase the optimal value of objective function*
B. *Decrease the optimal value of objective function*
C. *leave the same*
D. *B and C are correct*
E. *None of the above*

6a122. Basic solutions of linear programming dual problem include components in the following numbers (n and m are the numbers of variables and constraints of the primal problem respectively).
A. *m*
B. *n*
C. *n-m*
D. *m-n*
E. *None of the above*

6a123. Such matrix can be chosen as a basic for solving linear programming problems, the rank of which
(n is the number of variables, m - constraints).
A. *= m*
B. *= n*
C. *= m + n*
D. *= m - n*
E. *None of the above*

6a124. By application of simplex method of solving linear programming problems, solutions of problems can be obtained (n is the number of variables, m - constraints)
A. *After iterations, not more than* C_m^n
B. *After iterations, not less than* C_m^n
C. *After iterations, equal number to* C_m^n
D. *B and C are correct*
E. *A and C are correct*

6a125. If i-th component of the optimal solution of linear programming canonical problem is equal to zero ($x_i=0$), the corresponding constraint of dual problem is:
A. > 0
B. < 0
C. $= 0$
D. *B and C are correct*
E. *A and C are correct*

6a126. If i-th component of the optimal solution of linear programming canonical problem is not equal to zero ($x_i \neq 0$), the corresponding constraint of dual problem is:
A. > 0
B. < 0
C. $= 0$
D. *B and C are correct*
E. *A and C are correct*

6a127. If j-th component of the optimal solution of linear canonical programming dual problem is equal to zero ($y_j=0$), the corresponding constraint of primal problem is:
A. > 0
B. < 0
C. $= 0$
A. *B and C are correct*
B. *A and C are correct*

6a128. If j-th component of the optimal solution of linear canonical programming dual problem is not equal to zero ($y_j \neq 0$), the corresponding constraint of direct problem is:
A. > 0
B. < 0
C. $= 0$
D. *B and C are correct*
E. *A and C are correct*

6a129. In linear programming problems, simplex differences corresponding to basic variables
A. > 0
B. < 0
C. $= 0$
D. *B and C are correct*
E. *A and C are correct*

6a130. The optimal values of the auxiliary variables, inserted in linear programming problem, can:

A. *All take zero values*
B. *All take positive values*
C. *All take negative values*
D. *B and C are correct*
E. *A and C are correct*

6a131. What is the next iteration implementation condition of solving linear programming problems by a tabular simplex method?

A. *In pivot column presence of negative element*
B. *In simplex differences line, presence of negative element*
C. *In pivot row presence of negative element*
D. *In pivot row presence of positive element*
E. *In pivot column presence of positive element*

6a132. What is the stop condition of solving linear programming problems by a tabular simplex method?

A. *In pivot column presence of negative element*
B. *In simplex differences line, absence of negative element*
C. *In pivot row presence of negative element*
D. *In pivot row presence of positive element*
E. *In pivot column presence of positive element*

6a133. For optimal solution of linear programming problems, what condition occurs (n-number of variables of primal problem, m-constraints)?

A. $y_i^{dual} = -(st)_{n+i}^{primal}$
B. $y_i^{dual} = -(st)_{m+i}^{primal}$
C. $y_i^{dual} = (st)_{n+i}^{primal}$
D. $y_i^{dual} = (st)_{m+n}^{primal}$
E. $y_i^{dual} = (st)_{m-n}^{primal}$

6a134. For optimal solution of linear programming problems, what condition occurs (n-number of variables of primal problem, m-constraints)?

A. $x_i^{primal} = (st)_{n+i}^{dual}$
B. $x_i^{primal} = (st)_{m+i}^{dual}$
C. $x_i^{primal} = -(st)_{m+i}^{dual}$
D. $x_i^{primal} = -(st)_{m+n}^{dual}$
E. *None of the above*

6a135. The number of positive components of allowable basic solution of linear programming problems can be:

A. *Larger than the number of constraints*
B. *Smaller than the number of constraints*
C. *Equal to the number of constraints*
D. *B and C are correct*
E. *A and C are correct*

6a136. Addition of the same value to all elements of two-person, zero-sum game model matrix:

A. *Changes the game payoff*
B. *Changes optimal mixed strategies*
C. *Does not change the game payoff*
D. *B and C are correct*
E. *None of the above*

6a137. Zero-sum 2xn (n>2) game has no pure strategies. Then mixed strategies contain:

A. *Not more than 2 pure strategies*
B. *Not less than n pure strategies*
C. *n pure strategies*
D. *n+2 pure strategies*
E. *None of the above*

6a138. What equals the payoff of symmetric game?

A. *max(h_{ij})*
B. *min(h_{ij})*
C. *0*
D. *h_{ij}*
E. *None of the above*

6a139. Which statement is correct?

A. *Objective functions of primal and dual problems have the same value*
B. *Primal and dual problems have the same number of variables*
C. *Primal and dual problems have the same number of constraints*
D. *All*
E. *None of the above*

6a140. For what values of λ_1, λ_2 parameters, the following problem has infinite set of solutions?

$$f(X) = \lambda_1 x_1 + \lambda_2 x_2 \to \min_{X \in D},$$

$$D: \begin{cases} x_1 + 2x_2 \ge 2, \\ x_1 - 4x_2 \le 2, \\ 6x_1 + 5x_2 \le 30, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. $\lambda_1 = 2, \lambda_2 = 4$
B. $\lambda_1 = 2, \lambda_2 = 2$
C. $\lambda_1 = 1, \lambda_2 = 4$
D. $\lambda_1 = 2, \lambda_2 = 3$
E. $\lambda_1 = 4, \lambda_2 = 2$

6a141. For what values of λ_1, λ_2 parameters, the following problem has one solution?

$$f(X) = \lambda_1 x_1 + \lambda_2 x_2 \to \min_{X \in D},$$

$$D: \begin{cases} x_1 + 2x_2 \le 5, \\ x_1 + x_2 \le 4, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. $\lambda_1 = 2, \lambda_2 = 2$
B. $\lambda_1 = 1, \lambda_2 = 2$
C. $\lambda_1 = 1, \lambda_2 = 4$
D. $\lambda_1 = 2, \lambda_2 = 4$
E. $\lambda_1 = 4, \lambda_2 = 4$

6a142. For what values of λ_1, λ_2 parameters, the following problem has one solution?

$$f(X) = \lambda_1 x_1 + \lambda_2 x_2 \to \min_{X \in D},$$

$$D: \begin{cases} x_1 + 2x_2 \ge 2, \\ x_1 - 4x_2 \le 2, \\ 6x_1 + 5x_2 \le 30, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. $\lambda_1 = 2, \lambda_2 = 4$
B. $\lambda_1 = 1/2, \lambda_2 = 1$
C. $\lambda_1 = 1, \lambda_2 = 4$
D. $\lambda_1 = 3, \lambda_2 = 6$
E. $\lambda_1 = 1/3, \lambda_2 = 2/3$

6a143. For what values of λ parameters, the following problem has no solution?

$$f(X) = x_1 + x_2 + x_3 \to \max_{X \in D},$$

$$D: \begin{cases} x_1 + x_3 = 2, \\ x_1 + 2\lambda x_2 + x_3 = 0, \\ x_1 \ge 0, x_2 \ge 0, x_3 \ge 0: \end{cases}$$

A. *0*
B. *5*
C. *3*
D. *2*
E. *1*

6a144. The following linear programming problem has:

$$f(X) = 2x_1 + 3x_2 \to \max_{X \in D}$$

$$D: \begin{cases} 7x_1 + 6x_2 \le 42 \\ -x_1 + 5x_2 \le 15 \\ x_1 \ge 0,\ x_2 \ge 0: \end{cases}$$

A. One solution
B. An infinite set of solutions
C. Does not have a solution
D. Unlimited solutions
E. None of the above

6a145. The following linear programming problem has:

$$f(X) = 2x_1 + 4x_2 \to \max_{X \in D},$$

$$D: \begin{cases} x_1 + 2x_2 \le 5, \\ x_1 + x_2 \le 4, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. One solution
B. An infinite set of solutions
C. Unlimited solutions
D. Does not have a solution
E. None of the above

6a146. The following linear programming problem has:

$$f(X) = 2x_1 + x_2 \to \min_{X \in D},$$

$$D: \begin{cases} x_1 - x_2 \le 10, \\ 2x_1 \le 40, \\ x_1 \ge 0, x_2 \ge 0: \end{cases}$$

A. One solution
B. An infinite set of solutions
C. Unlimited solutions
D. Does not have a solution
E. None of the above

6a147. Which are mixed strategies of the following game?

$$H = \begin{bmatrix} 2 & 3 \\ 6 & 1 \end{bmatrix}$$

A. $X = \left(\frac{1}{6}, \frac{5}{6}\right), Y = \left(\frac{1}{3}, \frac{2}{3}\right), v = \frac{8}{3}$

B. $X = \left(\frac{5}{6}, \frac{1}{6}\right), Y = \left(\frac{1}{3}, \frac{2}{3}\right), v = \frac{8}{3}$

C. $X = \left(\frac{5}{6}, \frac{1}{6}\right), Y = \left(\frac{1}{3}, \frac{1}{3}\right), v = \frac{8}{3}$

D. $X = \left(\frac{3}{6}, \frac{1}{6}\right), Y = \left(\frac{2}{3}, \frac{1}{3}\right), v = \frac{8}{3}$

E. $X = \left(\frac{2}{6}, \frac{2}{6}\right), Y = \left(\frac{2}{3}, \frac{1}{3}\right), v = \frac{8}{3}$

6a148. Which are mixed strategies of the following game?

$$H = \begin{bmatrix} 5 & 3 \\ 1 & 4 \end{bmatrix}$$

A. $X = \left(\frac{3}{5}, \frac{2}{5}\right), Y = \left(\frac{1}{5}, \frac{4}{5}\right), v = \frac{17}{5}$

B. $X = \left(\frac{3}{5}, \frac{2}{5}\right), Y = \left(\frac{1}{5}, \frac{3}{5}\right), v = \frac{17}{5}$

C. $X = \left(\frac{4}{5}, \frac{1}{5}\right), Y = \left(\frac{1}{5}, \frac{3}{5}\right), v = \frac{17}{5}$

D. $X = \left(\frac{4}{5}, \frac{2}{5}\right), Y = \left(\frac{1}{5}, \frac{2}{5}\right), v = \frac{17}{5}$

E. $X = \left(\frac{1}{5}, \frac{1}{5}\right), Y = \left(\frac{4}{5}, \frac{1}{5}\right), v = \frac{17}{5}$

6a149. Let $f(x) = x^2 - 3x + 1$. Calculate $\sum_{n=0}^{\infty} \frac{f(n)}{n!}$

A. -e
B. e
C. 1
D. 0
E. 2e

6a150. Calculat $\lim_{n\to\infty}\left(\frac{1}{n^3} + \frac{2^2}{n^3} + \frac{3^2}{n^3} + \cdots + \frac{(n-1)^2}{n^3}\right)$

A. 1
B. 1/2
C. 1/3
D. 1/4
E. 1/5

6a151. Let $f(x) = 4[x] - 2[2x] + 1$ (here $[x]$ is a integer part of the number x –the greatest whole number not exceed the number x).

Calculate $I = \int_0^{15} \left(f(1000x) + f^2(1000x) \right) dx$

A. 20
B. 0
C. 1
D. 10
E. 15

b) Problems

6b1.

The following matrix game is given:

$$H = \begin{bmatrix} 3 & -2 & 4 \\ -1 & 4 & 2 \\ 2 & 2 & 6 \end{bmatrix}$$

Find the worth of game, optimal strategies and characterize the game. If necessary, construct corresponding problems of mathematical programming.

6b2.

Define the first two members of Taylor series $\Phi(t, t_0)$ if

$$A(t) = \begin{bmatrix} t & t^2 & t^3 \\ 1 & t & (2-1) \\ t^2 & t & 1 \end{bmatrix}, t_0 = 2$$

6b3.

Define Φ(t) if

$$A = \begin{bmatrix} 2 & 1 & 0 \\ 0 & 3 & 0 \\ 2 & 1 & 1 \end{bmatrix}.$$

6b4.
Reduce the system to diagonal form if

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 0 & 1 & 0 \\ 2 & 1 & 3 \end{bmatrix}$$

6b5.
The following matrix is given:

$$A = \begin{bmatrix} 1 & -2 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

What is the constant term of characteristic polynomial equal to?

6b6.
The following matrix is given:

$$A = \begin{bmatrix} 1 & -2 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

What is $||A||_2$ norm equal to?

6b7.
What is the coefficient of A_{3X3} matrix's characteristic polynomial term containing λ^2, if $\lambda_1 = 1, \lambda_2 = 2, \lambda_3 = 3$ are the eigenvalues of A_{3X3}.

6b8.
What equals A_{4X4} matrix's characteristic polynomial coefficient of the term which contains λ^2, if $\lambda_1 = 0, \lambda_2 = 1, \lambda_3 = 2, \lambda_4 = 3$ are the eigenvalues of A_{4X4}?

6b9.
The table of *log x* function in [0,1000] interval is built by the help of linear interpolation. What *h* step should be selected for the error not to exceed 0.001? Consider cases of constant and variable steps (by dividing the interval into several subintervals). Estimate the minimum number of nodes which is necessary to provide the given accuracy.

6b10.
Using generalized trapezoid rule, calculate

$$\int_0^1 \frac{e^x}{x^2 + b^2} dx$$

integral with $O(h^2)$ accuracy (h is division step). How should this formula be applied to provide the same accuracy if $b \ll 1$?

6b11.
Apply quadrature formula for the calculation of the integral

$$\int_0^1 \frac{f(x)}{\sqrt{x}} dx$$

with 10^{-4} accuracy, providing $|f''(x)| \leq 1$.

6b12.
Define the initial approximation domains of x_0 for which $x_{n+1} = \dfrac{x_n^3 + 1}{20}$ iterations converge.

6b13.

$f(x)=\dfrac{5}{1+100x^2}$ function is replaced by $y=\alpha x+\beta$ linear function in segment $[-10,10]$. Define coefficients α and β to provide the smallest error. Can such α and β uniquely be found? If yes, find it; if no – consider possible cases.

6b14.

Construct an approximate formula (multiple-application rectangle rule) for the calculation of the integral $\int_1^\infty \dfrac{f(x)dx}{1+x^2}$ with $\varepsilon=0{,}01$ accuracy. The function f on interval $[1,\infty)$ is continuously differentiable and bounded.

6b15.

Continuously differentiable function f is given on $[a,b]$ segment and $a<x_1<x_2<b$. Find the polynomial P_3 of the third order so that in x_1 and x_2 points its and its derivative's values coincide with $f(x_1)$, $f(x_2)$ and $f'(x_1)$, $f'(x_2)$ values respectively. Is it possible to generalize the obtained formula for arbitrary number of points $a<x_1<\ldots<x_2<b$?

6b16.

Find the roots of the equation $x^4-10x+1=0$ with $\varepsilon=0{,}01$ accuracy. Choose the fastest algorithm.

6b17.

Assume $f(x)=\dfrac{1}{1+x}+\dfrac{1}{3-x}$. Find $g(x)=ax^2+bx+c$ quadratic function, which gives the best approximation for the function f in $[0,2]$ interval. Consider different cases.

6b18.

Assume

$$\Delta_n = det\begin{pmatrix} 2 & 1 & 0 & 0 & \cdots & 0 \\ 1 & 2 & 1 & 0 & \cdots & 0 \\ 0 & 1 & 2 & 1 & \cdots & 0 \\ 0 & 0 & 1 & 2 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 2 \end{pmatrix}$$

.Calculate the limit $\lim\limits_{n\to\infty}\dfrac{\Delta_n}{n}$.

6b19.

The triangle ABC is given by the three vertices $A(x_1,y_1)$, $B(x_2,y_2)$, $C(x_3,y_3)$. How to check if the given point D with coordinates $D(x_0,y_0)$ lies in interior of that triangle? Describe the algorithm. Is it possible to generalize this algorithm for the case of

a) convex polygon

b) arbitrary polygon?

6b20.

x_j, $j=1,2$, and y_k, $k=0,\ldots,4$ real numbers are given. Find the forth degree polynomial P_4 in a way that $P_4^{(k)}(x_1)=y_k$, $k=0,1,2,3$; $P_4(x_2)=y_4$. Generalize the result: find the n-th degree polynomial P_n so that $P_n^{(k)}(x_1)=y_k$, $k=0,\ldots,m$; $P_n^{(j)}(x_2)=y_{m+1+j}$, $j=0,\ldots,n-m-1$.

6b21.

The following matrix is given: $A=\begin{bmatrix}1 & -3 & 0\\ 0 & 1 & 2\\ -1 & 0 & 1\end{bmatrix}$ What does the free term of characteristic polynomial equal?

6b22.

Given $A=\begin{bmatrix}1 & -3 & 0\\ 0 & 1 & 2\\ -1 & 0 & 1\end{bmatrix}$ matrix. What does $||A||_2$ norm equal?

6b23.

What does A_{3X3} matrix's characteristic polynomial coefficient of the term which contains λ equal if

$$\lambda_1=1,\lambda_2=4,\lambda_3=2.$$

6b24.

What does A_{4X4} matrix's characteristic polynomial coefficient of the term which contains λ^2 equal if

$$\lambda_1=4,\lambda_2=1,\lambda_3=2,\lambda_4=3.$$

6b25.

Find the n degree polynomial P_n which meets the following conditions:

$$P_n^{(j)}(1)=y_j,\quad j=0,1,2,\qquad P_n^{(k)}(0)=z_k,\quad k=0,1.$$

Find the smallest n for which the problem has a solution for arbitrary values y_j and z_k. For this n find the polynomial P_n in explicit form.

6b26.

On the segment $[-1,1]$ find the best uniform approximation polynomial of order one P_1 for $f(x)=x^3$ function, i.e. find P_1 polynomial for which the uniform norm $\|f-P_1\|=\max_{x\in[-1,1]}|f(x)-P_1(x)|$ is minimal.

6b27.

Find the eigenvalues of the matrix A which satisfies the condition $A^2=0$ (0 is zero matrix). What may be said about the eigenvalues of the matrix A which satisfies the condition $A^n=0$ where n is a natural number. Justify the answer.

6b28.

Calculate $ln\,2$ with 0.001 accuracy, using $ln(1+x)=\sum_{k=1}^{\infty}(-1)^{k+1}\frac{x^k}{k}$ series for $|x|<1$. Find more optimal solution, i.e. a method of solution which requires the smallest number of summands of series.

6b29.

The following matrix is given $A=\begin{bmatrix}2 & -6 & 0\\ 0 & 2 & 4\\ -2 & 0 & 2\end{bmatrix}$. What does the free term of characteristic polynomial equal?

6b30.

What does A_{4x4} matrix's characteristic polynomial coefficient of the term which contains λ^2 equal if

$$\lambda_1 = 2, \lambda_2 = 0.5, \lambda_3 = 1, \lambda_4 = 1.5:$$

6b31.

Given the matrix of state variables of controlling system.

$$A = \begin{bmatrix} -2 & 0 \\ 1 & -1 \end{bmatrix}$$

Define $\Phi(t)$ fundamental matrix of replacement.

6b32.

Find out full controllability of the system described by the following equations.

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 0.5 & 0 & 1 \\ 0.5 & 0.5 & 0 \\ 0 & 0.5 & 0.5 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} + \begin{bmatrix} 0 & 0.5 \\ 0.5 & 0 \\ 0.5 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix},$$

6b33.

Estimate an accuracy of the rectangle's symmetric rule

$$I = \int_a^b f(x)dx \approx f\left(\frac{a+b}{2}\right)(b-a) = \tilde{I},$$

supposing that the function f two times continuously differentiable on the segment $[a,b]$.

6b34.

Applying the rectangle's symmetric rule

$$\int_a^b f(x)dx \approx f\left(\frac{a+b}{2}\right)(b-a) = \tilde{I}_1,$$

and the trapezoidal rule

$$\int_a^b f(x)dx \approx \frac{f(a)+f(b)}{2}(b-a) = \tilde{I}_2,$$

to the integral $I = \int_{\ln a}^{\ln b} e^x dx$, where $0 < a < b$, prove an inequalities

$$\sqrt{ab} < \frac{b-a}{\ln b - \ln a} < \frac{a+b}{2}$$

(geometrical mean is less than logarithmical mean, which is less than arithmetical mean).

6b35.

A generalized Rolle's theorem. Suppose the function f is continuous on $[a,b]$ and $n+1$ times continuously differentiable on (a,b). Let $x_0 \in (a,b)$ be a point at which $f(x_0) = f'(x_0) = \ldots = f^{(n)}(x_0) = 0$. Then for arbitrary point $x \in (a,b)$, $x \neq x_0$ at which $f(x) = 0$ there is a point $\eta \in (x, x_0)$, such that $f^{(n+1)}(\eta) = 0$.

6b36.

Define the sequence of positive numbers: $x_0 > 0$, $\quad x_{n+1} = \dfrac{1}{1+x_n}$ for $n \geq 0$.

Prove that this sequence is converges and find the limit.

6b37.

Calculate the integral $I = \int_0^{0.5} \frac{\sin x}{x} dx$ with accuracy 0,001. That is, find number I^* such that $\left|I - I^*\right| < 0{,}001$.

6b38.

The following matrix is given:

$$A = \begin{bmatrix} 2 & -6 & 0 \\ 0 & 2 & 4 \\ -2 & 0 & 2 \end{bmatrix}$$

What does the free term of characteristic polynomial equal?

6b39.

What does A_{4x4} matrix's characteristic polynomial coefficient of the term which contains λ^2 equal if $\lambda_1 = 2, \lambda_2 = 0.5, \lambda_3 = 1, \lambda_4 = 3.$

6b40.

Given the matrix of state variables of controlling system.

$$A = \begin{bmatrix} -1 & 0 \\ 2 & -2 \end{bmatrix}$$

Define $\Phi(t)$ fundamental matrix of replacement.

6b41.

Find out full controllability of the system described by the following equations.

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 1 & 0 & 2 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} + \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 2 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix}$$

6b42.

Given the matrix of state variables of controlling system.

$$A = \begin{bmatrix} -1 & 0 \\ 1 & -3 \end{bmatrix}$$

Define Φ(t) fundamental matrix of replacement

6b43.

Find full controllability of system, described by the following motion equation.

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 0 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix}:$$

6b44.

Find full observability of system, described by the following motion equation.

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 1 & 2 & 0 \\ 2 & 0 & 1 \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} + \begin{bmatrix} 1 & 1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix},$$

$$\begin{pmatrix} Y_1(t) \\ Y_2(t) \end{pmatrix} = \begin{bmatrix} 1 & 2 & 0 \\ 3 & 2 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix}:$$

6b45.

What is the view of $U_{1opt}(t)$ and $U_{2opt}(t)$ if

$$I = \int_0^T \left(u_1^2(t) + u_2^2(t)\right) dt \to \min_{u_1(t), u_2(t)},$$

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{pmatrix} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix}:$$

6b46.
What does the sum of cubes of the roots of

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 1 & 2 & 3 \\ 1 & 0 & 2 \end{bmatrix}$$

matrix's $det[A - \lambda E] = \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$ characteristic equation equal to?

6b47.
What does $\psi^T(t) \cdot \psi(t)_{|t=2}$ equal if it is known that

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 2 \\ 1 & -2 & 0 \end{bmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} \begin{matrix} , x_1(0) = -1 \, , \\ , x_2(0) = 2 \, , \\ , x_3(0) = 1 \, , \end{matrix}$$

and $\psi(t) = (\psi_1(t),\ \psi_2(t),\ \psi_3(t))^T$ is conjugate variable vector.

6b48.
Find the general forms of $U_{1_{opt}}(t)$ and $U_{2_{opt}}(t)$ if

$$I = \int_0^T (U_1^2(t) + U_2^2(t))dt \xrightarrow[U_1(t),U_2(t)]{} min,$$

$$\begin{pmatrix} \dot{X}_1(t) \\ \dot{X}_2(t) \end{pmatrix} = \begin{bmatrix} 1 & 2 \\ 2 & 0 \end{bmatrix} \cdot \begin{pmatrix} X_1(t) \\ X_2(t) \end{pmatrix} + \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} U(t) \\ U_2(t) \end{pmatrix}:$$

6b49.
What does the sum of cubes of the roots of

$$A = \begin{bmatrix} 2 & 0 & 1 \\ 2 & 2 & 1 \\ 1 & 0 & 4 \end{bmatrix}$$

matrix's $det[A - \lambda E] = \lambda^3 + P_1 \cdot \lambda^2 + P_2 \cdot \lambda + P_3 = 0$ characteristic equation equal to?

6b50.
Find out full controllability of the system described by the following equations.

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_1(t) \\ \dot{x}_1(t) \end{pmatrix} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \cdot \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} + \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} u_1(t) \\ u_2(t) \end{pmatrix}:$$

6b51.
What does $\psi^T(t) \cdot \psi(t)_{|_{t=2}}$, equal if it is known that

$$\begin{pmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{pmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 2 \\ 1 & -2 & 0 \end{bmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{pmatrix} \begin{matrix} , x_1(0) = 1 \, , \\ , x_2(0) = 0 \, , \\ , x_3(0) = 1 \, , \end{matrix}$$

and $\psi(t) = (\psi_1(t),\ \psi_2(t),\ \psi_3(t))^T$ is conjugate variable vector.

6b52.
Find all differentiable functions that satisfy the following functional equation:

$$f(x+y) = \frac{f(x) + f(y)}{1 - f(x)f(y)}.$$

6b53.

Let $[x]$ be the integer part of the number x (the greatest integer number not more than the real number x (floor function)). Prove that for an arbitrary number x and natural number n the following equality takes place:

$$[x]+\left[x+\frac{1}{n}\right]+\left[x+\frac{2}{n}\right]+\cdots+\left[x+\frac{n-1}{n}\right]=[nx].$$

6b54.

Using the notation $[x]$ (the greatest integer number not more than the real number x (floor function)), define the quantity of points with integer coordinates in the domain $D=\{(x,y): a\le x\le b,\ 0\le y\le f(x)\}$ (a and b are integer numbers). Then, using the obtained function, calculate:

$$S=\left[\frac{q}{p}\right]+\left[\frac{2q}{p}\right]+\left[\frac{3q}{p}\right]+\cdots+\left[\frac{(p-1)q}{p}\right],$$

where p and q are relatively prime integers (numbers, that don't have common divisors other than 1).

6b55.

Let $f(x)=(r_1-x)(r_2-x)\ldots(r_n-x)$. Calculate the determinant Δ using this function:

$$\Delta=\begin{vmatrix} r_1 & a & a & a & \cdots & a \\ b & r_2 & a & a & \cdots & a \\ b & b & r_3 & a & \cdots & a \\ b & b & b & r_4 & \cdots & a \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ b & b & b & b & \cdots & r_n \end{vmatrix}.$$

6b56.

Let $\alpha>0$. Calculate the limit $A=\lim\limits_{n\to\infty}\dfrac{1^{\alpha-1}+2^{\alpha-1}+3^{\alpha-1}+\cdots+n^{\alpha-1}}{n^{\alpha}}$

6b57.

Find all differentiable functions satisfying the following functional equation:

$$f\left(\frac{x+y}{2}\right)=\frac{f(x)+f(y)}{2}.$$

6b58.

Let A,B,C be n order square matrices such that $\det A\ne 0$. Prove that

$$\det\begin{pmatrix} A & B \\ A^{-1} & C \end{pmatrix}=\det\left(AC-A^{-1}B\right).$$

6b59.

Define a function satisfying the equality $f'(x)f''(x)=0$.

6b60.

Define a continuous function f which satisfies the following integral equation:

$$f(x)-9\int_0^x (x-t)f(t)dt=3x.$$

6b61.

Define function f with a condition $f(0)=8$, satisfying the following functional equation:

$$f(4x)-f(x)=x.$$

6b62.

Two equally-skilled players play a game. There is only one winner in every round of this game with the probability 0.5. Each of the players stakes A$. The first player to win 10 rounds wins the whole stake – 2A$. For some reason the game stopped when the first player had won 8 rounds and the second one – 7 rounds. How to divide the bet fairly?

6b63.
Calculate the limit

$$\lim_{n\to\infty}\frac{n}{a^n}\sum_{k=1}^{n}\frac{a^k}{k}\text{, when } a>1$$

6b64.
Let x be an arbitrary real number.

$$\cos x \equiv \cos_1 x,\ \cos(\cos x)=\cos_2 x,\dots,\ \cos(\cos_n x)=\cos_{n+1} x$$

Does this sequence have a limit and if it does, then what is it?

6b65.
Find differentiable function f such that

$$f(x)+f(y)=f\left(\frac{x+y}{1-xy}\right),\quad xy\neq 1:$$

7. DISCRETE MATHEMATICS AND THEORY OF COMBINATIONS

a) Test questions

7a1. The set is countable if it is

A. Finite
B. Equivalent to some subset of finite set
C. Equivalent to any subset of natural number set
D. Equivalent to any infinite set
E. Equivalent to any infinite subset of natural number set

7a2. The graph includes Euler cycle if and only if

A. It is connected and the degrees of all nodes are even
B. It is connected and the degrees of some nodes are odd
C. The degrees of all nodes are even
D. It is not connected and the degrees of some nodes are even
E. It is connected and the degrees of all nodes are odd

7a3. If for $f(x_1,\dots,x_i,\dots,x_n)$ Boolean function $\omega_i^f=1$ (i=1,2,…,n), it is

A. Constant 1 function
B. Linear function
C. Self-dual function
D. Monotone function
E. Constant 0 function

7a4. If Boolean function is monotonous, then

A. Its short disjunctive normal form does not contain negation of variables
B. It is not self-dual
C. Its short disjunctive normal form does not coincide with its minimal disjunctive normal form
D. it is also a threshold
E. it is not a threshold

7a6. In the given design styles in what sequence does the performance increase in case of other same parameters a) library; b) gate matrix; c) full custom; d) programmable matrix;

A. d - b - a - c
B. a - b - c - d
C. b - d - a - d
D. c - a - b - d
E. d - c - b - a

7a7. Which of the presented description forms of an electrical circuit is more convenient for the realization of sequential placing algorithm?

A. Graph of commutation scheme
B. Complex list
C. Adjacency matrix
D. A and B equally
E. B and C equally

7a8. In case of the presented design styles, in what order does the density of cells' placing increase? a) standard IC design; b) library design; c) gate matrix design; d) full custom design; e) programmable matrix design.

A. b - a - c - e - d
B. a - b - c - d - e
C. d - c - b - e - a
D. a - d - b - c - e
E. d - b - c - e - a

7a9. The activity of x_3 argument of $(x_1 \vee x_2) \oplus (x_3 \vee x_4 x_5))$ function equals

A. 1/4
B. 1/8
C. 3/8
D. 5/8
E. 3/4

7a10. If for $f(x_1, \dots, x_n)$ Boolean function $\omega_{1,2,\dots,n}^f=1$, then f is

A. Constant 0 function
B. Constant 1 function
C. Monotone function
D. Self-dual function
E. Linear function

7a11. The activity of $x_1(\bar{x}_2 \vee x_3(x_4 \vee x_5 \bar{x}_6))$ function's x_1 argument equals

A. 25/32
B. 27/32
C. 21/32
D. 13/16
E. 19/32

7a12. $x_1(\bar{x}_2 \vee x_3(x_4 \vee x_5 \bar{x}_6))$ function's norm equals

A. 11/64
B. 13/32
D. 17/64
D. 21/64
E. 23/64

7a13. $(x_1 \vee x_2) \oplus (x_3 \vee x_4 x_5))$ function's norm equals

A. 7/16
B. 9/16
C. 13/16
D. 11/16
E. 5/16

7a14. $f(x_1, \dots, x_n)$ is dual if

A. $\exists(\alpha_1,\dots,\alpha_n)$

$$\bar{f}(\bar{\alpha}_1,\dots,\bar{\alpha}_n) = f(\alpha_1,\dots,\alpha_n)$$

B. $\forall(\alpha_1,\dots,\alpha_n)$

$$\bar f(\bar\alpha_1,\dots,\bar\alpha_n)=f(\alpha_1,\dots,\alpha_n)$$

C. $\exists(\alpha_1,\dots,\alpha_n)$

$$\bar f(\bar\alpha_1,\dots,\bar\alpha_n)=\overline{f}(\alpha_1,\dots,\alpha_n)$$

D. $\exists(\alpha_1,\dots,\alpha_n)$

$$f(\bar\alpha_1,\dots,\bar\alpha_n)=f(\alpha_1,\dots,\alpha_n)$$

E. $\forall(\alpha_1,\dots,\alpha_n)$

$$f(\bar\alpha_1,\dots,\bar\alpha_n)=f(\alpha_1,\dots,\alpha_n)$$

7a15. The activity of the combination of arguments X_3 and X_4 for the function $(x_1 x_2)\oplus(x_3 \vee x_4)x_5$ equals:

A. 1/4
B. 7/16
C. 3/4
D. 11/16
E. 1/8

7a16. If $f(x_1,\dots,x_n)$ is threshold function

A. $\bar f(x_1,\dots,x_n)$ *is not threshold function*

B. $f(\bar x_1,\dots,\bar x_n)$ *is not threshold function*

C. $\bar f(\bar x_1,\dots,\bar x_n)$ *is threshold function*

D. $x\oplus f(x_1,\dots,x_n)$ *is threshold function*

E. $x\oplus \bar f(x_1,\dots,x_n)$ *is threshold function*

7a17. Binary relation is the equivalence relation if it is

A. Transitive, symmetric but not reflexive
B. Not symmetric, reflexive and transitive
C. Symmetric, reflexive but not transitive
D. Reflexive, transitive and symmetric
E. Not symmetric, not reflexive and transitive

7a18. $(x_3 \vee x_2)\oplus(\bar x_1 \vee x_4 x_5))$ function's norm equals

A. 9/16
B. 11/16
C. 13/16
D. 7/16
E. 5/16

7a19. The activity of $(x_3 \vee x_2)\oplus(x_1 \vee x_4 x_5))$ function's x_3 argument equals

A. 1/4
B. 1/8
C. 3/8
D. 5/8
E. 1/2

7a20. How many connectivity components does the complementation of the graph which has 4-connected component have?

A. 1
B. 2
C. 3
D. 4.
E. The correct answer is missing

7a21. Given an n-input, m-output combinational circuit C, depending on input variables x_1, x_2, …, x_n and output variables y_1, y_2, …, y_m implementing functions $f_i(x_1, x_2, \dots, x_n)$, $1\le i\le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \dots, x_n)$, $1\le j\le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. Set T of input vectors is a test with respect to the set Φ of faults if

A. For any f∈Φ and for any an input vector $(\alpha_1, \alpha_2, \dots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1\le i\le n$, *and for any j,* $1\le j\le m$, $f^*(\alpha_1, \alpha_2, \dots, \alpha_n) \equiv f_j(\alpha_1, \alpha_2, \dots, \alpha_n)$;

B. For any f∈Φ and for any input vector $(\alpha_1, \alpha_2, \dots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1\le i\le n$, *and for any j,* $1\le j\le m$,

$f_j^*(\alpha_1, \alpha_2, \dots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \dots, \alpha_n)$;

C. For any f∈Φ there exists an input vector $(\alpha_1, \alpha_2, \dots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1\le i\le n$, *and there exists a j,* $1\le j\le m$, *such that*

$f_j^*(\alpha_1, \alpha_2, \dots, \alpha_n) \le f_j(\alpha_1, \alpha_2, \dots, \alpha_n)$;

D. For any f∈Φ there exists such an input vector $(\alpha_1, \alpha_2, \dots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1\le i\le n$, *and there exists a j,* $1\le j\le m$, *such that*

$f_j^*(\alpha_1, \alpha_2, \dots, \alpha_n) \ge f_j(\alpha_1, \alpha_2, \dots, \alpha_n)$.

E. For any f∈Φ there exists an input vector $(\alpha_1, \alpha_2, \dots, \alpha_n)$ *such that* $\alpha_i \in \{0, 1\}, 1\le i\le n$, *and there exists a j,* $1\le j\le m$, *such that*

$f_j^*(\alpha_1, \alpha_2, \dots, \alpha_n) \ne f_j(\alpha_1, \alpha_2, \dots, \alpha_n)$;

7a22. Given an n-input, m-output combinational circuit C, depending on input variables x_1, x_2, …, x_n and output variables y_1, y_2, …, y_m implementing functions $f_i(x_1, x_2, \dots, x_n)$, $1\le i\le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \dots, x_n)$, $1\le j\le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. Set $(\beta_1, \beta_2, \dots, \beta_n)$ detects fault F if

A. $\exists j$, $1\le j\le m$, *and*

$f^*(\beta_1, \beta_2, \dots, \beta_n) \ne f_j(\beta_1, \beta_2, \dots, \beta_n)$;

B. for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input patterns, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and for $\forall$ j, $1 \le j \le m$,

$f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \equiv f_j(\beta_1, \beta_2, \ldots, \beta_n)$;

C. for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input patterns, for $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$, $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j(\beta_1, \beta_2, \ldots, \beta_n)$;

D. $\exists$ j, $1 \le j \le m$, so that

$f_j^*(\beta_1, \beta_2, \ldots, \beta_n) \le f_j(\beta_1, \beta_2, \ldots, \beta_n)$;

E. $\exists$ j, $1 \le j \le m$, so that

$f_j^*(\beta_1, \beta_2, \ldots, \beta_n) \ge f_j(\beta_1, \beta_2, \ldots, \beta_n)$.

7a23. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le j \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. F fault cannot be detected with respect to some class faults if

A. $\exists$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ such input pattern, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, and $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

B. 1. F fault cannot be detected or

2. $\exists$ $G \in \Phi$ fault for which $\exists$ line B, for which in case of $\forall$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input pattern, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$, and $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) = f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$, where f_j^{**} is the function obtained from C when a fault G occurs on its line B

C. 1. fault F is detectable;

2.for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input patterns, for $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$, $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

D. 1. fault F is detectable;

2. $\exists$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ such input pattern, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, so that $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

E. 1. fault F is detectable;

2. $\exists$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ such input pattern, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, so that $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j^{**}(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

7a24. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le j \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. F fault is not redundant if

A. for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input patterns, for $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$,

$f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

B. $\exists$ input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ so that $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, for which

$f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

C. $\exists$ such input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, that $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) = f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

D. $\exists$ such input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, so that $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

E. for $\forall$ input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, $\exists$ j, $1 \le j \le m$, so that

$f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

7a25. Given an n-input, m-output combinational circuit C, depending on input variables $x_1, x_2, \ldots, x_n$ and output variables $y_1, y_2, \ldots, y_m$ implementing functions $f_i(x_1, x_2, \ldots, x_n)$, $1 \le i \le m$, and a combinational circuit C* implementing functions $f_j^*(x_1, x_2, \ldots, x_n)$, $1 \le j \le m$, and obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. Set T is not a test with respect to set Φ of faults if

A. $\exists$ $f \in \Phi$ so that for $\forall(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input patterns, for $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$, $f^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

B. for $\forall$ $f \in \Phi$, for $\forall$ input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, for $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$, $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \neq f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

C. for $\forall$ $f \in \Phi$, $\exists$ such input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, so that $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \le f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$;

D. for $\forall$ $f \in \Phi$, $\exists$ such input pattern $(\alpha_1, \alpha_2, \ldots, \alpha_n)$, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\exists$ j, $1 \le j \le m$, so that $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) \ge f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

E. $\exists$ $f \in \Phi$, for which, and for $\forall$ $(\alpha_1, \alpha_2, \ldots, \alpha_n)$ input pattern, $\alpha_i \in \{0, 1\}, 1 \le i \le n$, and $\forall$ j, $1 \le j \le m$, $f_j^*(\alpha_1, \alpha_2, \ldots, \alpha_n) = f_j(\alpha_1, \alpha_2, \ldots, \alpha_n)$.

7a26. In a combinational circuit which has N lines, any number of stuck-at-0 or stuck-at-1 faults can occur. Find all possible multiple (not single) number of faults.
A. 2^N
B. 3^N
C. $3^N - 1$
D. $3^N - 2^N - 1$
E. 2N

7a27. What is a technical object model? B technical object is called A technical object model if through its experiments it is possible to have an idea about A technical object's
A. design
B. properties
C. parameters
D. circuit
E. structure

7a28. In what sequence are the following stages of digital IC design executed? a) layout design, b) behavioral-level design, c) logic design, d) RTL design
A. c-a-b-d
B. d-b-c-a
C. b-d-c-a
D. c-a-d-b
E. a-b-c-d

7a29. In component level of IC design what kind of mathematical method is used?
A. Probability theory
B. Theory of queue system
C. Boolean algebra
D. Differential equations system
E. Partial differential equations system

7a30. In case of the given elemental bases, in what sequence does the consumption power increase if the other parameters are similar? a) bipolar; b) CMOS; c) N-MOS
A. b - c-a
B. a-c-b
C. a-b-c
D. b-a-c
E. c-b-a

7a31. Which of the given answers more contributes to the increase of performance in digital circuits?
A. Decrease of load capacitance
B. Increase of load capacitance
C. Decrease of technological sizes
D. Decrease of supply voltage
E. A. and C. together

7a32. Which of the given answers more characterizes the advantage of a MOS elemental base in comparison to bipolar?
A. Little consumption power
B. High performance
C. Simplicity of technology
D. A and C together
E. A and B together

7a33. A password must contain 2 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 4 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?
A. 1 000 000
B. 2 000 000
C. 5 000 000
D. 8 000 000
E. 10 000 000

7a34. A password must contain 2 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 2 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?
A. 100 000
B. 400 000
C. 600 000
D. 800 000
E. 1 000 000

7a35. A password must contain 2 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 3 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?
A. 600 000
B. 800 000
C. 1 000 000
D. 1 200 000
E. 1 800 000

7a36. A password must contain 3 numerals from the list {0, 1, 2, 3, 4, 5, 6, 7, 8, 9} and 3 letters from the list {a, A, b, B, c, C, d, D, e, E}. The first symbol must be a letter. Symbols may be repetitive. How many passwords can be generated meeting those conditions?
A. 100 000
B. 1 000 000
C. 10 000 000
D. 100 000 000
E. 1 000 000 000

7a37. $\bar{x}_1\left(x_2 x_3 v x_4\left(x_5 \oplus \bar{x}_6\right)\right)$ norm of function equals:
A. 3/32
B. 9/32
C. 5/36
D. 7/32
E. 11/32

7a38. $x_1 x_2\left(\bar{x}_3 \oplus x_4\left(\bar{x}_5 v x_6\right)\right)$ norm of function equals:
A. 3/16
B. 1/8
C. 5/8

D. 1/16
E. 3/4

7a39. $(x_1 \vee x_2) \oplus x_3(\bar{x}_4 \vee \bar{x}_5)\bar{x}_6$ norm of function equals:
A. 21/32
B. 25/32
C. 27/32
D. 11/32
E. 19/32

7a40. x_1 argument activity of $x_1\bar{x}_2(x_3 \vee x_4\bar{x}_5 x_6)$ function equals:
A. 5/32
B. 9/32
C. 9/16
D. 7/16
E. 19/32

7a41. x_3 argument activity of $x_1\bar{x}_2(x_3 \vee x_4\bar{x}_5 x_6)$ function equals:
A. 5/16
B. 11/32
C. 7/32
D. 5/32
E. 13/16

7a42. x_4 argument activity of $x_1\bar{x}_2(x_3 \vee x_4\bar{x}_5 x_6)$ function equals:
A. 13/32
B. 1/32
C. 9/32
D. 7/32
E. 11/32

7a43. The activity of the combination of x_4 and x_5 arguments for $(\bar{x}_1 x_2) \oplus (x_3 \vee \overline{x_4}) x_5$ function equals:
A. 3/4
B. 1/4
C. 5/8
D. 5/16
E. 3/8

7a44. The activity of the combination of x_3 and x_4 arguments for $(\bar{x}_1 x_2) \oplus (x_3 \vee \bar{x}_4) x_5$ function equals:
A. 1/8
B. 7/8
C. 1/4
D. 3/4
E. 5/8

7a45. The activity of the combination of x_4 and x_5 arguments for $(\bar{x}_1 \vee \bar{x}_2) \oplus (x_3 \vee \bar{x}_4\bar{x}_5)$ function equals:
A. 3/4
B. 1/4
C. 5/8
D. 1/8
E. 5/4

7a46. This table defines AND function for 5-valued logic of D-algorithm. Fill in the missing values.

AND	*0*	*1*	*x*	D	$\overline{D}$
0	*0*	*0*	*0*	*0*	*0*
1	*0*	*1*		D	$\overline{D}$
x	*0*				
D	*0*	D		D	*0*
$\overline{D}$	*0*	$\overline{D}$		*0*	*z*

A. All the missing values must be 0
B. All the missing values must be 1
C. All the missing values must be D
D. All the missing values must be ~D (inverse of D)
E. All the missing values must be x

7a47. This table defines OR function for 5-valued logic of D-algorithm. Fill in the missing values.

OR	*0*	*1*	*x*	D	$\overline{D}$
0	*0*	*1*		D	$\overline{D}$
1	*1*	*1*	*1*	*1*	*1*
x		*1*		*1*	
D	D	*1*		D	*1*
$\overline{D}$	$\overline{D}$	*1*		*1*	$\overline{D}$

A. All the missing values must be 0
B. All the missing values must be 1
C. All the missing values must be D
D. All the missing values must be ~D (inverse of D)
E. All the missing values must be x

7a48. The combinational circuit is divided into components each of which must be verified pseudo exhaustively: Let *C={C_1,C_2,…,C_k} be a division of* n-input combinational circuit, with respective $n_1,n_2,\dots,n_k$ inputs of k components. In that case which of the 5 variants does the number of input sets of pseudo exhaustive test correspond to?
A. $n_1+n_2+\dots+n_k$
B. $n_1 \cdot n_2 \cdot \dots \cdot n_k$
C. $2^{n_1+n_2+\dots+n_k}$
D. $2^{n_1} + 2^{n_2} + \dots + 2^{n_k}$
E. $n_1 2^{n_1}+n_2 2^{n_2}+\dots+n_k 2^{n_k}$

7a49. The combinational circuit is divided into components each of which must be verified exhaustively. Let C={C_1,C_2,…,C_k} be *a division of* n-input combinational circuit, with respective $n_1,n_2,\dots,n_k$ inputs of k components. In that case which of the 5 variants does the number of input sets of exhaustive test correspond to?

A. $n_1+n_2+\ldots+n_k$

B. $n_1 \cdot n_2 \cdot \ldots \cdot n_k$

C. $2^{n1+n2+\ldots+nk}$

D. $2^{n1} + 2^{n2} + \ldots + 2^{nk}$

E. $n_1 2^{n1}+n_2 2^{n2}+\ldots+n_k 2^{nk}$

7a50. $(x_1 \oplus x_2)(x_3 x_4 \vee (x_5 \oplus x_6))$ function's norm equals:

A. 9/16

B. 3/16

C. 5/16

D. 11/16

E. 1/16

7a51. $\bar{x}_1 x_2 \oplus (x_3 \vee x_4 \bar{x}_5 \bar{x}_6)$ function's norm equals:

A. 19/32

B. 17/32

C. 11/16

D. 19/32

E. 22/16

7a52. $(\bar{x}_1 x_2 \vee x_3) x_4 (x_5 \oplus \bar{x}_6)$ function's norm equals:

A. 7/64

B. 21/32

C. 5/32

D. 13/16

E. 15/32

7a53. The activity of argument x_1 for the function $(x_1 x_2 \oplus \bar{x}_3) v x_4$ is equal to:

A. 5/8

B. 3/4

C. 1/4

D. 7/4

E. 5/4

7a54. The activity of argument x_3 for the function $(x_1 \bar{x}_2 \oplus \bar{x}_3) v x_4$ is equal to:

A. 1/4

B. 1/2

C. 3/8

D. 5/8

E. 3/16

7a55. The activity of argument x_5 for the function $(x_1 \bar{x}_2 \oplus \bar{x}_3) v x_4 x_5$ is equal to:

A. 3/4

B. 5/8

C. 1/4

D. 3/8

E. 5/16

7a56. The activity of the combination of arguments x_4 and x_5 for the function $x_1 x_2 \oplus (x_3 \vee x_4 \vee x_5)$ is equal to:

A. 5/8

B. 3/2

C. 1/2

D. 5/2

E. 1/8

7a57. The activity of the combination of arguments x_1 and x_2 for the function $(x_1 \vee x_2) \oplus (\bar{x}_3 \vee \bar{x}_4 \vee \bar{x}_5)$ is equal to:

A. 5/8

B. 1/2

C. 3/4

D. 3/8

E. 5/16

7a58. The activity of the combination of arguments x_1, x_2 and x_3 x_2 for the function $x_1 x_2 x_3 (\bar{x}_4 \vee \bar{x}_5)$ is equal to:

A. 5/8

B. 3/16

C. 7/16

D. 5/16

E. 3/8

7a59. What design stage does the technological mapping follow?

A. High level synthesis

B. Logic synthesis

C. Physical synthesis

D. Circuit design

E. Technological design

7a60. In what sequence do the effects of design solutions increase on the final quality of the design a) conceptual, b) structural and c) parametrical synthesis steps?

A. a - b - c

B. c - b - a

C. b - c - a

D. b - a - c

E. c- a - b

7a61. What is the difference of electrical “short” or “long” interconnects at most characterized by?

A. Signal amplitude

B. Signal power

C. Signal edge increase

D. Current power
E. A. and B. together

7a62. Which of the numerated devices are used in high level synthesis algorithms? a) register; b) multiplexer; c) flip-flop; d) transistor; e) inverter; f) driver
A. a-b-e
B. a-c-f
C. a-b-d-f
D. a-b-f
E. c-d-e-f

7a63. Let Q be the number of integers from the segment [1,2, ... , 2010] that are divisible by 2 and 3 but not by 5. Find the number closest to Q.
A. 150
B. 200
C. 250
D. 300
E. 350

7a64. Let Q be the number of integers from the segment [1,2, ... , 2010] that are divisible by 3 and 5 but not by 7. Find the number closest to Q.
A. 100
B. 120
C. 150
D. 170
E. 200

7a65. Let Q be the number of integers from the segment [1,2, ... , 2010] that are divisible by 3 and 7 but not by 11. Find the number closest to Q.
A. 70
B. 80
C. 90
D. 100
E. 110

7a66. Let Q be the number of integers from the segment [1,2, ... , 2010] that are divisible by 5 and 7 but not by 11. Find the number closest to Q.
A. 15
B. 20
C. 50
D. 70
E. 80

7a67. $x_1(\bar{x}_2 \vee x_3)$ norm of function equals
A. 1/4
B. 1/2
C. 3/8
D. 3/4
E. 1/8

7a68. x_1 argument activity of $\bar{x}_1(x_2 \vee \bar{x}_3))$ function equals
A. 3/8
B. 19/32
C. 1/2
D. 1/8
E. 3/4

7a69. $x_3 \vee \bar{x}_4 x_5$ norm of function equals
A. 1/4
B. 3/8
C. 3/4
D. 5/8
E. ½

7a70. x_3 argument activity of $\bar{x}_3 \vee x_4 \bar{x}_5$ function equals
A. 1/4
B. 3/4
C. 5/8
D. 1/2
E. 3/8

7a71. x_1 argument activity of $(x_1 \vee \bar{x}_2) \oplus (\bar{x}_3 \vee \bar{x}_4 x_5)$ function equals
A. 3/4
B. 3/8
C. 1/2
D. 5/8
E. 7/16

7a72. The connected graph has ten vertices and six edges. How many new edges should be added to the graph to get a tree?
A. 1
B. 2
C. 3
D. 4
E. 5

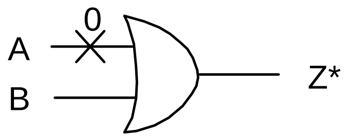
7a73. x_2 argument activity of $(x_1 \vee x_2) \oplus (\bar{x}_3 \vee \bar{x}_4) x_5$ function equals
A. 3/4
B. 5/8
C. 3/8
D. 7/16
E. ½

7a74. *Given an n-input, 1-output combinational circuit C, depending on input variables x_1, x_2, …, x_n and output variable y implementing a function $f(x_1, x_2, …, x_n)$, and a combinational circuit C* is given implementing the function $f^*(x_1, x_2, …, x_n)$ obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its arbitrary line A. The fault F is diagnosable with respect to a class of faults Φ if*
A. The fault F is necessarily detectable
B. The fault F is not necessarily detectable
C. It is necessary and sufficient that the fault F be detectable
D. All the faults from class Φ are necessarily detectable

E. All the faults from class Φ are not necessarily detectable

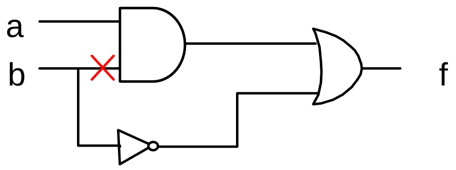
7a75. *Given a 2-input, 1-output logic element of disjunction, depending on input variables x_1, x_2 and output variable Z implementing a function $Z=x_1+x_2$, and a combinational circuit C* is given implementing the function Z*(x_1, x_2) obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its input line A. The fault A/0*
may be detectable by the help of the following set T of test patterns if

Fault circuit



A. T={(00)}
B. T={(11)}
C. T={(10)}
D. T={(00), (11)}
E. T={(00, (01), (11)}

7a76. Given a 2-input, 1-output combinational circuit, depending on input variables a, b and output variable f implementing a function $f = a \& b \vee \bar{b}$, and a combinational circuit C* is given implementing the function Z*(x_1, x_2) obtained from C when a fault F (for example, single stuck-at-0 or stuck-at-1) occurs on its input line A. "X" denotes the fault A/0 (stuck-at-0). As a result of the fault A/0, the circuit will implement a function f*:



A. $f^* = a \& b \vee \overline{a \vee b}$

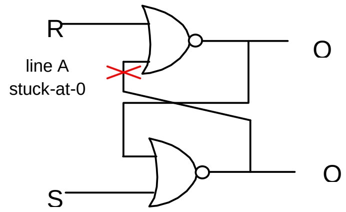
B. $f^* = a \oplus \bar{b}$

C. $f^* = a \vee \bar{b}$

D. $f^* = a \& b \vee \bar{b}$

E. $f^* = (a \wedge b) \oplus \bar{b}$

7a77. Given a 2-input and 2-output sequential circuit (flip-flop) depending on input variables R, S and output functions Q, $\bar{Q}$. "X" denotes the fault A/0 (stuck-at 0). Among the listed sequences of patterns which one detects the fault A/0?



A. SR_1=(01), SR_2=(00)
B. SR_1=(11), SR_2=(11), …, SR_{11}=(11)
C. SR_1=(00),SR_2=(01),SR_3=(10), SR_4=(11)
D. SR_1=(11),SR_2=(00),SR_3=(10), SR_4=(01)
E. SR_1=(11), SR_2=(00)

7a78. Which of elements are used in high level synthesis algorithms: a-Boolean logic elements; b- multiplexer; c-FF; d-transistor; e-register; f-driver?

A. c -d-e-f
B. a-c-f
C. a-b-e
D. a-b-d-f
E. b -e-f

7a79. How is the operation of a selector organized?

A. "False signal" is given to horizontal input and basic input
B. "False signal" is given to horizontal input and "true signal" to basic input
C. "True signal" is given to horizontal input and basic input
D. "True signal" is given to horizontal input and "false signal" to basic input
E. None of the above

7a80. Parametrical synthesis of a circuit precedes the design phase of:

A. Logic design
B. Structural synthesis of a circuit
C. Layout
D. High level synthesis
E. None of the above

7a81. For synchronization of Data Flow Graph (DFG) it is necessary to insert in graph:

A. Registers
B. Selectors
C. Inverters
D. Buffers
E. None of the above

7a82. The design consists of 30 transistors of different widths. Two groups by 15 and 8 transistors from this design are chosen. In how many ways can this selection be made such that the width of arbitrary transistor from the first group will be less than width of arbitrary transistor from the second group?

A. A_{30}^{23}
B. 30^{23}
C. C_{30}^{23}
D. 23^{30}
E. A_{38}^{15}

7a83. For what values of a and b the straight line y=ax+b and circle $(x-1)^2+(y-1)^2\le 1$ intersect?

A. $a=-1, b=0$
B. $a=0, b=1$
C. $a=-2, b=-1$
D. $a=1, b=2$
$a=1, b=1$

7a84. For what value of α the system of linear equations has more than two solutions?

$$\begin{cases} x_1+\alpha x_2+x_3=4 \\ x_1+x_2+2x_3=1 \\ x_1+x_2+\alpha x_3=1 \end{cases}$$

A. 1
B. 0
C. 1
D. 2
E. 3

7a85. For what value of α the function $f(x)=\alpha x^3 - 3x^2 + 3\alpha x - 1$ increases on all real line?

A. -1
B. -0.5
C. 0
D. 0.5
E. 1

7a86. The graph of the function $f(x)=\lim_{n\to\infty}\frac{xe^{nx}}{1+e^{nx}}$ is the function

A. $0.5(x+|x|)$
B. $0.5(x-|x|)$
C. $2x|x|$
D. $|x|-x$
E. $2x$

7a87. Calculate the integral $\int_0^4 x\,\mathrm{sgn}(x-3)dx$.

Here $\mathrm{sgn}\,x=\begin{cases}\frac{x}{|x|}, & x\neq 0\\ 0, & x=0\end{cases}$.

A. -2
B. -1
C. 0
D. 1
E. 2

7a88. From the 6 letters of the alphabet the word “Ararat” is composed. A child, who does not know how to read, mixed those letters and then assembled them in a random order. Find the probability that the new word will also be “Ararat”.

A. $\frac{1}{10}$
B. $\frac{1}{30}$
C. $\frac{1}{60}$
D. $\frac{1}{180}$
E. $\frac{1}{540}$

7a89. Let’s denote as signal the sequence of the eight symbols such that each of them is one of the letters A, B, C, D. How many signals can be composed?

A. 4^8
B. C_8^4
C. A_8^4
D. 8^4
E. C_{12}^4

7a90. Given is the following numerical integration formula (Adam-Bashford):

$$x(\upsilon+4)=x(\upsilon+3)+\frac{55}{24}\Delta t\,x'(\upsilon+3)-\frac{59}{24}\Delta t\,x'(\upsilon+2)+$$
$$+\frac{37}{24}\Delta t\,x'(\upsilon+1)-\frac{9}{24}\Delta t\,x'(\upsilon)$$

Which of the following properties does this method have?

A. Implicit
B. Explicit
C. Three-step method
D. Four-step method
E. B and D variants are correct

7a91. Controllability and observability are defined as:

A. The ability to control the chip from the input pins only
B. The ability to test the whole chip easily through checking the signals at output pins

C. Two metric used in chip-testing to measure testability
D. Two metric used before chip fabrication to test the level of manufacturability
E. None of the above

7a92. Which one of the listed tests for memory devices is a March test?
A. {⇕ (w0); ⇑ (r0, w1); (r1, w0) }
B. {⇕ (w0); ⇑ (r1, w0); ⇓ (r1, w0) }
C. {⇕ (w0); □ (r1, w0); □ (w0, r0)}
D. {⇕ (w0); ⇑ (r0, w1); ⇓ (r1, w0) }
E. {⇕ (w0); ⇑ (r0, w1); ⇓ (r0, w0) }

7a93. What is the complexity of a March test?
A. Linear
B. Square
C. Cubical
D. Exponential
E. NP-hard

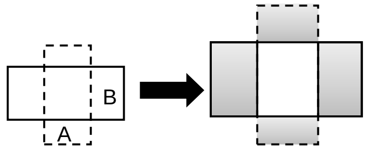
7a94. What is the complexity of the traditional GALPAT test?
A. Linear
B. Square
C. Cubical
D. Exponential
E. NP-hard

7a95. What is the complexity of D-algorithm?
A. Linear
B. Square
C. Cubical
D. Exponential
E. Constant

7a96. In oriented graph, what is called a set of strongly connected components?
A. The set of components which all are connected to one another by sides
B. The set of components where from any component there is a path to all the other components
C. The set of components which has at least one vertex from where there are paths to all the other components
D. The set of components which lacks cycles
E. The correct answer is missing

7a97. What do micromodels characterize?
A. Separate micromodules
B. Information processes, occurring in the object that is being designed
C. Separate elements
D. Interrelations, present between elements
E. Physical processes, occurring in solid environment

7a98. What logic-geometrical operation is presented?



A. OR
B. AND
C. XOR
D. NOT
E. NOR

7a99. In the square with the unit length side the triangle is inscribed (all vertices are on the sides of the square). What is the maximal area of such triangle?
A. $\frac{1}{3}$
B. $\frac{1}{2}$
C. $\frac{2}{3}$
D. $\frac{3}{4}$
E. $\frac{5}{6}$

7a100. Calculate the integral $\int_{-1}^{3}\left|x^2-1\right|$
A. 10
B. 2
C. 4
D. 6
E. 8

7a101. For what values of a and b the function $f(x)=\begin{cases} x^2+1, & x\geq 3 \\ ax+b, & x<3 \end{cases}$ is continuously differentiable?
A. a=6, b= -8
B. a=8, b= -6
C. a=6, b=8,
D. a= -6, b= -8,
E. a=1, b=0

7a102. The straight lines $y=x+1$, $y=10-x$, $y=-6$ and the points A(2.5; 5), B(3.5; 5), C(4.5; 5), D(5.5; 5), E(6.5; 5) are given. Which point is inside the triangle formed by those straight lines?
A. A
B. B
C. C
D. D
E. E

7a103. For what α the function $f\left(x\right)=\alpha^2x^3-2\alpha x^2+x+1$ increases on the real line?

A. *-1*
B. *0*
C. *1*
D. *2*
E. *-2*

7a104. Sort the integrals in the ascending order.

$$I_1=\int_{-0.5\pi}^{0.5\pi}x^3\sin x dx,\ \ I_2=\int_{-0.5\pi}^{0.5\pi}x^2\cos x dx,\ \ I_3=\int_{-0.5\pi}^{0.5\pi}x^2\sin x dx$$

A. *I1, I2, I3*
B. *I3, I2, I1*
C. *I2, I1, I3*
D. *I3, I1, I2*
E. *I2, I3, I1*

7a105. Which of the March tests listed below detects all stuck-at faults in the SRAM memory?

A. *{⇕(w0); ⇕(r0, w1); ⇕(w1,w0)}*
B. *{⇕(w0); ⇕(r0, w0); ⇕(r0) }*
C. *{⇕(w0); ⇕(r0, w1); ⇕(r0) }*
D. *{⇕(w0); ⇕(w1); ⇕(r1) }*
E. *{⇕(w0); ⇕(r0, w1); ⇕(r1) }*

7a106. For the given Boolean function f(x_1,x_2, …,, x_n), the Boolean difference with respect to variable x_i, 1≤ I $_i$≤ n, is called:

A. $f^*(x_1, x_2, \dots, x_n) = x_1^2 + x_2^2 + \dots + x_n^2$
B. $f^*(x_1, x_2, \dots, x_n) = f(0, 0, \dots, 0) - f(1, 1, \dots, 1)$
C. $f^*(x_1, x_2, \dots, x_n) = f(x_1,\dots, 0,\dots, x_n) \oplus f(x_1,\dots, 1,\dots, x_n)$
D. $f^*(x_1, x_2, \dots, x_n) = f(0, \dots, 0, \dots, 0) + f(1, \dots, 0, \dots, 1)$
E. $f^*(x_1, x_2, \dots, x_n) = f(0, \dots, 0, \dots, 0) * f(1, \dots, 0, \dots, 1)$

7a107. Which of the following March tests detects all Address decoder faults in SRAM memories?

A. *{⇕(w0); ⇕(r0, w1); ⇕(w1,w0)}*
B. *{⇕(w0); ⇕(r0, w0); ⇕(r0) }*
C. *{⇕(w0); ⇕(r0, w1); ⇓(r1, w0) }*
D. *{⇕(w0); ⇑(r0, w1); ⇑(r1, w0, r0) }*
E. *{⇕(w0); ⇑(r0, w1); ⇓(r1, w0) }*

7a108. Which of the following March tests detects all stuck-at, Transition and Address Decoder faults in SRAM memories ?

A. *{⇕(w0); ⇕(r0, w1); ⇕(w1,w0)}*
B. *{⇕(w0); ⇕(r0, w0); ⇕(r0) }*
C. *{⇕(w0); ⇕(r0, w1); ⇓(r1, w0) }*
D. *{⇕(w0); ⇑(r0, w1); ⇑(r1, w0, r0) }*
E. *{⇕(w0); ⇑(r0, w1); ⇓(r1, w0) }*

7a109. In what sequence are the following stages of IC design executed?

a) experimental-structural works, b) preparation of experimental sample and testing, c) physical design, d) technical design, e) scientific-research works

A. *a-b-c-d-e*
B. *e-a-d-c-b*
C. *d-a-b-c-e*
D. *e-a-c-d-b*
E. *c-a-e-b-d*

7a110. In what sequence are the following stages of digital IC design executed? a) layout design, b) behavioral-level design, c) logic design, d) RTL design

A. *c-a-b-d*
B. *d-b-c-a*
C. *b-d-c-a*
D. *c-a-d-b*
E. *a-b-c-d*

7a111. What kind of mathematical method is used in component level IC design?

A. Probability theory
B. Theory of queue system
C. Boolean algebra
D. Differential equations system
E. Partial differential equations system

7a112. What kind of parasitic elements can appear in IC?

A. *Only capacitors and resistors*
B. *Only inductances*
C. *Only transistor*
D. *Only A and B*
E. *A, B and C*

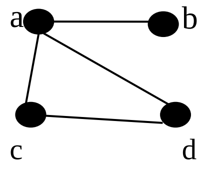
7a113. Which of the given logic expressions is wrong?

A. *AB ¯ · BC ¯ = B ¯ + A+C ¯*
B. *(A+B)(A+C)=A+BC*
C. *AB ¯ + BC ¯ = ABC ¯*
D. *A B ¯ + A ¯ C= AB ¯ (A+C)*
E. *A ¯ ⊕B=A⊕ B ¯*

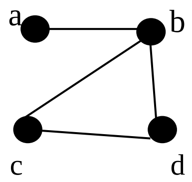
7a114. Which of the given graphs corresponds to the following adjacency matrix?

	a	b	c	d
a	0	1	1	0
b	1	0	1	0
c	1	1	0	1
d	0	0	1	0

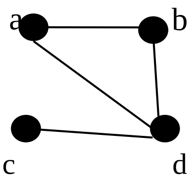
A.



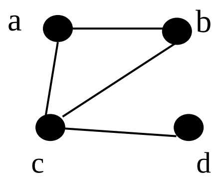
B.



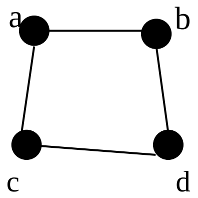
C.



D.



E.



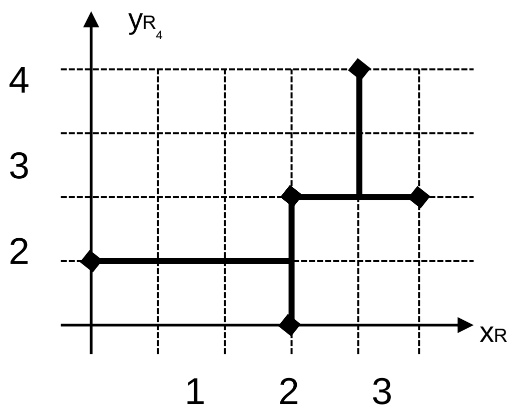
7a115. Which of the given answers more precisely expresses P-MOS transistor structure?

A. Gate is made of SiO
B. n type substrate և p –well are used
C. p type substrate is used
D. n type substrate is used
E. p type substrate and n-well are used

7a116. What is the order of the following processes to get an IC?
1) Packaging 2) Design 3) Chemical technological 4) Photolithography 5) Mask preparation

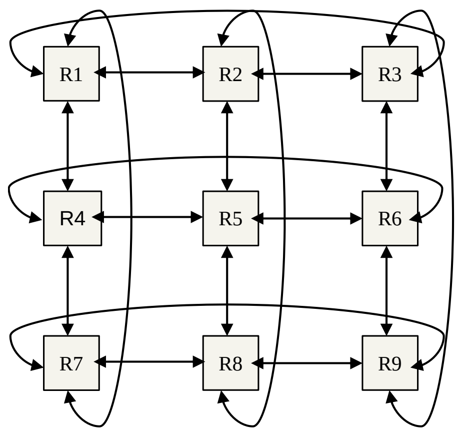
A. 1-3-2-5-4
B. 5-2-3-4-1
C. 5-2-3-4-1
D. 2-5-4-3-1
E. 1-2-3-4-5

7a117. Give the name of the illustrated net model.



A. Steiner tree
B. Source-sink-connection
C. Wire wrap
D. Steiner graph
E. None of the above

7a118. Given is a 3x3 torus network-on-chip (NoC).



What is the maximal number of hops (routers), needed to pass using a minimal routing algorithm (always takes the shortest path)?

A. 1
B. 2
C. 3
D. 4
E. 5

7a119. When simplified with Boolean Algebra (x + y)(x + z) simplifies to:

A. x
B. B.x + x(y + z)
C. C.x(1 + yz)
D. D.x + yz
E. None of the above

7a120. Given N_{10} = {1,2,3,4,5,6,7,8,9,10} set and its two subsets: A={a | a$\in N_{10}$, a – even}, B={b |b∈N_{10}, b ≤5}, C={c|c∈N_{10}, c > 3}.

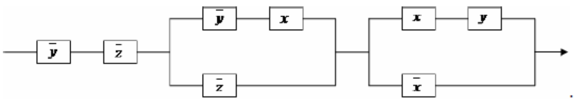
What does (A $\cap \overline{B}$) \C set equal?

A. *{2}*
B. *{6,8,10}*
C. *∅*
D. *N_{10}*
E. *{1,3,5}*

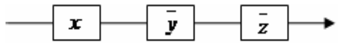
7a121. Which of the given expressions is the disjunctive normal form of f = $(10100110)^T$ function?

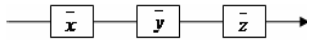
A. $\bar{x}\bar{y}\bar{z} \vee \bar{x}y\bar{z} \vee x\bar{y}z \vee xy\bar{z}$
B. $\bar{x}\bar{y}z \vee \bar{x}yz \vee x\bar{y}\bar{z} \vee xyz$
C. $(\bar{x} \vee \bar{y} \vee \bar{z})(\bar{x} \vee y \vee \bar{z})(x \vee \bar{y} \vee z)(x \vee y \vee \bar{z})$
D. $(\bar{x} \vee \bar{y} \vee z)(\bar{x} \vee y \vee \bar{z})(x \vee \bar{y} \vee \bar{z})(x \vee y \vee z)$
E. $(\bar{x} \vee \bar{y} \vee z)(\bar{x} \vee y \vee z)(x \vee \bar{y} \vee \bar{z})(x \vee y \vee z)$

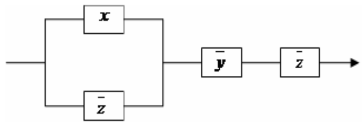
7a122. Given the following contact–relay circuit.

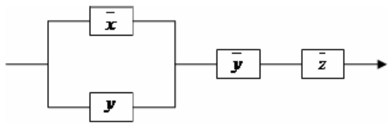


Which of the following circuits is equal to the given circuit?

A.


B.


C.


D.


E. *The correct answer is missing*

b) Problems

7b1.
Construct Zhegalkin polynomial for the threshold function with threshold w=3 and weights of variables ξ_1=2, ξ_2=2, ξ_3=2.

7b2.
Verify the completeness of functions' { $x_1 \vee x_2$, $x_1 \to x_2$, $x_1 x_2 \overline{x_3}$ } system.

7b3.
Using Post theorem verify the completeness of functions' {$1, 0, \bar{x}$, $(x_1 \to x_2) \to x_3$} system.

7b4.
Construct Zhegalkin polynomial of $(x_1 \to x_2)^{\bar{x}_3}$ function.

7b5.
Prove that for N bit number it is possible to calculate the number of 1-s for O(logN) time.

7b6.
Prove that in N bit number it is possible to calculate the number of 1s in O(M) time where M is the number of 1s.

7b7.
Prove that in unordered array K^{th} search can be executed in linear time.

7b8.
Prove that ordering based on binary heap is executed in O(NlogN) time.

7b9.
Construct complete disjunctive normal form of the Boolean function given by 11011011 table.

7b10.
Construct Zhegalkin polynomial of the Boolean function given by 11011101 table.

7b11.
Cayley code of G tree by numbered nodes is given h(G)=(3,5,4,4,5,6,7,8). Reconstruct the tree.

7b12.
Check the completeness of { $x_1^{x_2} \vee x_2^{x_3}, x_1\bar{x}_2, x_1 \mapsto x_2$ } system of functions.

7b13.
Cayley code of G tree by numbered nodes is given h(G)=(3,2,4,4,5,6,8,8). Reconstruct the tree.

7b14.

Check the completeness of $\{ x_1^{x_3} \vee x_2^{x_1}, x_1 \to \bar{x}_2, x_1 \oplus x_2 \}$ system of functions.

7b15.

Calculate arguments' $\xi_1 = 2, \xi_2 = 5, \xi_3 = 7, \xi_4 = 10$ balances and argument activities having w=10 threshold function.

7b16.

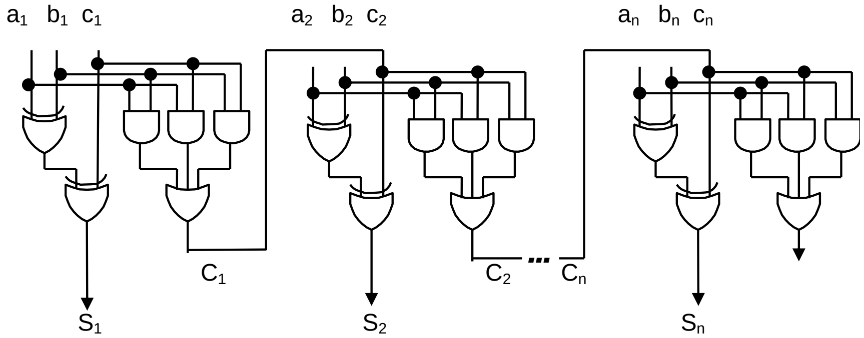
Check the completeness of functions' $\{ x_1 x_2, x_1 \to x_2, x_1 \oplus x_2, x_1 \vee x_2 \}$ system.

7b17.

Given an n-input Boolean function $f(x_1, x_2, \ldots, x_n) = x_1 \oplus x_2 \oplus \ldots \oplus x_n$. Construct the Binary Decision Diagram for $f(x_1, \ldots, x_i, \ldots, x_n)$.

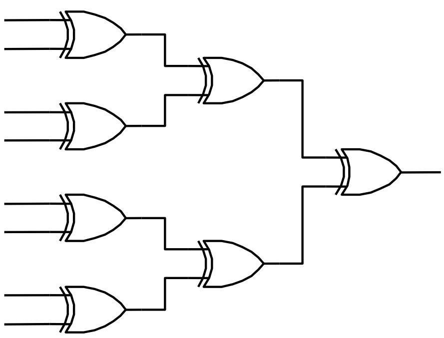
7b18.

Figure depicts the circuit of an n-bit adder. Prove that all possible single stuck-at-0 and stuck-at-1 faults on all lines of that circuit can be detected by means of only 8 test vectors.



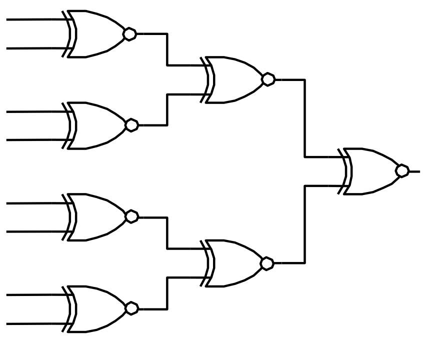
7b19.

Figure depicts the circuit of an N-input parity tree. Prove that all possible single stuck-at-0 and stuck-at-1 faults on all lines in that circuit can be detected by means of only 4 test vectors.



7b20.

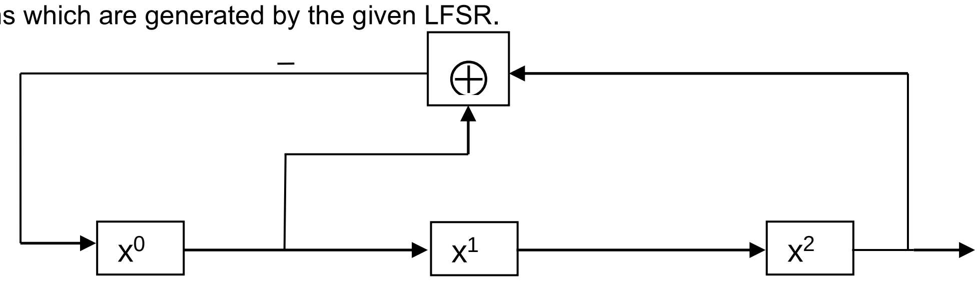
Figure depicts the circuit of N-input tree with negated Modulo 2 elements (gates XOR). Prove that all possible single stuck-at-0 and stuck-at-1 faults on all lines of that circuit can be detected by means of only 4 test vectors.



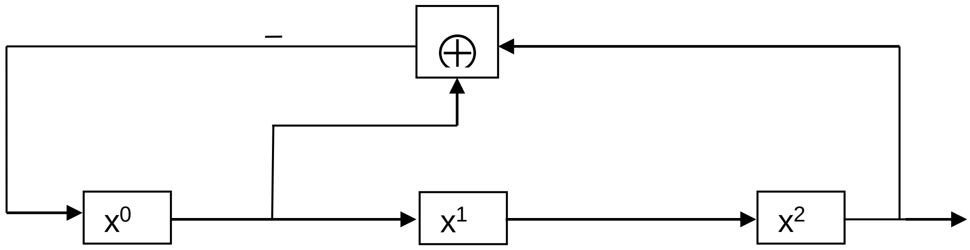
7b21.

The given combinational circuit has 1000000 lines. Constant 0 or constant 1 faults of random numbers can occur there. Find the number of all possible multiple faults.

7b22.
Given a Linear Feedback Shift Register corresponding to characteristic polynomial $1+x+x^3$. Find the subsets of all patterns which are generated by the given LFSR.



7b23.
Given a Linear Feedback Shift Register corresponding to characteristic polynomial $1+x+x^3$. Transform the circuit, adding elementary cell(s) in a way that the obtained new circuit generates one set, consisting of all patterns.



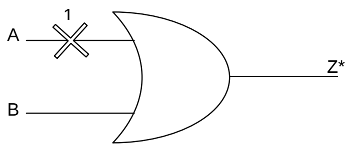
7b24.
Construct Zhegalkin polynomial of the Boolean function given by $f = x_1 \oplus x_3^{x_1 \vee x_2}$.

7b25.
By root tree's 000101001111 code, reconstruct that tree.

7b26.
Calculate arguments activities of $x_1 x_2 \oplus (x_1 \vee x_2 x_3)$ function.

7b27.
Cayley code of G tree by numbered nodes is given h(G)=(2, 3, 3, 4, 5, 5, 8). Reconstruct the tree.

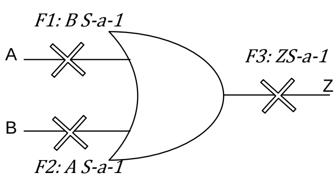
7b28.
Let T(F) be a test set for a fault F, a set of all possible input patterns detecting F.
Definition: Faults F1 and F2 from T(F) are called equivalent faults if T(F1) $\subseteq$ T(F2) and T(F2) $\subseteq$ T(F1), i.e., T(F1) = T(F2).



Find the faults that are equivalent to the mentioned in the figure fault "line A stuck-at-1".

7b29.
The combinational circuit is partitioned into components each to be tested exhaustively. Let $C=\{C_1,C_2,\ldots,C_5\}$ be a partition of a combinational circuit with n inputs into 5 components with 12, 14, 16, 18, 20 primary inputs. Calculate the number of input patterns for the pseudoexhaustive test with respect to the partition.

7b30.
Let T(F) be a test set for a fault F, a set of all possible input patterns detecting F.
Definition: Faults F1 and F2 from T(F) are called equivalent faults if T(F1) $\subseteq$ T(F2) and T(F2) $\subseteq$ T(F1), i.e., T(F1) = T(F2).

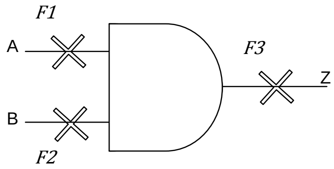


Prove that faults F1, F2 and F3 are equivalent.

7b31.

Suppose, given a 2-input, 1-output combinational circuit depending on input variables A, B and Z output variable implementing the function of conjunction $Z=A \wedge B$. Let T(F) be a test set for a single fault F, a set of all possible input patterns detecting F.

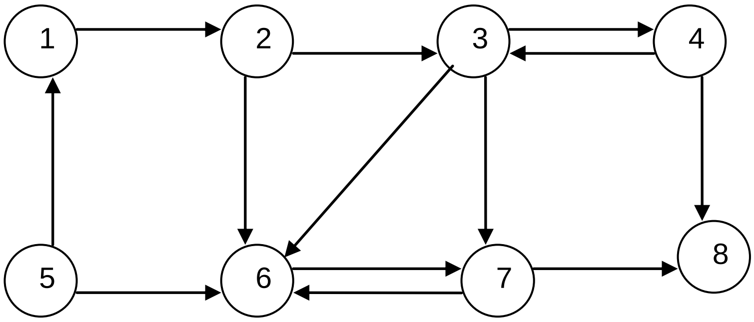
Definition: Faults F1 and F2 from T(F) are called equivalent faults if $T(F1) \subseteq T(F2)$ and $T(F2) \subseteq T(F1)$, i.e., T(F1) = T(F2).



Prove that faults F1, F2 and F3 are equivalent.

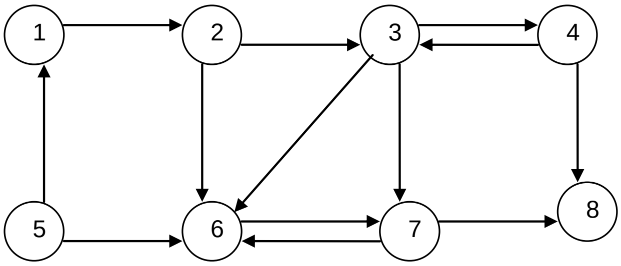
7b32.

In the given directed graph, realize search according to depth starting from the 2[nd] vertex.



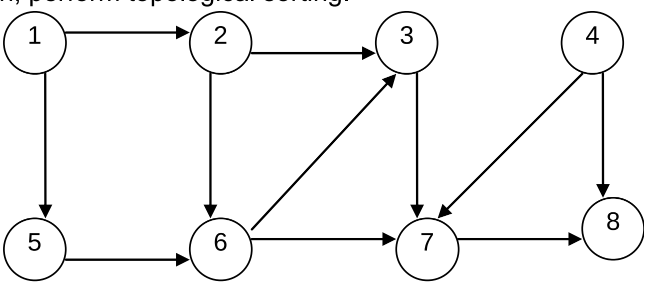
7b33.

In the given directed graph, separate strongly connected components.



7b34.

For the given directed graph, perform topological sorting.



7b35.

In 7 x 7 discrete field realize Lee algorithm by the following initial conditions:

The connecting contact coordinates A(1;2) , B(7;5).

Objective functions are: f_1 – number of crossings; f_2 – connection length.

Both objective functions are minimizing and respectively have the following importance coefficients $a_1=2$, $a_2=1$.

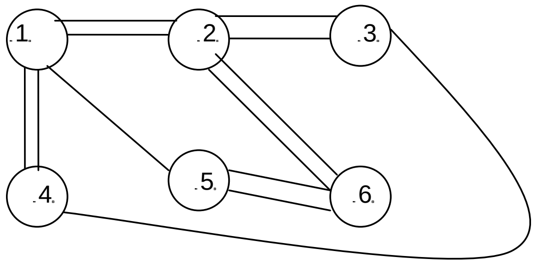
The discrete values of already occupied interconnections are: (2,5); (3,5); (4,1); (4,2); (4,3); (4,4); (4,5); (6,1); (6,3); (6,4); (6,5); (6,6)

7b36.

Given net's contact coordinates, having 5 contacts in a discrete field in conditional units: a(2,9); b(8,8); c(2,5); d(8,3); e(2,2): It is required to construct the orthogonal distance matrix of contacts and by its help compute the minimal tree by Prim's algorithm, realizing the given net.

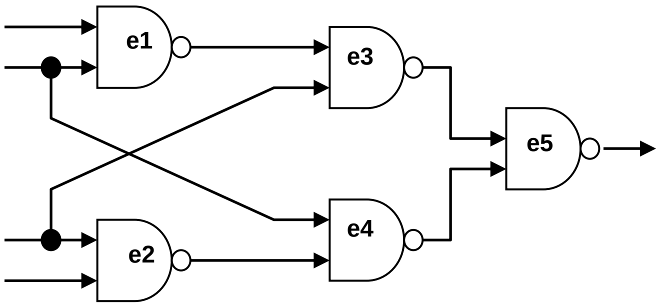
7b37.

For the given graph construct adjacency matrix and using partitioning sequential algorithm, partition into 2 equal parts. As an optimality criterion, take the minimum of connection numbers between the parts.



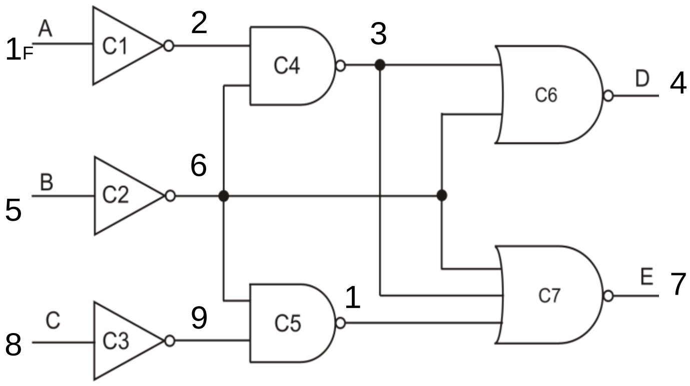
7b38.

Perform initial placement of the given circuit on the line using adjacency matrix, and using minimum interconnects length condition. As an initial element, take e1 cell.



7b39.

Construct the timing graph of the given circuit and compute its critical path delays if the cell delays are given in conditional units: C1=C3=5, C2=10, C5=20, C4=C6=C7= 30.



7b40.

Construct Zhegalkin polynomial of $f = x_1 \oplus x_2^{x_1 \vee x_3}$ Boolean function.

7b41.

Reconstruct the tree of root tree by 001010001111 code.

7b42.

Calculate argument activities of $\overline{x_1} x_3 \oplus (x_1 \vee x_2)$ function.

7b43.

$f = (x_1, x_2, x_3)$ threshold function's variable weights are: ξ_1=3, ξ_2=4, ξ_3=6, and the threshold w=5. Construct the perfect disjunctive normal form of $f = (x_1, x_2, x_3)$ function.

7b44.

Check the completeness of $\{\overline{x_1} \to x_2, x_1x_3, x_1 \vee x_2)\}$ system of functions.

7b45.

Construct Zhegalkin polynomial of the Boolean function given by last column of truth table - 11001011.

7b46.

Calculate arguments activities of $(x_1 \vee \bar{x}_2) \oplus (x_1 \vee \bar{x}_3 x_4)$ function.

7b47.

Check the completeness of $\{x_1^{x_3} \to x_2^{x_1}, x_1 \oplus x_2, x_1x_2\}$ system of functions.

7b48.

$f(x_1, x_2, x_3)$ threshold function's variable weights are: $\xi_1 = 2, \xi_2 = 3, \zeta_3 = 4,$ and threshold $w = 4.$ Calculate arguments activities of the function.

7b49.

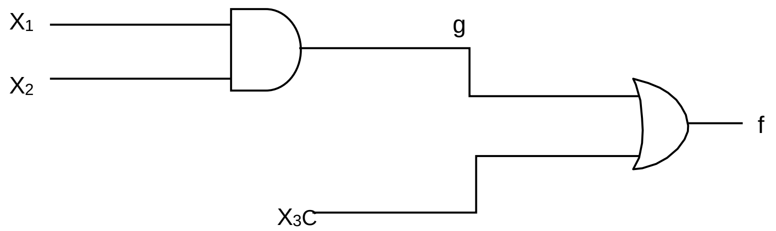
Construct Zhegalkin polynomial for the threshold function with threshold w=8 and weights of variables $\xi_1 = 2, \xi_2 = 3, \xi_3 = 4, \xi_4 = 5$.

7b50.

By root tree's 000100011111 code, reconstruct that tree.

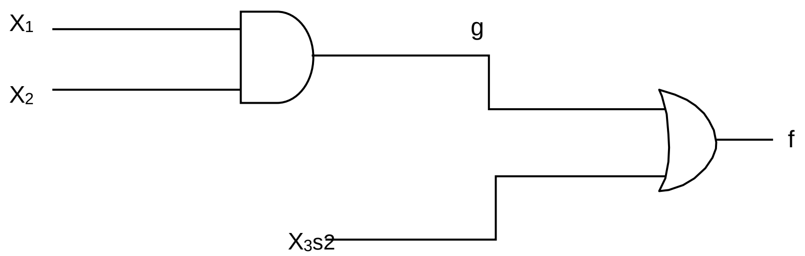
7b51.

Given a combinational circuit with 3 inputs and 1 output depending on input variables x_1, x_2, x_3 and output variable f realizing the function $f=x_1x_2+x_3$. By using the method of Boolean differences, find all test patterns detecting the fault "line g stuck at 0" (g/0).



7b52.

Given a combinational circuit with 3 inputs and 1 output depending on input variables x_1, x_2, x_3 and output variable f realizing the function $f=x_1x_2+x_3$. By using the method of Boolean differences, find all test patterns detecting the fault "line g stuck at 1" (g/1).



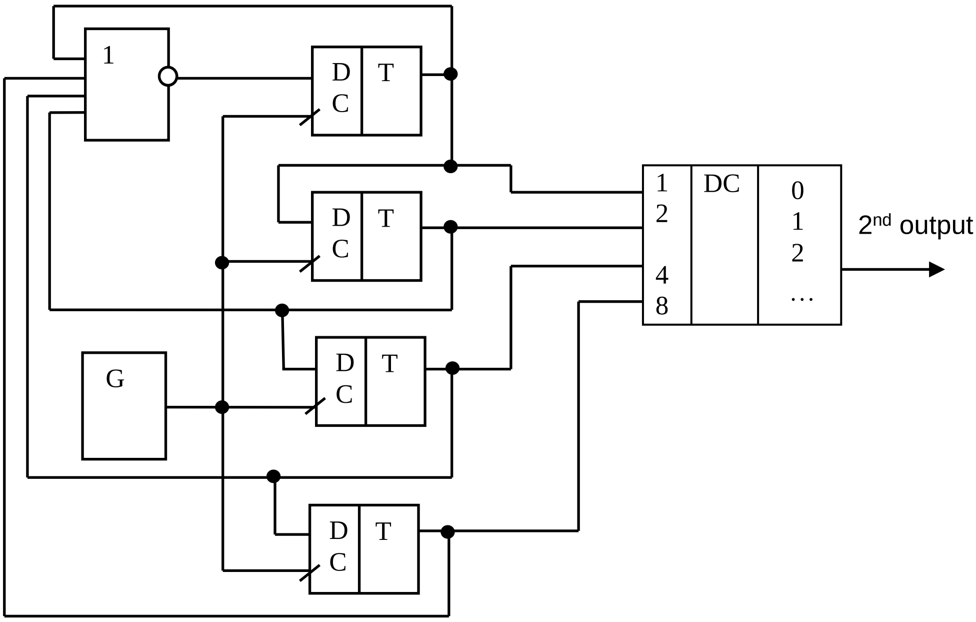
7b53.

A combinational circuit is given with N connectivity lines where for every line each of the faults "constant 0/1" (stuck-at-0, stuck-at-1) is possible. Find the number of all multiple, two and more, faults on the lines of the circuit.

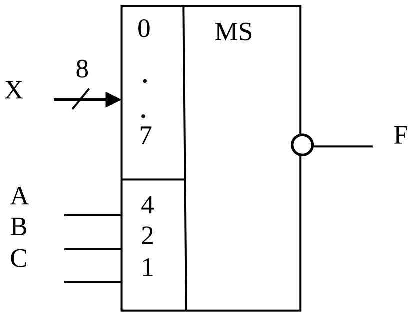
7b54.

A combinational circuit is given with N connectivity lines where for every line each of the faults "constant 0/1" (stuck-at-0, stuck-at-1) is possible. Find the number of all multiple, three and more, faults on the lines of the circuit.

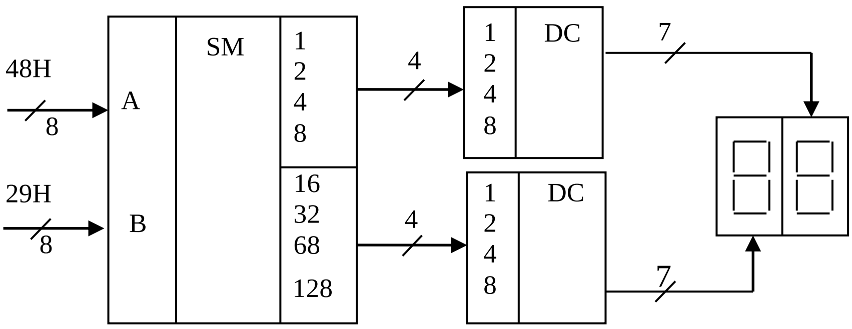
7b55.
Ring counter is shown in the figure. A decoder is connected to its outputs.
How many times will the pulse frequency in the 2nd output of the decoder be smaller than generator frequency? Explain the calculation process.



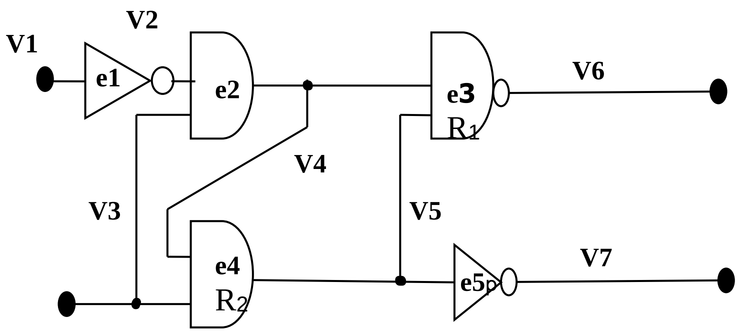
7b56.
Show X (x_7... x_0), 8-bit number that is necessary to be given to the inputs of multiplexer, shown in the figure $F = AB\bar{C} + A\bar{B}C + \bar{A}BC$ to implement logic function. Explain the solution process.



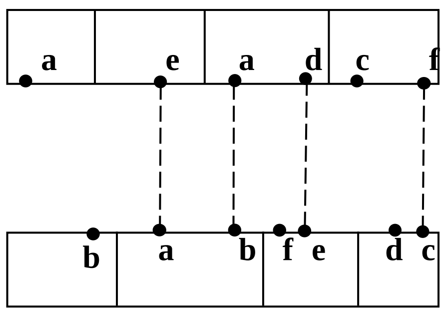
7b57.
A functional circuit, consisting of 8-bit adder and 2 decoders is given. Summands, given to inputs, are presented in hexadecimal system (H denotes hexadecimal system).
It is required to explain the operation of the circuit and define what number will be depicted on the detector.



7b58.
Perform initial placement of the given circuit on the line with minimization condition of interconnect total length (use adjacency matrix). Take e1 as an initial element.



7b59.
For two-row placement of cells, implement the interconnects of a, b, c, d, e, f nets in two-layer orthogonal form, using horizontal paths with minimum numbers. Solve the problem by the application of monochromatic graph.



7b60.
The following hardware and its delay values in conventional units (c.u.) are given:
multiplier-3, delay -3 c.u.
adder -1, delay -2 c.u.
Required to:

a) Construct Data Flow Graph (DFG) of the device and a functional circuit that will allow calculating the following expression: Y=((axb)+c)x(dxe).
b) Define where and what value (in conventional units) of delay elements should be added to exclude signal racing.

7b61.
The following devices are given:
Multiplier - 3
Adder -1
4-input multiplexer - 2
Required to:

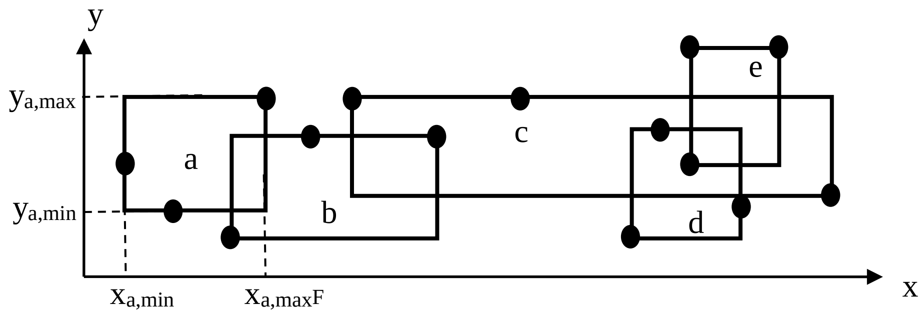
a) Design the functional circuit of the device without using multiplexers which will allow calculating the following expression: Y=((axb)+c)x(dxe);
b) Define the operating cycles of the circuit and the actions, taken at each cycle.
c) Perform device optimization (reduce the number of used multipliers), using multiplexers. Design the new circuit and its operating cycles.

7b62.
Contacts, belonging to a, b, c, d, e nets on x, y plane are given. For each net the minimum rectangular surrounding it is composed, as illustrated in the figure. The minimum and maximum coordinates (in conditional units) of edges of those rectangles are shown in the table.
It is required to:

a) Estimate the internal boundary of metal layers, necessary for net routing, if the overlaps and vias of rectangles, surrounding the nets are not allowed.
b) Define nets distribution by 2 metal layers, which will provide maximum routability, if vias are not allowed.

Use the chromatic number of weighted graph of nets overlap. Define the chromatic number heuristically. As a routability condition of the same level of 2 nets, use minimum condition of relative overlap area of rectangles, surrounding them. $f_{ij} = \dfrac{S(V_i \cap V_j)}{\max\{S(V_i), S(V_j)\}} \rightarrow \min$

where $S(V_i)$ and $S(V_j)$ are areas of rectangles, surrounding V_i and V_j nets respectively, $S(V_i \cap V_j)$ is the overlap area of rectangles, surrounding V_i and V_j nets.



	a	b	c	d	e
x_{min}	1	3	6	11	12
x_{max}	4	8	15	13	14
y_{min}	2	1	3	1	4
y_{max}	7	5	7	5	8

7b63.

Find the function y, continuous in R, which satisfies an integral equation $xy(x) - \int_0^x y(t)dt = f(x)$, where f is a given continuous function. When this problem has a solution, and if it has, is it unique?
Hint. First, consider the cases when $f(x) = x^k$, for k=0,1,2.

7b64.

Suppose that the function f on the interval [a,b] satisfies the condition $|f(x) - f(y)| \le C|x - y|^\alpha$, $x, y \in [a, b]$, where C is a constant and $\alpha > 1$. Prove that the function f is identically constant.

7b65.

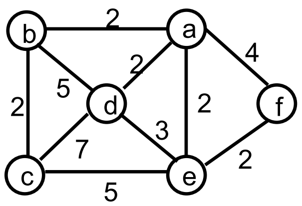
Prove that for arbitrary real numbers a,b and for even number n the equation $x^n+ax+b=0$ has not more than two real roots. What can be said for odd n?

7b66.

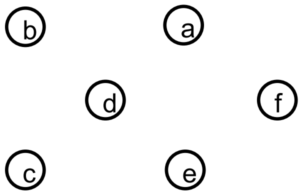
Find the differential function f, not equal to zero identically, the solution of the following equation $f(x+y) = f(x)f(y)$, $x, y \in R$. How many such functions there exist?

7b67.

The following picture shows a graph with six nodes. The numbers near the edges represent the length of the edge, i.e. the distance between the nodes. Please construct the shortest path tree rooted at node d. Use the given table and draw the resulting tree.

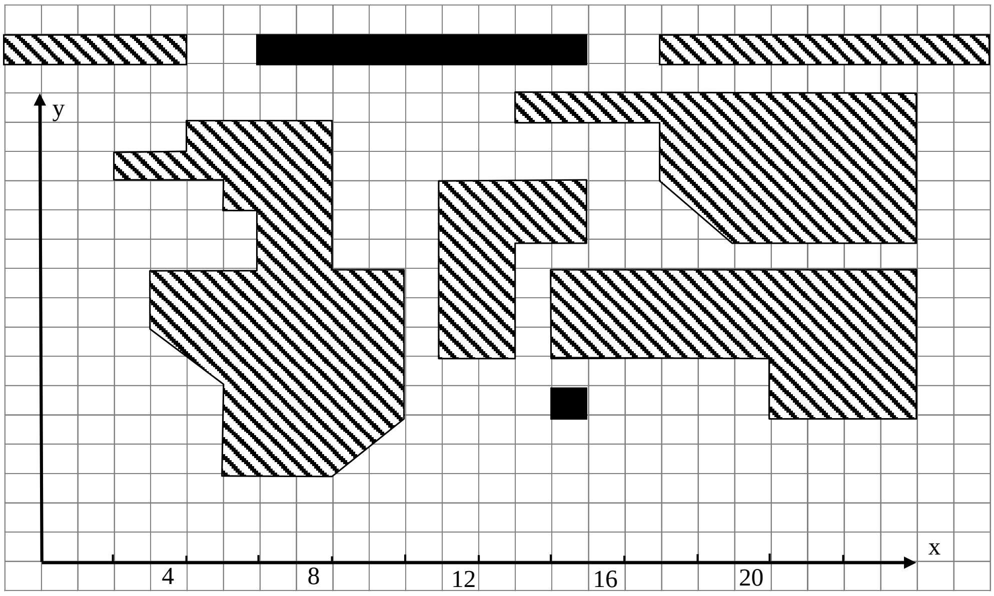


Graph0.

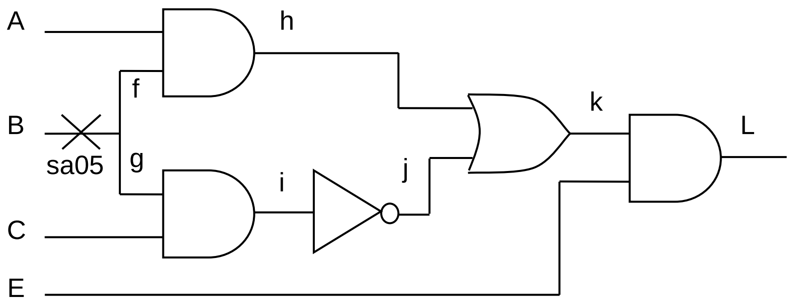


z	$L_{min}(d,a)$	$L_{min}(d,b)$	$L_{min}(d,c)$	$L_{min}(d,e)$	$L_{min}(d,f)$

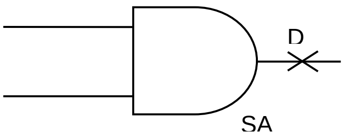
7b68.
Consider the following routing problem for a printed circuit board. Use the standard Lee algorithm to determine and highlight the shortest paths which connect the black boxes. Start at the upper box. Restrict your search window in y-direction to the vertical positions of the boxes and in x-direction to [3:20]



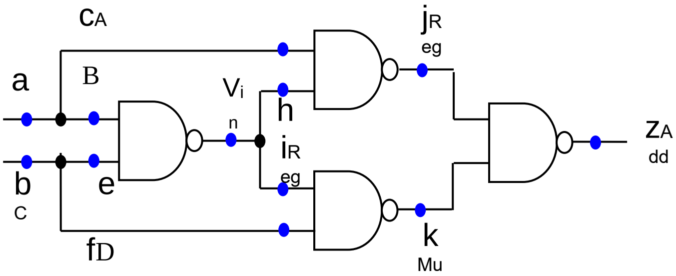
7b69.
For the shown circuit, where line B has a stuck-at-0 fault, construct a sensitive path detecting this fault, using the main ideas of D-algorithm.



7b70.
For the stuck-at-1 fault, shown in the following logical element, construct its Primitive D-Cubes of Failure (PDCFs), using the main ideas of D-algorithm.

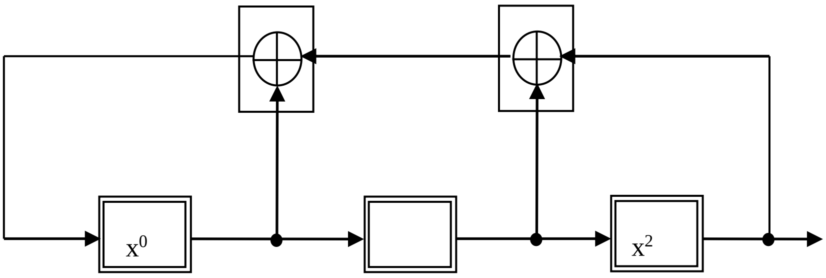


7b71.
Reduce the set of all single stuck-at-0, stuck-at-1 faults in the given circuit, using the idea of “checkpoint” and the main theorem on it. Indicate the initial and the reduced sets.



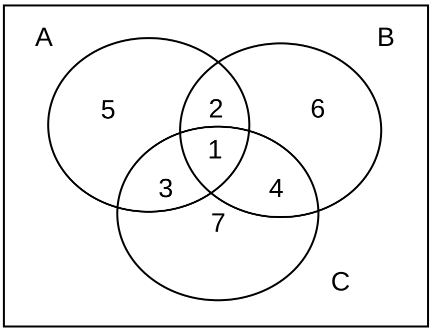
7b72.

For the Linear Feedback Shift Register (LFSR) given with the characteristic polynomial $1+x+x^2+x^3$, find the cycles of patterns of length 1 generated by it.



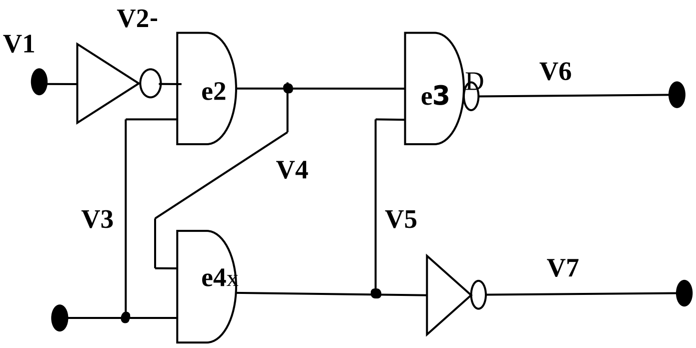
7b73.

On the Venn diagram (the schematic representation of possible crossings of several sets), show the segment that corresponds to C· (A+B) ¯ logic expression.



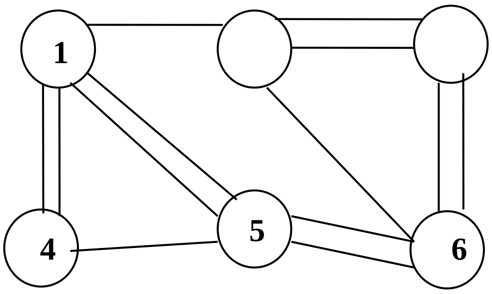
7b74.

Construct the timing graph of the given circuit, compute the earliest and the latest times of signal formation on all circuits from V1 to V7, time savings. Define the critical path and its delay if the delays of the elements are given in conventional units: Te1=Te5=10, Te3=15, Te2=Te4=20.



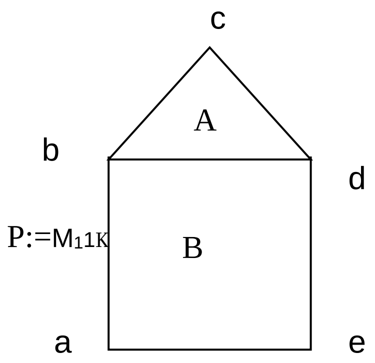
7b75.

For the given graph construct adjacency matrix and using sequential algorithm of partitioning, partition into 2 equal parts. As an optimality criterion, take the minimum number of connections between the parts.



7b76.

For the topological graphical image below, construct the hierarchic and net graph models of data representation if (x,y)coordinates of vertices of the image are known.



7b77.

Solve the functional equation

$$f(x)\,f(-x) = c^2 = \left(f(0)\right)^2.$$

Here f is a single-valued positive function of the real variable x.

7b78.

Suppose a is a given real number. It is needed to find a single-valued real function that for all are real numbers satisfies the equation:

$$e^{as} f(t) = f(t+s) - f(s).$$

7b79.

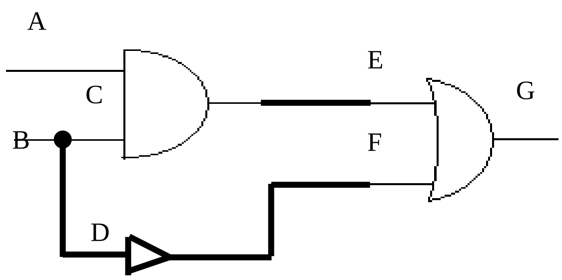
Suppose x_0 and x_1 are given numbers. The sequence $\{x_n\}$ is given by recurrent formula $x_n = \dfrac{n-1}{n} x_{n-1} + \dfrac{1}{n} x_{n-2}$, where $n = 2,3,\dots$. Find $\lim\limits_{n\to\infty} x_n$.

7b80.

On a road with a length a two people are standing. Find the probability that the distance between them isgreater than b. Consider general case, too (with n people).

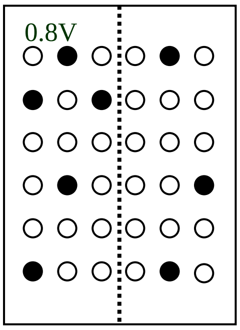
7b81.

In the figure below, indicate which stuck-at fault on a line is redundant and justify the claim.



7b82.

Is it possible to repair the depicted memory with faults indicated as black circles with two redundant rows and two redundant columns?



7b83.

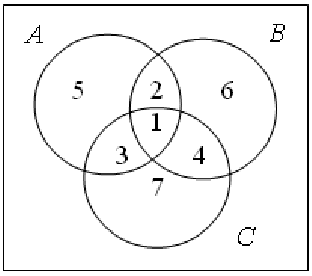
Construct a March test of minimal complexity with minimal number of March elements that detects all stuck-at-0 and stuck-at-1 faults in the memory.

7b84.

Construct a March test of minimal complexity with maximal number of March elements that detects all stuck-at-0 and stuck-at-1 faults in the memory.

7b85.

A,B,C partially intersected sets are shown on Venn diagram (which is the schematic representation of possible intersections of several sets), and as a result of those intersections different subsets are indicated with 1-7 numbers.



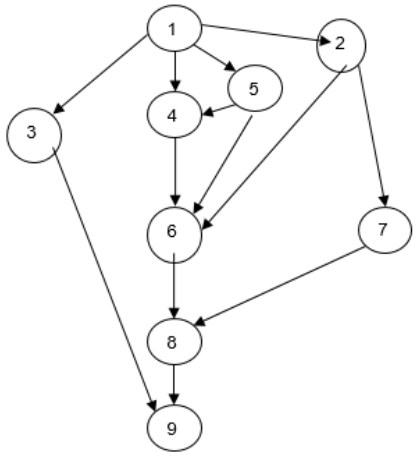
It is required to define the logic expressions corresponding to the following sets of the subsets.

1) {1, 2}
2) {1, 4}
3) {1, 2, 4}
4) {4, 7}
5) {1, 2, 4, 7}
6) {1, 2, 3, 4, 5, 7}

7b86.

A conditional design route is shown in the figure where the vertices correspond to the following design activities:

1. Specification
2. Library selection
3. Test development
4. High level synthesis
5. Timing analysis
6. Logic synthesis
7. Technological mapping
8. Physical synthesis
9. Testing



t is required to implement topological sorting of design steps according to depth search algorithm and based on the gained results sort the vertices in one horizontal line so that feedbacks are excluded.

7b87.

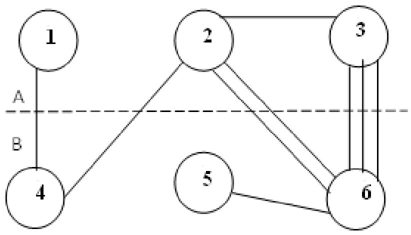
4 circuits are given (a,b,c,d). Conventional coordinates of contacts, belonging to them, are:

a(x, y)- $a_1(1,6)$; $a_2(3,6)$; $a_3(7,4)$

b(x, y)- b_1(4,5); b_2(11,3)
c(x, y)- c_1(9,4); c_2(21,1)
d(x, y)- d_1(16,6); d_2(19,3)
It is required to construct an overlapping graph in case of perpendicular routing and estimate the upper limit of the number of minimum layers, necessary for implementation of interconnects, conditioned that overlapping and interlayer transitions of rectangles, involving nets, are not allowed. To solve the problem, use the chromatic number of overlapping graph of rectangles that involve nets. Decide the chromatic number by heuristic way.

7b88.

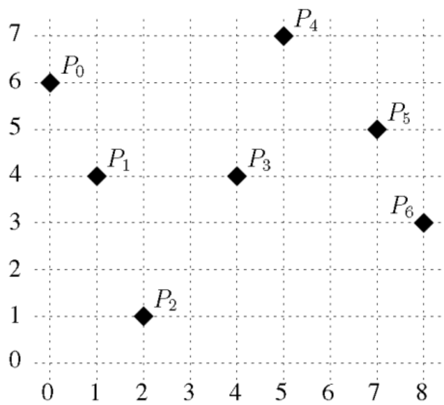
To partition the graph into A and B between A and B parts, by means of iteration algorithm of moving the vertices in pairs, calculate the number of present edges between A and B parts in the result of all possible exchanges of pairs and define the pair of vertices, the exchange of which will lead to the minimum of the number of edges.



7b89.

Steiner Tree

Draw the Steiner Tree using the algorithm by Hanan and the direction from left to right.

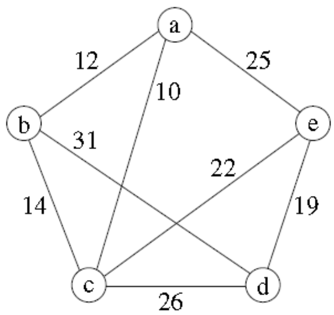


Estimate the net length by using the half perimeter of enclosing rectangle.

7b90.

Minimum Spanning Tree (KRUSKAL)

A weighted graph is given:



Construct the minimum spanning tree using the KRUSKAL method. Fill the added edge e and its weight d of each step i in the following table.

Step i	1	2	3	4
Edge e				
Weight d				

7b91.

How many usual different fractions can be made from 3, 5, 7, 11, 13, 17 numbers so that each fraction includes 2 different numbers. How many of these fractions will be smaller than 1?

7b92.

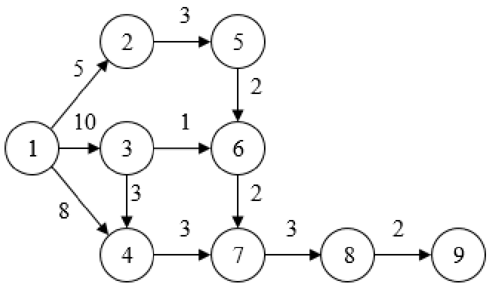
The coded gate code consists of a combination of 4 numbers, each of which is encoded by any number from 0 to 9.

a. Define the opening probability of a gate in case of typing random code.

b. Define the opening probability of a gate if it is known in advance that all 4 digits of the code are different in case of typing random code.

7b93.

Given a weighted directed graph, which is also called the network model, where the numbers on the edges show the times required for certain operations, and the vertices are the events, made as a result of certain operations.



It is required to:

1. Identify the earliest time when each event will take place;
2. Identify the latest time when each event will take place;
3. Identify the time reserve of each event;
4. Identify the critical path from 1st event to the 9th event.

8. OBJECT-ORIENTED PROGRAMMING

a) Test questions

8a1. A function is formed that displays data (on the screen) as well as writes them in the file. Referring to the scenario, which one of the following function declarations satisfies that need?

A. void print(cout);
B. void print(ostream &os);
C. void print(istream &is);
D. void print(ofstream ofs);
E. void print(istream is);

8a2. After performing the below mentioned code, which is the value of n?
int n = !(!5 & !7)

A. false
B. 1
C. 3
D. 5
E. It contains an error. After using ! operator, constant values should be definitely taken in brackets, e.g.(!5)

8a3. Small function is present, which is often called from several special places. How can the implementation of the codes be accelerated which use the given function?

A. Make function virtual
B. Replace floating point computation of integer numbers, to use FPU device
C. Reduce the use of automat variables
D. Make all the variables of that function volatile
E. Make function inline

8a4. Which is the difference between non-specialized function's member and constructor?

A. Constructor can return values, and member-functions - no
B. Member-functions can define values, constructors – no.
C. Constructor can define values, and member-functions - no
D. Member-functions can return values, and constructors - no
E. Constructor can announce values, and member-functions - no

8a5. const int x= 0xFFFE;
int y = 2;
int z = x&&y;
Which is the value of z, in terms of the above code?

A. 0
B. 1
C. 2
D. 3
E. 4

8a6. Which of the below mentioned statements concerning overloading of ++ operator is true?

A. It is impossible to overload prefix ++ operator
B. It is impossible to overload postfix ++ operator
C. It is necessary to use additional int type parameter to overload ++ postfix operator
D. It is always necessary to create prefix ++ operator
E. It is impossible to overload both prefix and postfix ++ operators for one class.

8a7. Binary search complexity is

A. O(logN), where N is the number of elements
B. O(NlogN)
C. O(N)
D. $O(N^2)$
E. The correct answer is missing

8a8. The complexity of Prim's algorithm is

A. O(|E|)
B. $(|V|^2)$
C. O(|E||V|)*
D. O(|E|+|V|)
E. The correct answer is missing

8a9. When the class is inherited from base as public, which of the below mentioned statements is right?

A. All the members of base class become public members of inherited class
B. All the members of inherited class become public members of base class
C. All the protected members of base class are protected members of inherited class
D. All the members of base class become protected members of inherited class
E. All the members of inherited class become private members of base class

8a10. The ability to invoke a method of an object without knowing exactly what type of object is being acted upon is known as which one of the following?

A. Encapsulation
B. Class relationship
C. Inheritance
D. Polymorphism
E. Friend relationship

8a11.
```
class X
{
  int I;
public:
  int f() const;
};
int X::f() const {return I++;}
```
Where is an error in the above written code?

A. X::f member-function must be static
B. X::f member-function is constant but changes non-mutable data-member of the object
C. X::I data-member lacks access specifier
D. X::f member-function cannot change as it lacks access specifier
E It is not possible to change the integer I as it lacks access specifier

8a12. The complexity of quick sorting algorithm for the worst case will be

A. O(logN), where N is the number of elements
B. O(NlogN)
C. O(N)
D. $O(N^2)$
E. The correct answer is missing

8a13.
```
class Base {
public:
  Base();
  ~Base();
  int getBaseNum();
private:
  int baseNum;
};

class A : public Base{
public:
  A();
  ~A()
  float getBaseNum();
private:
  float baseNum;
};
```
Which concept is presented through the code in the example?

A. Recursion
B. Polymorphism
C. Inheritance
D. Reloading of functions
E. Virtual functions

8a14.
```
int i = 4, x = 0;
do {
  x++;
} while(i--);
```
What is the value of X after performing the above written code?

A. 5
B. 4
C. 0
D. Infinite
E. There is syntax error while cycle cannot be formed as mentioned above

8a15. The complexity of Floyd algorithm is

A. $O(N^3)$*, where N is the number of nodes*
B. O(NlogN)
C. O(N)
D. $O(N^2)$
E. The correct answer is missing

8a16. The complexity of subline search in Knut-Morris-Pratt algorithm on average will be (n – length of the line, m – length of the subline)

A. O(n)
B. O(m)
C. O(n+m)
*D. O(n*m)*
E. The correct answer is missing

8a17.
```
class MyClass {
public:
  MyClass();
  virtual void MyFunction()=0;
};
```
Which is the below written statements is correct for the given code?

A. MyClass is a pure virtual class
B. Class definition is wrong
C. MyClass is a virtual base class
D. Function returns value
E. MyClass is an abstract class

8a18. Which of the below written statements is correct for function overloading?

A. Although the return type can be modified, the types of the parameters can as well. The actual number of parameters cannot change.
B. Function overloading is possible in both C++ and C
C. Templates and namespaces should be used to replace occurrences of function overloading.
D. Overloaded functions may not be declared as "inline."
E. The compiler uses only the parameter list to distinguish functions of the same name declared in the same scope.

8a19. The complexity of Dexter algorithm is

A. $O(|E|)$
B. $O(|E|*|V|)$
C. $O(|V|^2)$
D. $O(|E|+|V|)$
E. The correct answer is missing

8a20. Assume an algorithm determines the number of triangles formed by *n* points in the plane. What is the maximal possible output of A for n=7?

A. 35
B. 27
C. 17
D. 15
E. The correct answer is missing

8a21. What is the difference between class and struct?

A. Class must contain constructor, and struct may not have it
B. Struct does not have inheritance opportunity
C. Struct does not have deconstructor
D. By default input specificators are distinguished
E. No difference

8a22. Which is the value of z in case of the code below?

```
const int x= 012;
int z = 1 << x;
```

A. 0
B. 1024
C. 4096
D. 2048
E. It contains an error and will get compilation error

8a23. Which of the mentioned cycles is infinite?

A. `for (int i=1;i>23;i++);`
B. `for (int i=0;i>=1;i++);`
C. `for (int i=10;i>6;i++);`
D. `for (int i=5;i>15;i++);`
E. `All the cycles are finite`

8a24. After performing the code below, what will be displayed on the screen? (assume `sizeof(int) = 4)`

```
#include <iostream>
using namespace std;
void main(){
    int (*p)[10]= {NULL};
    int k= int((size_t)(p+1) -
(size_t)p);
      cout<<k<<endl;
}
```

A. 1
B. 2
C. 4
D. 10
E. 40

8a25. Which of the mentioned ones is not heredity access attribute

A. public
B. private
C. virtual
D. protected
E. All are heredity access attribute

8a26. For a given pair of integers *n, k* it is calculated n^k. Assuming that calculation uses only multiplications, show the minimal number of multiplications among represented in the table that is enough to calculate 5^{1024}.

A. 12
B. 11
C. 10
D. 9
E. 8

8a27. After performing the code below, which is the value of n?

```
int i = 5;
int n = i++-1;
```

A. 6
B. 5
C. 4
D. 3
E. It contains an error and will get compilation error

8a28. After performing the code below, which is `the value of b?`

```
#include <iostream>
using namespace std;
void main (){
      int a = 0;
      int b = 2;
      switch (b)  {
            case 1:
                  a=1;
                  break;
            case 2:
                  int b=0;
      }
}
```

A. 0
B. 1
C. 2
D. There is syntax error, switch is not possible to form as described above
E. The program will work infinitely

8a29. Which of the mentioned is not C++ data type?

A. unsigned long
B. unsigned short
C. unsigned char
D. unsigned int
E. All are C++ data types

8a30. Which of the mentioned is not one of the basic clauses of object-oriented programming?

A. Encapsulation
B. Typification
C. Inheritance
D. Polymorphism
E. All the mentioned belong to the basic clauses of object-oriented programming.

8a31. An algorithm is developed that for any given list of natural numbers L = {a_1, …, a_n} finds the maximum, minimum elements and the arithmetical average value of L. What is the minimal number of passes in reading L that is enough get the output in the algorithm?

A. 5
B. 4
C. 3
D. 2
E. 1

8a32. After performing the code below, which is the value of n?

int n = 1 << 3 * 2 + 1;

A. 1
B. 17
C. 65
D. 128
E. It contains and error and will get compilation error

8a33. To classify the following 1,2,3,5,4 sequence ascending, it is more appropriate to use

A. Quick Sort
B. Bubble Sort
C. Merge Sort
D. Heap Sort
E. No appropriate version

8a34. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
using namespace std;
double A;
void main ()
{
        int A;
        A=5;
        ::A = 2.5;
        cout<<A<<"    "<<::A;
}
```

A. 5 2.5
B. 2.5 5
C. 5 5
D. 2.5 2.5
E. The program contains a syntax error

8a35. How much is the complexity of algorithm to add element in binary tree?

A. $O(N^2)$, where N is the number of nodes
B. O(logN)
C. O(N)
D. O(1)
E. The correct answer is missing

8a36. An algorithm is developed that for any given list of natural numbers L = {a_1, …, a_n} finds the sum $\sum_{i=1}^{n}(a_i - \bar{a})^2$, where $\bar{a}$ denotes the arithmetical average of the elements list L: What is the floor amount of passes enough to calculate the output?

A. 1
B. 2
C. 3
D. 4
E. 5

8a37. Which of the statements is correct?

A. Class cannot have 2 constructors
B. Class cannot have 2 destructors
C. Virtual destructor does not exist
D. All the above mentioned statements are correct
E. All the above mentioned statements are wrong

8a38. The complexity of Merge Sort algorithm in the worst case will be:

A. O(NLogN)
B. $O(N^2)$
C. O(N)
D. $O(N^3)$
E. The correct answer is missing

8a39. After performing the code below, what will be displayed on the screen?

```
#include <stdio.h>
class a {
public: virtual void print()
{printf("a");}
};
class b: public a{
public: virtual void print()
{printf("b");}
};

int main(){
    b b0;
    a a0= b0, &a1= b0;
    a0.print();
    a1.print();
    return 0;
}
```

A. aa
B. ab
C. bb
D. ba
E. The program contains syntax error

8a40. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
using namespace std;

void main(){
    int c = 1;
    c= ++c + ++c;
      cout<<c;
}
```

A. 2
B. 3
C. 4
D. 5
E. 6

8a41. What is the output of the following part of the program?

cout << (2 | 4 ^ ~3);

A. 0
B. 1
C. 2
D. 3
E. the correct answer is missing

8a42. How many errors are below?

```
class B {}
class A
        :  public B
{
        int m_value
        int get_value(int = 0)
```

```
        {
                return m_value;
        }
}
int main () {
        A a();
        a = a;
        a.*get_value();
        return 0;
}
```

A. 3
B. 4
C. 5
D. 6
E. 7

8a43. What is (7 >> 1 << 1) expression value?
A. 5
B. 6
C. 7
D. 8
E. the correct answer is missing

8a44. What is the output of the following part of the program?

```
int n = 5;
switch(n){
        case '5':
                cout << "A \n";
                break;
        case 5:
                cout << "B \n";
        default:
                cout << "C \n";
                break;
}
```

A. A
B. B
C. C
D. BC
E. AC

8a45. Complexity of “merge” sorting algorithm
A. linear
B. constant
C. logn
*D. n*logn*
E. square

8a46. int n = !(!5 & !7)
What is the value of n after performing the code above?
A. false
B. true
C. 0
D. 1
E. It has an error. Using ! operator, constant values must be written in brackets. For example, (!5)

8a47. Complexity of adding element in search balanced binary tree
A. linear
B. constant
C. logn
*D. n*logn*
E. square

8a48.

```
int i = 4, x = 0;
do{
  x++;
}while(i--);
```

After executing the above written code, which is the value of X?
A. 0
B. 1
C. 3
D. 4
E. 5
F.

8a49.

```
class MyClass
{
public:
 MyClass();
 virtual void MyFunction()=0;
};
```

Which statement is true for the above mentioned code?
A. Class definition is wrong
B. MyClass is a virtual class
C. MyClass is a virtual base class
D. MyClass is an abstract class
E. the correct answer is missing

8a50. What is the value of (13 >> 1 << 1) expression?
A. 11
B. 12
C. 13
D. 14
E. 15

8a51. How many errors does the following part contain?

```
class A
      :  int
{
      int m_value
      int get_value(int = 0)
{
      return m_value;
}
}
int main () {
      A a();
      a = a;
      a->get_value();
return 0;
}
```

A. 2
B. 3
C. 4
D. 5
E. 6

8a52. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
struct A {
        virtual void f(int x = 0) {
                std::cout << "A: " <<
x << std::endl;
```

```
       }
};
struct B : public A {
       virtual void f(int x = 1) {
              std::cout << "B: " <<
x << std::endl;
       }
};
int main()
{
       A* p = new B();
       p->f();
       return 0;
}
```

A. A 0
B. A 1
C. B 0
D. B 1
E. The correct answer is missing

8a53. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
struct A {
       virtual ~A() {
              std::cout << "A" <<
std::endl;
       }
};
struct B : public A {
       virtual ~B() {
              std::cout << "B" <<
std::endl;
       }
};
int main() {
       A* p = new B();
       delete p;
       return 0;
}
```

A. A
B. A B
C. B
D. B A
E. The correct answer is missing

8a54. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
#include <memory>
void f(std::auto_ptr<int> a) {
       *a = 3;
}
int main() {
       std::auto_ptr<int> p(new
int(0));
       f(p);
       std::cout << *p <<
std::endl;
       return 0;
}
```

A. 0
B. 3
C. The program contains compile-time error
D. The program contains run-time error
E. The correct answer is missing

8a55. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
struct Base {
       virtual void f() {
              foo();
       }
       virtual void foo() = 0;
};
struct Derived : public Base {
       virtual void foo() {
std::cout << "Derived" <<
std::endl; }
};
int main() {
       Base* pb = new Derived();
       pb->f();
       return 0;}
```

A. The program contains compile-time error as foo function has been called without description
B. Derived
C. Nothing
D. The program contains run-time error
E. The correct answer is missing

8a56. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
int main() {
       int x = 1, y = 1;
       if (x++ || y++) {
              x += 5;
       }
       std::cout << y << std::endl;
       return 0;
}
```

A. 1
B. 2
C. 5
D. 6
E. The correct answer is missing

8a57. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
struct A {
       int m_x;
       A(int x) : m_x(x) {
std::cout << m_x << " "; };
};
struct B : virtual public A {
       B() : A(5) { }
};
struct C : virtual public A {
       C() : A(0) { }
};
struct D : public B, public C {
       D() : A(1) { }
};
int main() {
       A* p = new D();
       return 0;
}
```

A. 5 0 1
B. 0 1

C. 1
D. The program contains compile-time error
E. The correct answer is missing

8a58. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
void f(int& x) {
	x += 3;
	std::cout << x <<
std::endl;
}
int main() {
	f(0);
	return 0;
}
```

A. 0
B. 3
C. The program contains compile-time error
D. The program contains run-time error
E. The correct answer is missing

8a59. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
struct A {
	int mx;
	A(int x) : mx(0) { }
};
int main() {
	A arr[5];
	for (int i = 0; i < 3;
++i) {
		std::cout <<
arr[i].mx << std::endl;
	}
	return 0;
}
```

A. 0 0 0
B. 5 5 5
C. 3 3 3
D. 3 3 3 0 0
E. The correct answer is missing

8a60. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
struct Exc1 {
	void what() { std::cout <<
"Exc1" << std::endl; }
};
struct Exc2 : public Exc1 {
	void what() { std::cout <<
"Exc2" << std::endl; }
};
int main() {
	try {
		throw Exc2();
	} catch (Exc1& e) {
		std::cout << "First
	catch: ";
		e.what();
	} catch (Exc2& e) {
		std::cout << "Second
catch: ";
		e.what();
	} catch(...) {
		std::cout << "Unknown
exception" << std::endl;
	}
	return 0;
}
```

A. First catch Exc1
B. First catch Exc2
C. Second catch Exc2
D. Unknown exception
E. The correct answer is missing

8a61. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
template <int i>
struct A {
	static const int n =
i*A<i-1>::n;
};
template <>
struct A<1> {
	static const int n = 1;
};
int main(){
	std::cout << A<5>::n <<
std::endl;
	return 0;
}
```

A. The program contains compile-time error
B. 5
C. 24
D. 120
E. The correct answer is missing

8a62. Can the overloaded operator of the class be declared virtual?

A. Yes
B. No
C. Only ++ and – operators
D. Only if the class contains virtual destructor
E. The correct answer is missing

8a63. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
#include <typeinfo>
struct A {};
struct B : public A {};
int main() {
	A* p = new B();
	std::cout <<
typeid(p).name() << std::endl;
	return 0;
}
```

*A. Struct A**
*B. Struct B**
C. The program contains compile-time error
D. The program contains run-time error
E. The correct answer is missing

8a64. What design pattern is presented below?

```
#include <iostream>
struct A {
	virtual void f() {
		func();
	}
	virtual void func() = 0;
};
struct B : public A {
	virtual void func() {}
};
```

A. Virtual constructor
B. Template method
C. Strategy
D. The program contains compile-time error
E. The correct answer is missing

8a65. What design pattern is presented below?

```
struct A {
	virtual A* clone() {
return new A(*this); }
};
struct B : public A {
	A* clone() { return new
B(*this); }
};
```

A. Virtual constructor
B. Strategy
C. Template method
D. None
E. The correct answer is missing

8a66. Which of the following class methods is not generated by compiler by default – in case of being not defined by the programmer?

A. Default constructor
B. Copy constructor
C. Assignment operator
D. Destructor
E. The correct answer is missing

8a67. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
void f(int) { std::cout <<
"Integer" << std::endl; }
void f(unsigned short) { std::cout
<< "Unsigned Short" << std::endl;
}
void f(unsigned int) { std::cout
<< "Unsigned Integer" <<
std::endl; }
int main() {
	short c = 5;
	f(c);
	return 0;
}
```

A. Integer
B. Unsigned Short
C. Unsigned Integer
D. The program contains compile-time error
E. The correct answer is missing

8a68. After performing the code below, what will be displayed on the screen?

```
#include <iostream>
#include <algorithm>
#include <functional>
struct A {
	virtual void f() {
std::cout << "A "; }
};
struct B : public A {
	virtual void f() {
std::cout << "B "; }
};
int main() {
	A* a[] = { new A(), new B()
};
	std::for_each(a, a+2,
std::mem_fun(&A::f));
	return 0;
}
```

A. A A
B. A B
C. B A
D. B B
E. *The correct answer is missing*

8a69. What design pattern is presented below?

```
struct AImpl {
	void f() { }
};
class A {
	AImpl* m_impl;
public:
	A() : m_impl(new AImpl()) {
}
	void f() { m_impl->f(); }
};
```

A. Virtual constructor
B. Strategy
C. Template method
D. Bridge
E. The correct answer is missing

8a70. What data-members can be initialized at declaration?

A. Static
B. Static const
C. Static const integral type
D. None
E. The correct answer is missing

8a71. Consider the following code:

```
#include<iostream>
class A
{
public :
         A()
         {
            std::cout <<
"Constructor of A\n";
         };
         ~A()
         {
            std::cout <<
"Destructor of A\n";
         };
};
class B : public A
{
public :
         B()
```

```
        {
            cout << "Constructor
of B\n";
        };
        ~B()
        {
            cout << "Destructor
of B\n";
        };
};
int main()
{
        B* p;
        p = new B();
        delete p;
        return 0;
}
```

What will be the printed output?

A. Constructor of B
Constructor of A
Destructor of A
Destructor of B

B. Constructor of A
Constructor of B
Destructor of B
Destructor of A

C. Constructor of B
Constructor of A
Destructor of B
Destructor of A

D. Constructor of A
Constructor of B
Destructor of A
Destructor of B

E. The sequence of construction and destruction of A and B will be compiler specific

8a72. Consider the sample code given below and answer the question that follows.

```
class Car
     {
     private:
            int Wheels;

     public:
            Car(int wheels = 0)
        : Wheels(wheels)
            {
            }

            int GetWheels()
            {
        return Wheels;
            }
     };
     int main()
     {
            Car c(4);
        cout << "No of wheels:"
<< c.GetWheels();
            return 0;
     }
```

Which of the following lines from the sample code above are examples of data member definition?

A. 4
B. 7
C. 8
D. 14
E. 19

8a73. What will happen when the following code is compiled and executed?

```
#include<iostream>
class my_class
{
private:
       int number;
public:
       my_class()
       {
                     number = 2;
       }
       int& a()
       {
                     return number;
       }
};
int main()
{
       my_class m1, m2;
       m1.a() = 5;
       m2.a() = m1.a();
       std::cout << m2.a();
       return 0;
}
```

A. Compile time errors will be generated because right hand side of expressions cannot be functions
B. The printed output will be 5
C. The printed output will be 2
D. The printed output will be undefined
E. None of the above

8a74. What will be the output of the following code?

```
class A
{
public:
   A() : m_data(0){}
   ~A(){}
   int operator ++()
   {
     m_data ++;
     std::cout << "In first ";
     return m_data;
   }
   int operator ++(int)
   {
     m_data ++;
     std::cout << "In second ";
     return m_data;
   }
private:
   int m_data;
};

int main()
{
  A a;
  std::cout << a++;
```

```
  std::cout << ++a;
  return 0;
}
```

A. *In first 1 In second 2*
B. *In second 1In first 2*
C. *In first 0 In second 2*
D. *In second 0 In first 2*
E. *None of the above*

8a75. What will be the output of the following code?

```
#include<iostream>
class b
{
int i;
public:
void vfoo()
{ std::cout <<"In Base "; }
};
class d : public b
{
int j;
public:
void vfoo()
{
std::cout<<"In Derived ";
}
};
int main()
{
b *p, ob;
d ob2;
p = &ob;
p->vfoo();
p = &ob2;
p->vfoo();
ob2.vfoo();
return 0;
}
```

A. *In Base In Base In Derived*
B. *In Base In Derived In Derived*
C. *In Derived In Derived In Derived*
D. *In Derived In Base In Derived*
E. *In Base In Base In Base*

8a76. Consider the following code:

```
#include<stdio.h>
int main(int argc, char* argv[])
{
        enum Colors
        {
                red,
                blue,
                white = 5,
                yellow,
                green,
                pink
        };
        Colors color = green;
        printf("%d", color);
        return 0;
}
```

What will be the output when the above code is compiled and executed?

A. *4*
B. *8*
C. *16*
D. *7*
E. *The code will have compile time errors*

8a77. Consider the sample code given below and answer the question that follows.

```
class SomeClass
{
int x;
public:
SomeClass (int xx) : x(xx) {}
};
int main()
{
SomeClass x(10);
SomeClass y(x);
       return 0;
}
```

What is wrong with the sample code above?

A. *SomeClass y(x); will generate an error because SomeClass has no copy constructor*
B. *SomeClass y(x); will generate an error because SomeClass has no default constructor*
C. *SomeClass y(x); will generate an error because SomeClass has no public copy constructor*
D. *x(xx) will generate an error because it is illegal to initialize an int with that syntax*
E. *The code will compile without errors*

8a78. Which of the following are NOT valid C++ casts?

A. *dynamic_cast*
B. *reinterpret_cast*
C. *static_cast*
D. *const_cast*
E. *void_cast*

8a79. Consider the following code:

```
class BaseException
{
public:
       virtual void Output()
        {
               cout << "Base
Exception" << endl;
       }
};

class DerivedException
: public BaseException
{
public:
       virtual void Output()
       {
             std::cout << "Derived
Exception" << std::endl;
       }
};
void ExceptionTest()
{
       try {
             throw
DerivedException();
       }
```

```
        catch (BaseException& ex)
{
                ex.Output();
        } catch (...) {
                cout << "Unknown
Exception Thrown!" << endl;
        }
}
```

Invoking Exception Test will result in which output?

A. Base Exception
B. Derived Exception
C. Unknown Exception Thrown
D. No Output will be generated
E. None of the above

8a80. Consider the sample code given below and answer the question that follows.

```
class X {
        int   i;
protected:
       float f;
public:
       char  c;
};
class Y : private X { };
```

Referring to the sample code above, which of the following data members of X are accessible from class Y?

A. c
B. f
C. i
D. f and c
E. None of the above

8a81. Which of the following sets of functions is not qualified as overloaded function?

*A. void fun(int, char *)*
*void fun(char *, int)*
B. void x(int, char)
*int *x(int, char)*
C. int get(int)
int get(int, int)
*D. void F(int *)*
*void F(float *)*
E. All of the above are overloaded functions

8a82. Consider the sample code given below and answer the question that follows.

```
class Grandpa
{
} ;
class Ma : virtual public Grandpa
{
} ;
class Pa : virtual public Grandpa
{
} ;
class Me : public Ma, public Pa,
virtual public Grandpa
{
} ;
```

How many instances of Grandpa will each instance of Me contain?

A. 1
B. 2
C. 3
D. 4
E. None of the above

8a83. What is the output of the following code segment?

```
int n = 9;
int *p;
p = &n;
n++;
cout << *p + 2 << ", " << n;
```

A. 11, 9
B. 9, 10
C. 12, 10
D. 11, 10
E. None of the above

8a84. Consider the sample code given below and answer the question that follows:

```
char** foo;
/* Missing code goes here */
for(int i = 0; i < 200; i++)
{
foo[i] = new char[100];
}
```

Referring to the sample code above, what is the missing line of code?

*A. foo = new *char[200]*
B. foo = new char[200]
*C. foo = new char[200]**
D. foo = new char[200]*
E. foo = new char[][200]

8a85. Consider the sample code given below and answer the question that follows.

```
class A
{
public:
A() {}
~A()
{
cout << "in destructor" << endl;
}
};
int main()
{
A a;
a.~A();
return 0;
}
```

How many times will "in destructor" be output when the above code is compiled and executed?

A. 0
B. 1
C. 2
D. A compile time error will be generated because destructors cannot be called directly
E. None of the above

8a86. Consider the sample code given below and answer the question that follows.

```
class Person
{
   string name;
   int age;
   Person *spouse;
public:
   Person(string sName);
   Person(string sName,
          int nAge);
   Person(const Person& p);
   Copy(Person *p);
   Copy(const Person &p);
   SetSpouse(Person *s);
};
```

Which one of the following are declarations for a copy constructor?

A. Person(string sName)
B. Person(string sName, int nAge)
*C. Copy(Person *p)*
D. Person(const Person &p)
E. Copy(const Person &p)

8a87. Consider the following code.

```
template<class T>
void kill(T *& t)
{
       delete t;
       t = NULL;
}
class my_class
{
};
void test()
{
       my_class*ptr = new
my_class();
       kill(ptr);
       kill(ptr);
}
```

Invoking Test() will cause which of the following?

A. Code will Crash or Throw and Exception
B. Code will Execute, but there will be a memory leak
C. Code will execute properly
D. Code will exhibit undefined behavior
E. None of the above

8a88. Which of the following is not a standard STL header?

A. <array>
B. <deque>
C. <queue>
D. <list>
E. None of the above

8a89. Which of the following member functions can be used to add an element in an std::vector?

A. Add
B. front
C. push
D. push_back
E. None of the above

8a90. Consider the sample code given below and answer the question that follows.

```
class Shape
{
public:
virtual void draw() = 0;
};
class Rectangle: public Shape
{
public:
void draw()
{
// Code to draw rectangle
}
//Some more member functions.....
};
class Circle : public Shape
{
public:
void draw()
{
// Code to draw circle
}
//Some more member functions.....
};
int main()
{
Shape obj;
obj.draw();
return 0;
}
```

What happens if the above program is compiled and executed?

A. Object obj of Shape class will be created
B. A compile time error will be generated because you cannot declare Shape objects
C. A compile time error will be generated because you cannot call draw function of class 'Shape'
D. A compile time error will be generated because the derived class's draw() function cannot override the base class draw() function
E. None of the above

8a91. What is the output of the following C++ program?

```
#include <iostream>
class A
{
public:
    explicit A(int n = 0) : m_n(n)
{ }

    A(const A& a)
        : m_n(a.m_n)
```

```
    {
        ++m_copy_ctor_calls;
    }
public:
    static int m_copy_ctor_calls;

private:
    int m_n;
};

int A::m_copy_ctor_calls = 0;
A f(const A& a) { return a; }
A g(const A a) { return a; }

int main()
{
    A a;
    A b = a, c(a);
    std::cout <<
A::m_copy_ctor_calls;

    b = g(c);
    std::cout <<
A::m_copy_ctor_calls;

    const A& d = f(c);
    std::cout <<
A::m_copy_ctor_calls << std::endl;

    return 0;
}
```

A. 245
B. 134
C. 124
D. Contains compile error
E. None of the above

8a92. What is the output of the following C++ program?

```
#include <iostream>
#include <vector>

class A
{
public:
    A(int n = 0) : m_n(n) { }

public:
    virtual int value() const {
return m_n; }
    virtual ~A() { }

protected:
    int m_n;
};

class B
    : public A
{
public:
    B(int n = 0) : A(n) { }

public:
    virtual int value() const {
return m_n + 1; }
};

int main()
{
    const A a(1);
    const B b(3);
    const A *x[2] = { &a, &b };
    typedef std::vector<A> V;
    V y;
    y.push_back(a);
    y.push_back(b);
    V::const_iterator i =
y.begin();

    std::cout << x[0]->value() <<
x[1]->value()
              << i->value() << (i
+ 1)->value() << std::endl;

    return 0;
}
```

A. 1313
B. 1413
C. 1423
D. Contains compile error
E. None of the above

8a93. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A(int n = 2) : m_i(n) { }

    ~A() { std::cout << m_i; }

protected:
    int m_i;
};

class B
    : public A
{
public:
    B(int n) : m_x(m_i + 1) ,
m_a(n) { }

public:
    ~B()
    {
        std::cout << m_i;
        --m_i;
    }

private:
    A m_x;
    A m_a;
};

int main()
{
    { B b(5); }

    std::cout << std::endl;

    return 0;
}
```

A. 2531
B. 5432
C. 2513
D. Contains compile error
E. None of the above

8a94. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A() : m_i(0) { }

protected:
    int m_i;
};

class B
{
public:
    B() : m_d(0.0) { }

protected:
    double m_d;
};

class C
    : public A
    , public B
{
public:
    C() : m_c('a') { }

private:
    char m_c;
};

int main()
{
    C d;
    A *b1 = &d;
    B *b2 = &d;

    const int a =
(reinterpret_cast<char*>(b1) ==

reinterpret_cast<char*>(&d)) ? 1 :
2;
    const int b = (b2 == &d) ? 3 :
4;
    const int c =
(reinterpret_cast<char*>(b1) ==

reinterpret_cast<char*>(b2)) ? 5 :
6;

    std::cout << a << b << c <<
std::endl;

    return 0;
}
```

A. 246
B. 135
C. 136
D. Contains compile error
E. None of the above

8a95. What is the output of the following C++ program?

```
#include <algorithm>
#include <functional>
#include <iostream>
#include <iterator>
#include <list>

int main()
{
    typedef std::list<int> L;
    L l(5);

    typedef L::const_iterator CI;
    CI cb = l.begin(), ce =
l.end();
    typedef L::iterator I;
    I b = l.begin();

    std::transform(cb, --ce, ++b,

std::bind2nd(std::plus<CI::value_t
ype>(), 1));
    std::copy(l.begin(), l.end(),

std::ostream_iterator<CI::value_ty
pe>(std::cout));
    std::cout << std::endl;

    return 0;
}
```

A. 01234
B. 43210
C. 12345
D. Contains compile error
E. None of the above

8a96. What is the output of the following C++ program?

```
#include <cstddef>
#include <iostream>

class A
{
public:
    A() : m_x(0) { }

public:
    static ptrdiff_t
member_offset(const A &a)
    {
        const char *p =
reinterpret_cast<const char*>(&a);
        const char *q =
reinterpret_cast<const
char*>(&a.m_x);

        return q - p;
    }

private:
    int m_x;
};

class B
    : public A
{
public:
    B() : m_x('a') { }

public:
    static int m_n;

public:
    static ptrdiff_t
member_offset(const B &b)
    {
```

```
        const char *p = 
reinterpret_cast<const char*>(&b);
        const char *q = 
reinterpret_cast<const 
char*>(&b.m_x);

        return q - p;
    }

private:
    char m_x;
};

int B::m_n = 1;

class C
{
public:
    C() : m_x(0) { }
    virtual ~C() { }

public:
    static ptrdiff_t 
member_offset(const C &c)
    {
        const char *p = 
reinterpret_cast<const char*>(&c);
        const char *q = 
reinterpret_cast<const 
char*>(&c.m_x);

        return q - p;
    }

private:
    int m_x;
};

int main()
{
    A a;
    B b;
    C c;
    std::cout << 
((A::member_offset(a) == 0) ? 0 : 
1);
    std::cout << 
((B::member_offset(b) == 0) ? 0 : 
2);
    std::cout << 
((A::member_offset(b) == 0) ? 0 : 
3);
    std::cout << 
((C::member_offset(c) == 0) ? 0 : 
4);
    std::cout << std::endl;

    return 0;
}
```

2. 1234

3. 0204

4. 1230

5. Contains compile error

6. None of the above

8a97. What is the output of the following C++ program?

```
#include <iostream>

template<class T, T t = T()>
class A
{
private:
    template<bool b>
    class B
    {
    public:
        static const int m_n = b ? 
1 : 0;
    };

public:
    static const int m_value = 
B<(t > T())>::m_n - B<(t < 
T())>::m_n;
};

int main()
{
    std::cout << A<int, -
9>::m_value << A<bool, 
true>::m_value
              << A<char>::m_value 
<< std::endl;

    return 0;
}
```

7. -110

8. 101

9. -101

10. Contains compile error

11. None of the above

8a98. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A(int n = 0)
        : m_i(n)
    {
        std::cout << m_i;
        ++m_i;
    }

protected:
    int m_i;
};

class B
    : public A
{
public:
    B(int n = 5) : m_a(new A[2]), 
m_x(++m_i) { std::cout << m_i; }
```

```
    ~B() { delete [] m_a; }

private:
    A m_x;
    A *m_a;
};

int main()
{
    B b;

    std::cout << std::endl;

    return 0;
}
```

12. 02020

13. 20020

14. 02002

15. Contains compile error

16. None of the above

8a99. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    virtual void f(int n) {
std::cout << n << 1; }
    virtual ~A() { }

    void f(int n) const {
std::cout << n; }
};

class B
    : public A
{
public:
    void f(int n) { std::cout <<
(n << 1); }

    void f(int n) const {
std::cout << n + 1; }
};

int main()
{
    const A a;
    B b;
    A &c = b;
    const A *d = &b;

    a.f(2);
    b.f(2);
    c.f(1);
    d->f(1);

    std::cout << std::endl;

    return 0;
}
```

17. 2421

18. 4131

19. 2411

20. Contains compile error

21. None of the above

8a100. What is the output of the following C++ program?

```
#include <algorithm>
#include <iostream>
#include <list>
#include <vector>

class Int
{
public:
    Int(int i = 0) : m_i(i) { }

public:
    bool operator<(const Int& a)
const { return this->m_i < a.m_i;
}

    Int& operator=(const Int &a)
    {
        this->m_i = a.m_i;
        ++m_assignments;
        return *this;
    }

    static int get_assignments() {
return m_assignments; }

private:
    int m_i;
    static int m_assignments;
};

int Int::m_assignments = 0;

int main()
{
    std::list<Int> l;
    l.push_back(Int(3));
    l.push_back(Int(1));
    l.sort();

    std::cout <<
Int::get_assignments();

    std::vector<Int> v;
    v.push_back(Int(2));
    v.push_back(Int());
    std::sort(v.begin(), v.end());

    std::cout <<
Int::get_assignments() <<
std::endl;

    return 0;
}
```

22. 20

23. 00

24. 02

25. Contains compile error

26. None of the above

8a101. What is the output of the following C++ program?

```
#include <algorithm>
#include <iostream>
#include <list>

struct P
{
    bool operator()(const int &n)
const
    {
        return n % 3 == 0;
    }
};

int main()
{
    const int a[] = { 5, 2, 6, 1,
13, 9, 19 };
    const int count = sizeof(a) /
sizeof(a[0]);
    std::list<int> l(a, a+ count);
    std::cout << l.size();
    std::remove_if(l.begin(),
l.end(), P());
    std::cout << l.size() <<
std::endl;

    return 0;
}
```

27. 66

28. 77

29. 44

30. Contains compile error

31. None of the above

8a102. What is the output of the following C++ program?

```
#include <iostream>
#include <stdexcept>

class A
{
public:
    A(int n) : m_n(n) { std::cout
<< m_n; }

    ~A() { std::cout << m_n; }

private:
    int m_n;
};

int f(int n)
{
    if (1 == n) {
        throw
std::logic_error("0");
    }
    A l(n);
    return f(n - 1) * n / (n - 1);
}

int main()
{
    try {
        int r = f(3);
        A a(r);
    }
    catch (const std::exception
&e) {
        std::cout << e.what() <<
std::endl;
    }

    return 0;
}
```

32. 32230

33. 03223

34. 32023

35. Contains compile error

36. None of the above

8a103. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A(int i) : m_i(i) { }

public:
    int operator()(int i = 0)
const { return m_i + i; }

    operator int () const { return
m_i; }

private:
    int m_i;

    friend int g(const A&);
};

int f(char c)
{
    return c;
}

int g(const A& a)
{
    return a.m_i;
}

int main()
{
    A f(2), g(3);
```

```
    std::cout << f(1) << g(f) <<
std::endl;

    return 0;
}
```

37. 53

38. 33

39. 35

40. Contains compile error

41. None of the above

8a104. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    explicit A(int n = 0) : m_n(n)
{ }

public:
    A& operator=(const A& a)
    {
        this->m_n = a.m_n;
        ++m_assignment_calls;
        return *this;
    }

public:
    static int m_assignment_calls;

private:
    int m_n;
};

int A::m_assignment_calls = 0;

A f(const A& a) { return a; }

A g(const A a) { return a; }

int main()
{
    A a(3);
    A b = a;
    std::cout <<
A::m_assignment_calls;

    b = g(a);
    g(b);
    std::cout <<
A::m_assignment_calls;

    const A& c = f(b);
    std::cout <<
A::m_assignment_calls <<
std::endl;

    return 0;
}
```

42. 110

43. 101

44. 011

45. Contains compile error

46. None of the above

8a105. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A(int n = 0) : m_n(n) { }
    A(const A &a) : m_n(a.m_n) {
++m_copy_ctor_calls; }
    ~A() { ++m_dtor_calls; }

private:
    int m_n;

public:
    static int m_copy_ctor_calls;
    static int m_dtor_calls;
};

int A::m_copy_ctor_calls = 0;
int A::m_dtor_calls = 0;

int main()
{
    A *p = 0;
    {
        const A a = 2;
        p = new A[3];
        p[0] = a;
    }
    std::cout <<
A::m_copy_ctor_calls <<
A::m_dtor_calls;
    p[1] = A(1);
    p[2] = 2;
    delete [] p;
    std::cout <<
A::m_copy_ctor_calls <<
A::m_dtor_calls << std::endl;

    return 0;
}
```

47. 0106

48. 6100

49. 0601

50. Contains compile error

51. None of the above

8a106. What is the output of the following C++ program?

```
#include <iostream>
```

```
class B
{
public:
    virtual int shift(int n = 2)
const { return n << 2; }
};

class D
    : public B
{
public:
    int shift(int n = 3) const {
return n << 3; }
};

int main()
{
    const D d;
    const B *b = &d;

    std::cout << b->shift() <<
std::endl;

    return 0;
}
```

52. 16

53. 61

54. 11

55. Contains compile error

56. None of the above

8a107. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A(int n = 2) : m_n(n) {}

public:
    int get_n() const { return
m_n; }
    void set_n(int n) { m_n = n;
}

private:
    int m_n;
};

class B
{
public:
    B(char c = 'a') : m_c(c) {}

public:
    char get_c() const { return
m_c; }
    void set_c(char c) { m_c =
c; }

private:
    char m_c;
};

class C
    : virtual public A
    , public B
{ };

class D
    : virtual public A
    , public B
{ };

class E
    : public C
    , public D
{ };

int main()
{
    E e;
    C &c = e;
    D &d = e;
    std::cout << c.get_c() <<
d.get_n();

    c.set_n(3);
    d.set_c('b');
    std::cout << c.get_c() <<
d.get_n() << std::endl;

    return 0;
}
```

57. 2a3a

58. a2a3

59. a3a2

60. Contains compile error

61. None of the above

8a108. What is the output of the following C++ program?

```
#include <iostream>
#include <set>

struct C
{
    bool operator()(const int
&a, const int &b) const
    {
        return a % 10 < b % 10;
    }
};

int main()
{
    const int a[] = { 4, 2, 7,
11, 12, 14, 17, 2 };
    const int count = sizeof(a)
/ sizeof(a[0]);
```

```
    std::set<int> x(a, a +
count);
    std::cout << x.size();
    std::set<int, C>
y(x.begin(), x.end());
    std::cout << y.size() <<
std::endl;

    return 0;
}
```

62. 47

63. 44

64. 74

65. Contains compile error

66. None of the above

8a109. What is the output of the following C++ program?

```
#include <algorithm>
#include <cassert>
#include <cstddef>
#include <functional>
#include <iostream>
#include <vector>
class A
{
public:
    A() : m_size(sizeof(A)) { }
public:
    virtual void f() const {
std::cout << 1; }
    virtual ~A() { }
public:
    static bool compare(const A
*a, const A *b)
    {
        assert(a != 0);
        assert(b != 0);
        return a->m_size < b-
>m_size;
    }
protected:
    size_t m_size;
};
class B
    : public A
{
public:
    B() : m_b(0) { m_size =
sizeof(B); }
public:
    virtual void f() const {
std::cout << 2; }

private:
    char *m_b;
};
class C
    : public A
{
public:
    C() { m_size = sizeof(C); }
public:
    virtual void f() const {
std::cout << 3; }
public:
    static int *m_c;
};
int *C::m_c = 0;
struct D
{
    void operator()(A *a) const
{ delete a; }
};
int main()
{
    typedef std::vector<A*> V;
    V v;
    v.push_back(new C);
    v.push_back(new B);
    v.push_back(new A);
    std::stable_sort(v.begin(),
v.end(), A::compare);
    std::for_each(v.begin(),
v.end(), std::mem_fun(&A::f));
    std::cout << std::endl;
    D d;
    std::for_each(v.begin(),
v.end(), d);
    return 0;
}
```

67. 123

68. 312

69. 231

70. Contains compile error

71. None of the above

8a110. What is the output of the following C++ program?

```
#include <iostream>

class A
{
public:
    A(int n = 0) : m_i(n) {
std::cout << m_i; }

protected:
    int m_i;
};

class B
    : public A
{
public:
    B(int n) : m_j(n) , m_a(--m_j)
, m_b() { std::cout << m_j; }

private:
    int m_j;
    A m_a;
    A m_b;
```

```
        static A m_c;
    };

    int main()
    {
        B b(2);

        std::cout << std::endl;

        return 0;
    }

    A B::m_c(3);
```

72. 30101

73. 30103

74. 00101

75. Contains compile error

76. None of the above

8a111. After performing the code below, what is the output of the program?

```
#include <iostream>

class Data {
public:
        Data()
        : m(0)
        { std::cout << "Data "; }
        ~Data()
        { std::cout << "~Data "; }
private:
        int m;
};

class Base {
public:
        Base()
        { std::cout << "Base "; }
        ~Base()
        {std::cout << "~Base ";}
private:
        Data m_b;
};

class Der : public Base {
public:
        Der()
        { std::cout << "Der "; }
        ~Der()
        {std::cout << "~Der ";}
private:
        Data m_d;
};

int main()
{
        Base* b = new Der();
        delete b;
        std::cout << std::endl;
        return 0;
}
```

A. Data Base Data Der ~Base ~Data ~Der ~Data
B. Base Data Der Data ~Data ~Base ~Data ~Der
C. Data Base Data Der ~Base ~Data
D. Data Base Data Der ~Data ~Base
E. Base Data Der Data ~Data ~Base

8a112. After performing the code below, what is the output of the program?

```
#include <iostream>

class A {
public:
        A()
        { ++count; }

        A(const A& )
        { ++count; }

        ~A()
        { --count; }
        static unsigned count;
};

unsigned A::count = 0;

int main()
{
        const int N = 100;
        A a[N];
        char* apt = new char[N *
    sizeof(A)];
        for(int i = 0; i < N; ++i) {
                new (&apt[i])
    A(a[i]);
        }
        delete[] apt;
        std::cout << A::count <<
    std::endl;
        return 0;
}
```

A. 0
B. 100
C. 200
D. Compilation error
E. None of the above

8a113. After performing the code below, what is the output of the program?

```
#include <iostream>

class A {
public:
        A() {std::cout << "A()";}
        A(int) {std::cout <<
    "A(int)";}
        A& operator =(int)
    {std::cout << "=";}
```

```
};

class B {
public:
        B() : m2(8)
        {m1 = 5;}
private:
        A m1;
        A m2;
};

int main()
{
        B b;
        std::cout << std::endl;
        return 0;
}
```
A. *A(int)=*
B. *A()A(int)=*
C. *A(int)A()=*
D. *=A(int)*
E. *None of the above*

8a114. After performing the code below, what is the output of the program?
```
#include <iostream>

class A {
        A()
            : m_i(0)
            { std::cout << "Hello
   world" << std::endl; }
        int m_i;
};


int main()
{
        A a;
        return 0;
}
```
A. *Hello world*
B. *Compilation error*
C. *Hello*
D. *World*
E. *All the answers are correct*

8a115. After performing the code below, what is the output of the program?
```
#include <iostream>

int& foo()
{
        static int a = 3;
        return a;
}

int main()
{
        ++++foo();
        std::cout << foo() <<
   std::endl;
        return 0;
}
```
A. *0*
B. *3*
C. *4*
D. *5*
E. *None of the above*

8a116. The given program in order to check if N number that is larger than 2 is simple, divides it on all possible divisors starting 2. If N is not divided into any divisor without reminder, it is considered to be simple. What is the maximum possible divisor for N number, dividing on which it will be possible to determine the N-'s simplicity.
A. *N*
B. *N/2*
C. *sqrt(N)*
D. *sqrt(N)+1*
E. *N/3*

8a117. Which of the following features is not characteristic of scripting languages?
A. *Interpretation*
B. *Dynamic typifiqation*
C. *Strict typifiqation*
D. *Static typifiqation*
E. *Object-orientation*

8a118. The part of alleged program, presented below, finds the maximum value of element that contains integers:
```
max = 0;
for (i=0 .. N)
  if (a[i] > max)
    max = a[i];
```
How much is the complexity of this algorithm?
A. *$\Theta(n) = 2n$*
B. *$\Theta(n) = 2\log(n)$*
C. *$\Theta(n) = \log(n)$*
D. *$\Theta(n) = n^2$*
E. *$\Theta(n) = n$*

8a119. For which of the following data structures "push" and "pop" activities are used?
A. *Array*
B. *List*
C. *Stack*
D. *Matrix*
E. *Cyclic list*

8a120. Which of the following data structures is used for storing the same type of data?
A. *Class*
B. *Record*
C. *Array*

D. Linked list
E. None of the above

8a121. If two strings are identical, strcmp() function returns?
A. -1
B. 1
C. 0
D. Yes
E. No

8a122. Which bitwise operator is suitable for checking whether a particular bit is on or off?
A. && operator
B. & operator
C. || operator
D. !operator
E. None of the above

8a123. What is executed by the following program?

```
w=0;
for(i=0;i<strlen(s);++i) {
        if(s[i]==' ') {
                k=0;
                for(j=i;j<strlen(s);++j) {
                        if(s[j]!=' ') {

a[w][k]=s[j];
                                k++;

a[w][k]='\0';
                                i++;
                        }
                        else break;
                }
        }
        else continue;
        w++;
}
```

77. It finds the letters in a string

78. It finds the words in a string

79. It finds the frequency of letters in a string

80. It finds the frequency of words in a string

81. It does not execute any useful operation

8a124. Which of the following data structures provides equal access time to any member:

82. Array

83. Related list

84. Stack

85. Cyclic list

86. Queue

8a125. How many times will the program below print "Hello"? 8ɯ125

```
#include<stdio.h>
int main()
{
   printf("Hello");
   main();
   return 0;
}
```

A. Infinite times
B. 32767 times
C. 65535 times
D. Stack overflow will occur
E. Compilation error will occur

8a126. How much is the complexity of an algorithm given?

```
int[]numbers = { 35, 47, 16, 12, 
11, 145};
int searched = 11;
int found = -1;
for (int i = 0; i < 6; i++)
{
    if(numbers[i] == searched)
    {
        found = i;
              break;
    }
}
```

A. O(1)
B. O(n)
C. O(log(n))
D. O(sqrt(n))
E. O(exp(n))

8a127. What data structure is given in Structure type example if it operates as shown?

```
----- Program ------------
Structure var;

var.add(24);
var.add(13);
var.add(123);
var.add(118);

print var.getnext();
print var.getnext();
print var.getnext();
```

print var.getnext();

----- Output ------------
118
123
13
24

A. *Hash*
B. *Queue*
C. *Stack*
D. *Combined list*
E. *Associative mass*

b) Problems

8b1.
Develop a program that, given two symbol sequences, finds the length of the longest common subsequence of the given sequences
For example,
<u>S</u>YNOP<u>SYS</u>, <u>S</u>INOP<u>SYS</u> $\rightarrow$ 7

8b2.
Assume A is the known W. Ackermann function:

$$A(0, y) = y + 1;$$

$$A(x, 0) = A(x - 1, 1);$$

$$A(x + 1, y + 1) = A(x, A(x + 1, y)).$$

Redefine A in a way that it is computed modulo 7717.

$$AM(x, y) = A(x, y) \;\; Mod(7717),$$

Restrict the enormous growth of A.
Develop a program that can compute AM(10,10) in several seconds and find the value of AM(10,10).

8b3.
Assume Fib is the Fibonacci function: $Fib(n) = \begin{cases} 1, \text{ if n} = 1 \text{ or n} = 2 \\ Fib(n-1) + Fib(n-2), \text{otherwise.} \end{cases}$

Define the number Q as follows: $Q = \sum_{k=1}^{11} (1 / \mathrm{Fib}(\mathrm{Fib}(k))).$

Calculate the number Q with an accuracy guaranteeing that the sum of the first 36 decimal digits can be computed exactly.

8b4.
Develop an algorithm that for any given pair of natural numbers n ≥ k constructs the set of all the subsets of {1,2,…,n} having cardinality equal to k.

8b5.
Prove (using induction argument) that the following algorithm for exponentiation is correct.
function power (y,s)
comment Return y^z, where $y \in$ R, $z \in$ N
x:=1;
while z > 0 do
if z is odd then x := x * y;
z:= ⌊z/2⌋;
y:=y2;
return(x)

8b6.
Prove (using induction argument) that the following algorithm for the multiplication of natural numbers is correct.
function multiply (y, z)
comment Return y*z, where y,z $\in$ N
x:=0:
while z > 0 do
x := x + y * (z mod 2);
y:=2y; z:=⌊z/2⌋;
return(x)

8b7.
Prove (using induction argument) that the following algorithm for the multiplication of natural numbers is correct.
function multiply(y, z)
comment Return the product y*z.
If z = 0 then return(0) else
return(multiply(2y, ⌊z/2⌋ + y*(z mod 2))

8b8.
Write a program which, given a sequence of integers, finds the length of the longest increasing subsequence.

Input

Input contains length of sequence 0<N<1000, then follows N integers, does not exceed 109 by absolute.

Output

Write one number in the output, length of the longest increasing subsequence.

Example

Input	Output
5	1
7 1 5 2 3	3

8b9.
Assume F is a Fibonacci sequence.

F0 = 1;
F1 = 1;
FN = FN-1 + FN-2   N>1

Write a program to find N-th Fibonacci number modulo 1000007. 0 < N < 109

Example

N = 5   F5 % 1000007 = 8

8b10.
Given a positive integer N.

Write a program to count the number of positive integers, not exceeding N and not divisible none of the given integers: 2,3,5.

Input

Input contains one integer N (1≤N≤2000000000).

Output

Output one number, answer for the given N.

Example

Input	Output
10	2

8b11.
Develop a detailed flowchart for an algorithm computing the greatest common divisor for a pair of positive integers, avoiding deletion operation.

8b12.
Assume a digital image is given by means of $M = \|m_{ij}\|$ $n\times n$ matrix where m_{ij} are non-negative integers.

a. Develop a detailed flowchart for an algorithm that finds the (rounded) coordinates of the centre of gravity of the image. Define needed auxiliary functions.

b. Evaluate the complexity of the developed algorithm.

8b13.
Assume for any integer $m \geq 2$ $P(m)$ is a result of attaching consecutive positive integers represented in m-ary form. For example, the beginning part of $P(3)$ looks as follows:

$$\underbrace{1}_{1}\ \underbrace{2}_{2}\ \underbrace{10}_{3}\ \underbrace{11}_{4}\ \underbrace{12}_{5}\ \underbrace{20}_{6}\ \underbrace{21}_{7}\ \underbrace{22}_{8}\ \underbrace{100}_{9}\ \underbrace{101}_{10}\ 110$$

Develop a detailed flowchart for an algorithm that given $m \geq 2$ and $n \geq 1$ finds the numeral allocated at n-th place in $P(m)$. Define needed auxiliary functions.

8b14.
A sequence is said to be a *polyndrome* if it has the central symmetry. Develop a detailed flowchart for an algorithm that given binary sequence S finds a longest segment of S that is a palindrome. If there are several such segments then it is enough to find one of them and the length of it.

8b15.
Print out all simple numbers not exceeding 1000. Natural number is called simple if it has exactly two dividers.

8b16.
Print out all perfect numbers not exceeding 1000. Natural number is called perfect if it equals the sum of all its dividers. For example, 6 = 1 + 2 + 3.

8b17.
Check if the given n number is symmetric or not (n < 107). The number is symmetric if it is read the same way from the beginning and the end. For example, 7586857.

8b18.
Let $n \geq 2$ be an integer. A *partition* of n is a representation of n as a sum of positive integers without taking their order into account. For example, the partitions of 3 are:

1+1+1; 2+1; 3.

Develop a pseudocode for an algorithm generating the list of all the partitions of the given n.

8b19.
Binomial coefficients $\binom{n}{m}$ are defined as follows: $\binom{n}{m} = \frac{n!}{m!(n-m)!}$
Assume that admissible arithmetical operations are addition, subtraction, multiplication and division. Assuming that multiplication and division operations have the same complexity, and neglecting addition and subtraction operations, do the following.

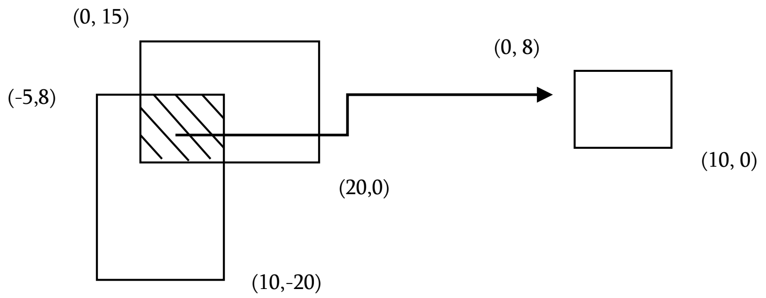
A. Write a pseudocode for trivial, direct calculation of binomial coefficients.
B. Propose a faster algorithm for calculation of binomial coefficients and develop a pseudocode.
C. Evaluate the complexities C1(n,m) and C2(n,m) of the developed codes.
D. Find, how faster your own algorithm's code works with respect to the trivial one for n=100 and m=90.

8b20.
The array coefficients $A_n = [a_n, a_{n-1}, \dots a_1, a_0]$ are associated with a random polynomial $A_n(x) = a_n x^n + a_{n-1} x^{n-1} + \dots + a_1 x + a_0$.

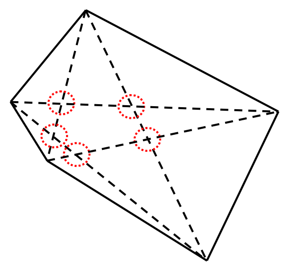
A. Develop an algorithm that given polynomial coefficients arrays $A_n = [a_n, a_{n-1}, \dots a_1, a_0]$ and $B_m = [b_m, b_{m-1}, \dots b_1, b_0]$ calculates the array corresponding the product $A_n(x) * B_m(x)$.
B. Develop a detailed flowchart for that algorithm.

8b21.
The sequence P(n) represents monotonically ordered integer powers and sums of those powers of the number 5. For simplification, the initial segment of P(n) is as follows:
1, 5, 6, 25, 26, 30, 37,125, ...
Develop a detailed flowchart for an algorithm that calculates P(n).

8b22.
Assume given two rectangles – with top left vertex and bottom right vertex coordinates. Implement a program that will detect the crossing of those rectangles.

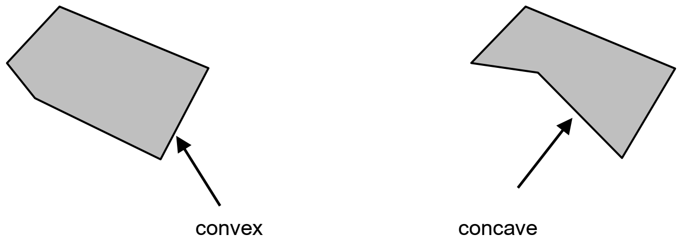


8b23.
Assume the number of vertices of convex polygon is given. No three diagonals of a convex polygon cross in one point. Develop a program that finds the number of crossing points of polygon's diagonals.



The number of crossing points of diagonals is equal to 5.

8b24.
Develop a program that will check whether the given polygon is convex or not. A convex polygon is a simple polygon interior of which is a convex set. The following properties of a simple polygon are all equivalent to convexity:



Every internal angle is less than 180 degrees.
Every line segment between two vertices remains inside or on the boundary of the polygon.
Otherwise, the polygon is called concave.

8b25.
Assume given a MxN rectangle in a unit grid. Develop a program that will find all rectangles within the given rectangle, the vertices of which are the nodes of the grid, and the sides of which are parallel to the coordinate axis.

Example: For the 2x3 rectangle given above, the result is 18 rectangles.

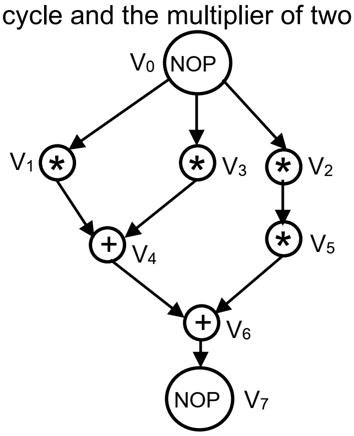
8b26.
Write a program which will set the natural number n and will print the count of n digit numbers which are relatively prime with 30 (the numbers are called relatively prime if they have no common positive divisor other than 1, for example 7 and 30). For example if input number is 1, the output will be 2.

8b27.
Write a program which will set the natural number n and will print the count of last zeros of number n! (n! = n*(n-1)*…*1). For example if input is 5, the 5! = 120 ends by one zero, therefore the output will be 1.

8b28.
Write a program which will set the natural number n and will print the sum of all n digit numbers the digits of which are 1, 2, 3, 4, and 5. For example if input number is 1, the output will be 15.

8b29.
Write a program which will set the natural number n and will print the count of n digit numbers that contain digits 1 and 2. For example if input number is 2, the output will be 34.

8b30.
Given is the following sequencing graph of an algorithm. The edges describe the data-dependencies between the operations such that an operation may only be executed after all its predecessors in the sequencing graph finished execution. The available functional units are an adder and a multiplier. The adder has a latency of one clock cycle and the multiplier of two clock cycles.



Determine the start times of all operations using the as-soon-as-possible scheduling (ASAP) method. What is the latency of this schedule? How many operational units are required for this schedule?

8b31.
Given matrix A(nxm) of rows and all columns of which are sorted, i.e. for all valid i and j A[i][j] < A[i][j+1] and A[i][j] < A[i+1][j]. Write a program which takes matrix A and k elements $c_1,...,c_k$ numbers as an input and for each c_i prints the following "dose c_i exist in matrix A" at the output.

8b32.
Left rotation of a string is to move some leading characters to its tail. Implement a function to rotate a string. For example, if the input string is "abcdefg" and number 2, the rotated result is "cdefgab". Write a program which rotates given string with given length n by given number c (c < n).

8b33.
Write a program which takes given natural numbers M, N, and a_1, …, a_M integral numbers and prints the N minimum numbers. For example, if the given numbers are 5, 2, and {4, 5, 6, 2, 8}, the output must be {2, 4}.

8b34.
There are N doors in a row numbered from 1 to N. Initially all doors are closed. N passes are made by the N doors. In pass 1 all the doors (1,2,3,4....) are toggled starting from the first door. In the second pass every second door is toggled (2,4,6,8,...). In the third pass every third door is toggled (3,6,9...). Similarly N passes are made. Write a program which takes natural numbers N and k and prints the state of door k after N passes, i.e. "Open" or "Close".

8b35.
Suppose that the N-degree ladder (1 <= N <90) is given. A person can make 1 or 2 steps in that ladder upstairs at a time. For the given N, it is required to count the number of all possible different paths that a person can climb from the beginning to the end.

8b36.
N points are given in the plane with dekardian coordinates. It is required to count the perimeter of minimal polygon (bulging membrane), containing those point in 0,1 accuracy. It is guaranteed that the polygon has no 0-area.
For example, 5, (1, 0), (0, 1), (-1, 0), (0, -1), (0, 0);

8b37.
Consider identical N weigh count scales which are different from each other in weight. There is balance scale, through which it is possible to compare weights of two weigh count scales that were chosen. It is required to find the heaviest and the lightest weigh count scales by means of as few weighs as possible.

8b38.
Suppose d (e) is compiled with each e = {u, v} edge of G = (V, E) combinational graph, negative number is also possible: saying skeletal tree length of G = (V, E) graph, the sum of the lengths of the edges, belonging to it is understood. Consider the following problem: such find skeletal tree of the given graph, the length of which is as small as possible.

8b39.
Assume there are 1, 2, .., N objects and the price and volume of each of them is known c (i), v (i). It is necessary to move such objects with a bag, having volume V, the sum of volumes of which does not exceed the amount of volume of a bag and the total price of which is as large as possible.

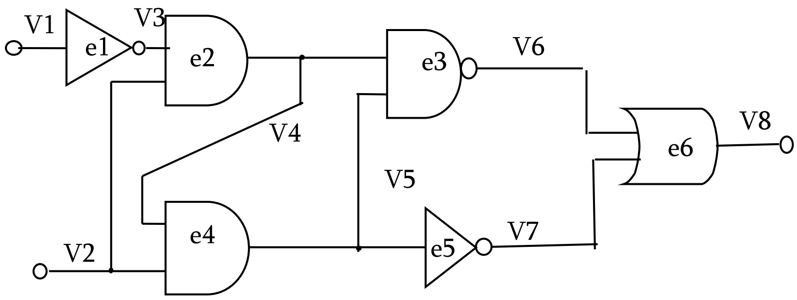
8b40.
During the design, IC area has been divided into N rows and M columns. In the result it has NxM cells where a digital element can be put. Elements have been put in some of columns, which are all the size of one column. Elements are to be connected to power. To connect it to power, along the column (or row) that contains the element, power rail passes; this will connect all elements of that column (or row) to the power. Compile a program which as an input gets the order of elements and returns minimum number of rails, which are sufficient for supply of all circuits. The structure of an integrated circuit is given as NxM 2D matrix. Each element of matrix can contain a circuit in case of which its content is "1", otherwise "0".

8b41.
For IC synchronization it is necessary to construct M efficient chains of signal repetition, each comprised of two buffers. The efficiency of the circuit is measured by the ratio of its frequency and area. The circuit frequency is considered to be equal to the frequency of a buffer, having minimum frequency, area – to the sum of areas of buffers of the circuit. Given even number of 2M logic buffer. For each i-th buffer, its Fi maximum frequency and Ai occupied area are given. Compile a program which for the given input buffer sets {Fi, Ai}, i=1..N, N=2M (1 < M < 50) will display the efficiency of having the minimum efficiency of M circuits and the numbers of buffers in the set.

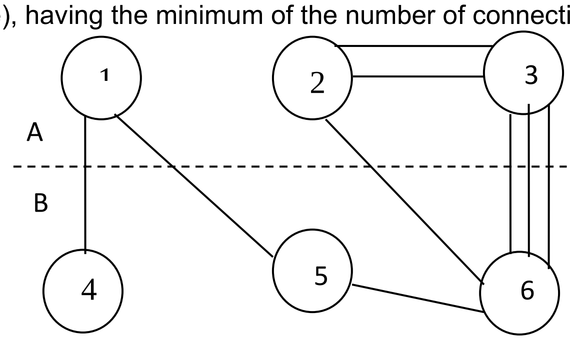
8b42.
During IC design, necessity rose to design a digital circuit from sequentially connected 6 types of cells. The types of cells are different and known but the designer should choose a convenient cell for each type. It has a set, containing N (6 < N < 101) cells, where there are only those 6 types of cells. On the other hand, its goal is to get a circuit that has as high frequency as possible as well as power consumption, smaller than the given value. Both depend on the selection of cells as the general frequency of the circuit is equal to the frequency of cell, having the minimum frequency, and the total power consumption – to the sum of power consumption values of cells.
Compile a program which, getting Fi frequency of each cell of a set of cells and Pi power consumption {Fi, Pi}, i=1..N, as well as the maximum permissible power consumption Pmax will display the numbers, having the maximum frequency and smaller power consumption than Pmax in the set.

8b43.
An integrated circuit has N pins. It is necessary to connect one lamp to each pin. Only a lamp, with smaller resistance than a certain value, is allowed to connect to the pin. Compile a program which for the given N lamps will calculate maximum how many lamps can be connected to the output of an integrated circuit if Ri, i=1..N resistances and RMAXi, i=1..N maximum permissible resistances of IC pins (2<N<1000) of the lamp are known.

8b44.
For the given circuit, compose the adjacency matrix and using the sequential algorithm of partitioning, split into 2 equal parts, having a minimal number of connections between the parts as an optimality criterion. As the first partitioning element, choose the one with the minimum connection.



8b45.
Optimize partitioning of the given graph into parts A and B, with the help of iteration algorithm of transition in pairs (one cycle), having the minimum of the number of connections between parts as an optimality criterion.



8b46.
In a given Physical Synthesis tool there are two routing algorithms R1 and R2 available. These can run in parallel. The routing task is to route N nets. It is known that for each net the amount of time it takes to route by different algorithms will be different. More specifically, if R1 routes net_i it will take Ai time and if R2 is used for routing it will take Bi time. The goal is to distribute net routing between two algorithms to minimize overall

running time. Also, due to computer memory constraints R1 can only route X nets and R2 Y nets. It is guaranteed that X+Y is greater than N. Find the minimum possible routing time of all N nets.

The following input is given: three integers N, X, Y, arrays A and B.

8b47.
Find first and last k digits of n^n (n to the power of n, where n is an integer). The input is two numbers n and k ($1 \le n \le 10^9$, $1 \le k \le 9$). It is guaranteed that k is not more than the number of digits of n^n.

9. NANOELECTRONICS

a) Test questions

9a1. What are the conditions that minimum energy change of contact potential must satisfy to notice one electron-tunneling?
A. Must be smaller than temperature fluctuation
B. Must be larger than quantum fluctuation
C. Must be larger than temperature fluctuation
D. Must be larger than potential barriers
E. B) and C) together

9a2. Why is size quantization phenomena more accessible and easier observed in semiconductors than the metals?
A. Charge carriers' density in semiconductors is small
B. Semiconductors can be doped by mixtures
C. The effective electron mass and energy in semiconductors are small
D. Charge carriers' density in metals is large
E. Charge carriers' mobility in semiconductors is small

9a3. What model is required to be used considering size quantization phenomena in a MOS transistor in deep inverse mode?
A. Rectangular infinite well model
B . Rectangular finite well model
C. Short channel phenomena model
D. Full depletion mode model
E. Triangular well model

9a4. In order to overcome Columb blockade, voltage must be applied which should be
A. Larger than potential barriers value
B. Smaller than potential barriers value
C. Equal to
D. Larger than
E. A) and D) together

9a5. What are the zone marginal bendings in hyper networks (eg. GaAs) conditioned by?
A. Difference of bandgap prohibited zones
B. Difference of output work
C. Interrelation difference towards electron
D. Concentration of mixtures
E. Charged different depletion layers, following each other

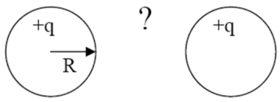
9a6. Mark the wrong answer for carbon nanopipes:
A. Carbon nanopipe is the third subtype of carbon
B. Carbon nanopipe is a molecule, consisting of one of the various atoms of carbon
A. Carbon nanopipe is a pipe with up to 1nm in diameter and several um roller tube
B. Carbon atoms are arranged in the plane of separate layers in carbon nanopipes
C. Carbon atoms are arranged on the vertices of regular six-angles on the walls of carbon nanopipes.

9a7. What is atomic force microscope operation based on?
A. The intermolecular interactions in case of angstrom sized distances between probe and the surface
B. The intermolecular interactions in case of micrometer sized distances between probe and the surface
C. The intermolecular interactions in case of several dozen nanometers sized distances between probe and the surface
D. The registration of the tunnel current between probe and the surface
E. The optical interactions between the probe and surface

b) Problems

9b1.

It is known that colloidal solutions (sols), for example, quantum dots, can agglomerate, forming composite complexes, consisting of 2 or more particles. One reason for this phenomenon is the excess surface energy and the power of molecular attraction, forcing other small particles to unite. To prevent agglomeration, it is possible to report the charge of the same name sign to nanoparticles, which will lead to their repulsion. How can nanoparticles be charged in a colloidal solution ? What could be the minimum and maximum charge of nanoparticles? Suppose, for example, each of the forming sols of silicon nanocrystals (Si), having a spherical shape with a radius R = 1 nm, and a positive charge q, equal in magnitude to twice the electron charge was reported. Will these particles form agglomerates in a collision in a colloidal solution in benzene at room temperature? Will the result change if benzene is replaced with water? Does the probability of agglomeration depend on size of the nanoparticle, their concentration, the temperature of the solution?



Charged colloidal nanoparticles

9b2.

At present, many types of light sources are known. However, few know that the work of any of them is impossible without the use of nanotechnology. Moreover, the more informed a person is using nanotechnology to create a light source, the more sophisticated, versatile and reliable they become.

Historically, the first light source for humans was the fire. Sitting in a cave near the fire, the old man indifferently followed how under the influence of ascending air currents, nanoparticles ash and soot, smoke generators, moved into aerosol state and evaporated back.

1) Calculate the upward air flow *V* speed, which is necessary for translation of spherical nanoparticles of carbon with a diameter of 100 nm into aerosol state, if μ (coefficient of internal friction of particles) is equal to 0.72, outhezia force F (which determines the particle sedimentation) 0.4 N, the resistance coefficient of particles equal to 10^7, particle density is taken as 1.17 g/cm^3.
   Note: for calculation use $v = (2\mu F/\rho cS)^{1/2}$, *where S = area of* cross-section of the particle.

The next generation light sources were incandescent lamps. The work of such light sources is based on a tungsten (wolfram) filament that glows because of warm-up from passing of electric current through it. The lifetime of the lamp is small. However, it was found that the addition of halogens into a lamp (especially iodine) significantly prolongs the lifetime of the light source (the so-called halogen lamps). Special research has shown that the lifetime of the lamp in this case is due to the chemical transport reactions involving formed intermediate compounds nanoclusters of tungsten and halogen.

2) One of such nanoclusters has composition W_6I_{12} and is characterized by an ionic structure. Experimentally it is stated that under the action of silver nitrate, only 1/3 of the total amount of iodine can be precipitated of the nanoclusters. Suggest a nanocluster structure. Note that the cation in the nanocluster has high-symmetric structure.

The main drawback of incandescent lamps - the enormous loss of energy in the form of useless heat dissipation. As an alternative to incandescent lamps mercury (Hg) lamps can be seen, in which the sources of light radiation are the mercury atoms, excited by a glow electric discharge. The main disadvantage of such lamps - the complexity of their utilization.

3) Suggest a reasonable means of utilizing mercury lamps by means of nanotechnology. Note that the proposed method should be simple, economically viable and exclude any risk for the environment.

The most advanced light sources (LED lamps) are based on the luminescence of quantum dots. Their main peculiarity is that, by varying the size of nanoparticles of luminescent material, radiation with different energies and, consequently, with different wavelengths can be obtained.

4) What color will light LED lamp based on quantum dots of cadmium selenide radius of 3 nm? For calculation use $(E_g)^2 = (E_0)^2 + [2\times(h/2\pi)^2\times E_0\times(\pi/r)^2] / m$, where E_g – gap width for a quantum quantum dot, E_0 - the band gap for the bulk sample, r - radius of the nanocrystal (m), m - electron effective mass. For CdSe $E_0 = 2.88\times10^{-19}$ J, m = 1.09×10^{-31} kg.

9b3.

In a nanoworld there is everything - even machines that can transport molecules, clusters and other nanogoods or simply ride without business. Imagine a nano-vehicle, in which the roles of front and rear pairs of wheels do the same nanotube, closed on both sides (Fig. 1).

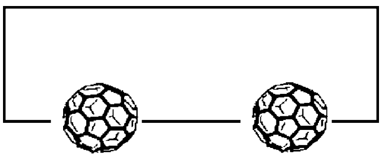


Fig.1. Nano-vehicle on nano-wheels

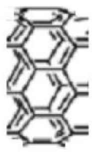


Fig.2. Section of a wheel (N = 8)

The wheels of such a vehicle are not perfect cylinders. They are composed of hexagons with a side of 0.14 nm, and the cross section is not a circle, but correct N-gon (Fig. 2).

When moving, the truck will keep on hopping, spending energy mgh on each jump, where m - mass of the truck, h - the height of the jump, which depends on the number of hexagons in a section of the wheel – N.

The mass of nano-truck for large N can be described by: $m(N) = m_1 + m_2N + m_3N^2$, where m_1 = 10 000 a.m.u. (atomic mass unit), m_2 = 700 a.m.u., m_3 = 25 a.m.u.

1) Explain the type of dependence m(N) .
2) Determine the dependence of the energy E required for one step, from N .
3) Determine the value of N, for which the energy wastes in one step are minimal, and calculate these costs.

Consider that for small angles, the approximate expressions for trigonometric functions can be used: $\sin(x) \approx x$, $\cos(x) \approx 1 - x^2/2$.

9b4.

A quantum dot is a semiconductor nanocrystal, in which the movement of charges is limited to three dimensions in space. In a bulk semiconductor material there exists valence band and conductivity band, separated from one another by band gap. If the electron energy increases, it passes into the conductivity band and a hole appears in valence band. In a quantum dot instead of bands, there are discrete levels, and the band gap (Eg) in this case is the difference of higher energy filled and lowest unoccupied electronic levels.

1) Qualitatively sketch the energy band diagram for the bulk semiconductor and the quantum dot. In both figures, mark the band gap.
2) What is a hole?
   It was found that wavelength of luminescence and band gap are related for quantum dots:
   $(E_g)^2 = (E_0)^2 + [2\times(h/2\pi)^2\times E_0\times(\pi/r)^2] / m$, where E_g – gap width for a quantum dot, E_0 - the band gap for the bulk sample, r - radius of the nanocrystal (m), m - effective mass of electron. For cadmium selenide $E_0 = 2.88\times10^{-19}$ J, $m = 1.09\times10^{-31}$ kg.
3) What is the luminescence?
4) Calculate what is the wavelength of the luminescence (assuming that it corresponds to the band gap) for a crystal with 1 cm radius, 1 nm equal to.
5) What is the minimum size of the quantum dot that corresponds to the luminescence in the visible range? Find the required data.

One way of obtaining nanoparticles of cadmium selenide is the interaction of cadmium oleate $Cd(C_{17}H_{33}COO)_2$ and trioctilephosphinselenide $SeP(C_8H_{17})_3$ in the environment of diphenyl ether $(C_6H_5)_2O$. The reaction is carried out by heating up to 200°C for 5 minutes in an argon atmosphere, then cooled to room temperature. The obtained quantum dots of cadmium selenide are precipitated with acetone.

6) Write the reaction equation of obtaining quantum dots as per the above written method.
7) Why such specific conditions (argon atmosphere, reagents, solvents) are needed for the reaction? Maybe it is easier to pour hot water solutions of salts of cadmium and appropriate selenide?
8) Where quantum dots, based on cadmium selenide, can be (or are already) applied?

9b5.

Once, two young friend-nanotechnologists asked, at first glance, a simple question: how does the de Broglie wave frequency ω of free particle depend on wave vector k? They decided to get the right formula, but each of them acted in his own way.

The first one thought this way. Write the well-known formula of connection (cyclic) frequency with the period: $\omega = \frac{2\pi}{T}$. Express the period through the wavelength and speed: $T = \frac{\lambda}{\upsilon}$. In the result, this is obtained:

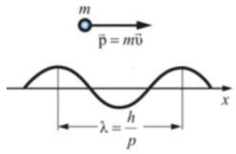
$$\omega = \frac{2\pi}{T} = \frac{2\pi\upsilon}{\lambda} \quad (1)$$

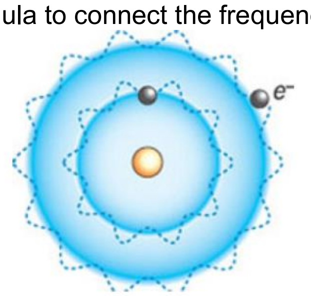
Then apply the de Broglie relation for the pulse and wavelength: $\lambda = \frac{h}{p}$. Substitute it in (1), after which consider $h = 2\pi\hbar$, and multiply the numerator and denominator by mass of the particle m. Then apply the definition of pulse $\vec{p} = m\vec{v}$ and connection pulse by wave vector $\vec{p} = \hbar\vec{k}$. The chain of equalities is obtained:

$$\omega = \frac{2\pi}{T} = \frac{2\pi\upsilon}{\lambda} = \frac{2\pi\upsilon p}{h} = \frac{p\upsilon}{\hbar} = \frac{pm\upsilon}{\hbar m} = \frac{\hbar^2 k^2}{\hbar m} = \frac{\hbar k^2}{m}$$ (2) that is the desired dependence.

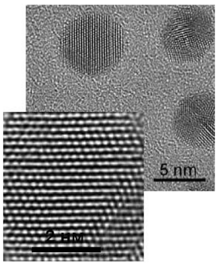
The second one argued differently. Energy and frequency are related by ratio $E = \hbar\omega$.

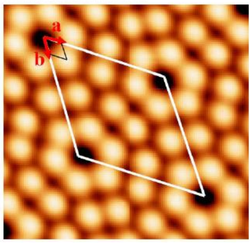
In case of a free particle the energy is $E=\frac{mv^2}{2}$, and the pulse equals to $\vec{p}=m\vec{v}$. From the last two equalities $E=\frac{p^2}{2m}$. Considering that $\vec{p}=\hbar\vec{k}$, there is: $\hbar\omega=E=\frac{\hbar^2k^2}{2m}$.Hence the answer follow $\omega=\frac{\hbar k^2}{2m}$ (3)
To the surprise of the friends, their results (2) and (3) differ twice. Why? Find a mistake in the reasoning (or errors if there are several), and bring the correct formula to connect the frequency and wave vector.





9b6.





To date, it is well known that in a microcosm (or rather, on the atomic scale length) the laws of classical physics do not work, and quantum mechanics comes to replace them. Because of Heisenberg's uncertainty relation, the exact location or boundary of any object in space is impossible to determine. It makes no sense to talk about the exact location of an electron in an atom, as well as the boundary of the atom. Of course, it is possible to talk about orbital and electron density, but the density is, actually the probability amplitude to detect the electron in the vicinity of a point in the elementary act of measurement, rather than a continuous distribution of charge density. Why on many images of micro- and nanostructures obtained by using different types of microscopes (AFM, TEM, AFM, STM), the atoms look like balls or "clusters"? What a circumstance common for different types of microscopy, allows creating images illustrated in the figure?

9b7.

In the years of 1825-1827 George Simon Ohm discovered his famous law which connects the power of the current flowing through the conductor and the voltage applied to the ends of the conductor, through a factor - the conductivity (or resistance). This dependence is observed with sufficiently high accuracy for bulk conductors.
Recently, however, physicist-researchers with the help of a tunneling microscope were able to measure I-V characteristics of the contact of the tungsten(wolfram) wire with a diameter of 1 nm with a gold substrate. Experimental data is shown in the table.

Table with experimental data

U, mV	I, mkA	U, mV	I, mkA	U, mV	I, mkA
7.5	0.37	276	14.95	455.6	33.76
22.7	0.83	293	16.15	470.7	35.5
45.4	1.74	300.6	16.79	480.2	36.97
68	2.66	310	17.34	493.4	38.35
92.7	3.58	323.3	17.98	502.8	39.08
111.5	4.59	330.8	18.62	514.2	40.28
149.3	6.33	342.2	20	523.6	41.93
160.7	7.25	351.6	21.56	533.1	43.58
173.9	7.89	361.1	22.29	542.5	45.32
192.8	8.81	374.3	23.67	550.1	46.97
200.4	9.45	385.6	25.23	557.7	48.53
207.9	9.91	397	26.61	567.1	50.28
225	11.2	412.1	27.8	576.6	51.74
243.9	12.48	421.6	29.45	584.1	53.3
260.9	13.76	431	30.92	593.6	55.14
266.5	14.31	442.3	32.39	601.1	56.88

1. Why gold or tungsten wires are most commonly used?

2. What effect was observed by physicists? What is the difference between current-voltage characteristics of a tungsten wire of circular section of 1 mm diameter, 1 micron, 10 nm and 1 nm and a unit length (plot all these curves on a graph and explain).
3. Plot the conductivity of the applied voltage according to point 3. Constant G_0 is usually applied to the effect. What is this constant called? What is its dimension and value in the SI system? And for what is this value currently used?

9b8.

Porous silicon is an aggregate of nanocrystals and pores with sizes ranging from units to hundreds of nanometers. This material is currently subject to many research laboratories around the world because of its unique structural, optical, electronic and biological properties. Porous silicon is classified in accordance with the International Union of Pure and Applied Chemistry which determines the type of porous material depending on the size of pores.

Table. Classification of porous silicon according to the size of its porous.

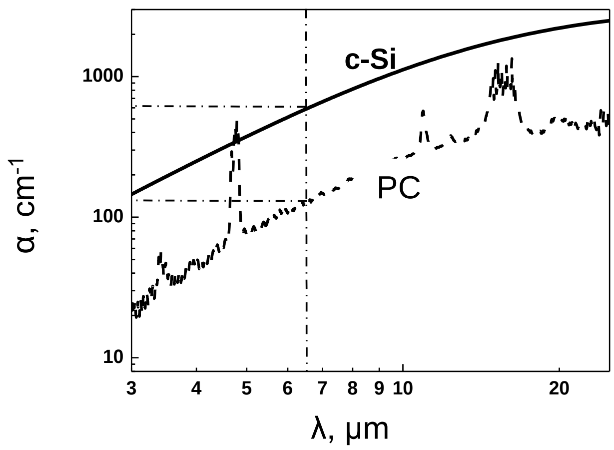
Porous silicon type	Porous size
Microporous (Nanoporous)	*≤2 nm*
Mesoporous	*2-50 nm*
Macroporous	*>50 nm*

The existence of equilibrium free charge carriers in mesoporous silicon nanocrystals (meso-PC) was recently proved. It was found that in addition to the bands of local surface oscillations in the spectra of IR transmission of films of meso-PC, absorption of infrared radiation due to the presence of free charge carriers (FCC) is observed.

1) How can the decrease in the concentration of free charge carriers (FCC) in mesoporous silicon nanocrystals compared with bulk silicon be explained?
2) the figure shows the absorption coefficient α of crystalline silicon (c-Si) and meso-PC on the wavelength λ of infrared radiation. Dependencies α (λ) were determined on the basis of measured transmission spectra according to the relation

$$\alpha(\lambda) \approx -h^{-1}\, ln\left[T(\lambda)\right], \qquad (1)$$

where *h* – thickness of meso-PC, T (λ) - transmission (depending on T (λ) are obtained experimentally).



A dependence of the absorption coefficient of c-Si and meso-PC on the wavelength of infrared radiation.

Note that the transmission spectrum of crystalline silicon was removed under the same conditions as for the porous silicon. Specific resistance of crystalline silicon, the dependence of α (λ) of which is shown in the figure, coincides with the specific resistance of the substrate with a-Si, on which the film of meso-PC was grown.

Assuming scattering times of holes in silicon nanocrystals with characteristic sizes, far from the conditions of the quantum size effect, are close to the values for the substrate c-Si. And also, the nature of the absorption for samples of meso-PS corresponds to the classical Drude model, determine the concentration of FCC in the meso-PC, using the normalization of the spectrum of crystalline silicon with a known concentration of charge carriers equal to 10^{20} cm^{-3}.

The following expression is used to calculate FCC concentration:

$$\alpha(\nu) = N_{CH3} \quad \frac{e^2 n\lambda^2}{4\pi^2 c^3 \varepsilon_0 m^* \tau}, \tag{2}$$

where N_{FCC} – FCC concentration, n – refractive index of the sample ($n_{c\text{-}Si}$ = 3.4, $n_{meso\text{-}PC}$ = 1.7), τ - scattering time of quasi-pulse of holes (consider $\tau_{c\text{-}Si}=\tau_{meso\text{-}PC}$), take value $A = 4\pi^2 c^3 \varepsilon_0 m^* / e^2$ equal to *const* (here m^*- effective mass (for free holes in c-Si $m^* = m_p^* = 0.37 m_0$, $m_0 = 9.1 \cdot 10^{-31}$ kg; $\varepsilon_0 = 8.85 \cdot 10^{-12}$ Ф/m, $e = 1.6 \cdot 10^{-19}$ *Кл*). The porosity of the film of meso-PC is considered equal to 60 %.

3) How will the concentration of FCC change during thermal oxidation of mesoporous silicon and why?
4) Is there FCC in microporous silicon?

9b9.

One of the main microscopic methods used in nanoworld research is atomic-force microscopy. The design of the scanning head of such a device is shown in the figure. The scanning element of microscope (probe) is silicon cantilever. The image quality and accuracy of the measured values depends on the correct setting of the microscope. Typical cantilevers have the form of a rectangular beam of length L = 200 um, thickness t = 0.5 um and width w = 40 um, Young's modulus of silicon E=2* 1010Pa.

Before starting the work, the experimenter sets up a laser system for detecting the bending of the cantilever. In this case the laser beam must be set on the edge of the beam - just above the spot where the needle is located. In a free state cantilever is located horizontally, and during the scan, force on the part of the sample affects and it bends. Bending is fixed by laser system: a laser beam reflects from the beam and falls on the four-section photo diode. While the cantilever is in a free state, the beam hits the very center of the photodiode, when the cantilever is bent, the beam is displaced (signal deviation or Deflection) and this shift is proportional to the bending of the cantilever. Beam displacement as per photodiode in turn is converted into the height, and the methods of conversion may be different.

1. Estimate the value of relative error of measurements (in%), which occurs in the signal Deflection, if the laser beam is substantially removed from the edge of the cantilever (located in the middle of the beam or even farther).
2. What causes this error on the topographical image (signal height)?
3. Is this error essential? In the study of what objects, this effect must be stronger?
4. For what geometric parameters of cantilever the error will be minimizedd?

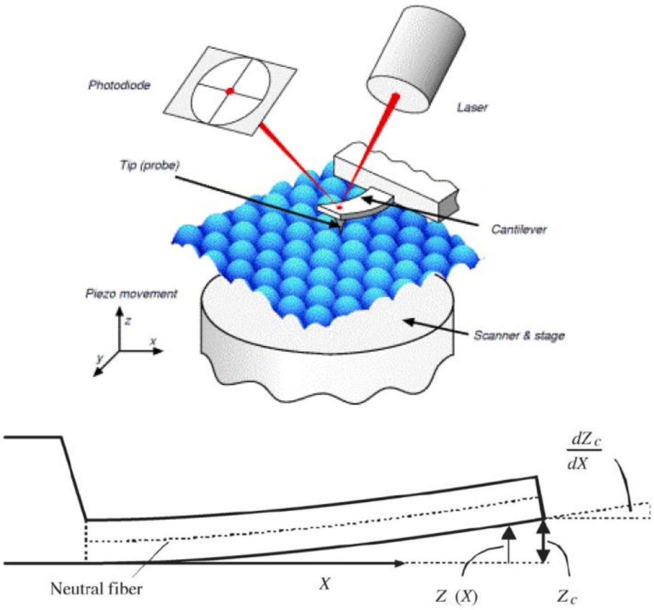


Figure. Schematic diagram of the scanning head of an atomic-force microscope.

9b10.

Among the number of chemical synthesis methods (and not only) it is required to convert water or water solutions into an aerosol - a suspension of tiny drops in a gaseous environment. Consider the following method of obtaining water "nano-drop": parallel stream of water with velocity V crashes from vertical streams, which strikes perpendicular to the solid surface and breaks into small drops of different diameters.

Estimate the speed of the stream of water V, required to obtain a drop size of about 100 nm, 10 nm (the surface tension of water = 0.07 H / m). Can the stream be heard?

9b11.
Using a simple infinite barrier approximation, calculate the “effective bandgap” of a 100Å GaAs/AlAs quantum well.

9b12.
Using a quasi-classical approximation, estimate the number of energy levels of cubic quantum dot made of GaAs if L_x=L_y=L_z=100Å, and V_0=0.2ev.

9b13.
Estimate the energy values of the first two quantum levels for a GaAs quantum well if the well width is 12.5nm.

9b14.
What dimensions must a GaAs quantum well have for the energy differences of lower levels to be of the order of average thermal energy of electrons in a room temperature (T=300K)?

9b15.
Show that in 2D coulomb field, the basic state energy of an electron is four times higher than the energy value of basic state in 3D.
Calculate how many times is the difference between the basic state energy of an electron in 2D coulomb field and the energy value of basic state in 3D.

9b16.
Calculate the density of states and critical density for a GaAs quantum well for unit area in a room temperature.

9b17.
Estimate the electron energy for a GaAs quantum well if the quantum well is in an electrical field for 10^4 V/sm.

9b18.
For basic state of exciton in a GaAs/$Al_{0.3}Ga_{0.7}As$ quantum well with 100Å width and 1mEv semiwidth, calculate the absorption coefficient value for a light with x polarity. Consider only the case of heavy hole. The exciton radius for a quantum well is equal to 2/3 radius of 3D case.

9b19.
Draw the dependence of density of states from energy for bulk crystal, quantum well, quantum wire and quantum dot.

9b20.
A GaAs/$Al_{0.3}Ga_{0.7}As$ multilayer quantum structure with 100Å width has exciton (heavy hole case) absorption peak in case of 1.51eV. 80kV/sm voltage is applied to the well (exciton absorption peak change is 20meV). Calculate radiation beam intensivity ratio in case of the presence and absence of the field, if the exciton line length is 2.5eV, the total length of heterostructure is 1um, and the photon energy is 1.49eV.

9b21.
The height of the potential barrier, total thickness of the space charge layer and barrier capacity of the p-n junction made on InP crystal at the room temperature must be defined. Assume that the concentrations of electrons and holes at the $\mathrm{T} = 300\ \mathrm{K}$ are equal to $\mathrm{p_p} = 5 \cdot 10^{16} \mathrm{cm^{-3}}$and $\mathrm{n_n} = 2 \cdot 10^{16} \mathrm{cm^{-3}}$, their effective masses are equal to $\mathrm{m_n^*} = 0{,}073\mathrm{m_0}$, $\mathrm{m_p^*} = 0{,}4\mathrm{m_0}$ respectively ($\mathrm{m_0} = 9{,}1 \cdot 10^{-31}$ kg is the free electron mass). Also assume that at the $300\ \mathrm{K}$ the bandgap energy of InP is equal to $\mathrm{E_g} = 1{,}34$ eV and dielectric permittivity is equal to $\varepsilon = 12{,}35$.

9b22.
The intrinsic concentration of electrons in the Ge at the 300 K must be defined. Assume that the effective masses of the electrons and holes in Ge are correspondingly equal to $\mathrm{m_n^*} = 0{,}56\mathrm{m_0}$, $\mathrm{m_p^*} = 0{,}37\mathrm{m_0}$ ($\mathrm{m_0} = 9{,}1 \cdot 10^{-31}$ kg is the free electron mass) and bandgap energy is equal to $\mathrm{E_g} = 0{,}66$ eV (T=300 K).

9b23.
Find how many times the equilibrium concentration of electrons in the intrinsic 6H-SiC crystal changes when temperature changes from T_1 =300 K to T_2 =280 K. Assume that temperature dependency of the bandgap energy in 6H-SiC is the following: $\mathrm{E_g(T)} = (3{,}23 - 4 \cdot 10^{-4}\mathrm{T})$ eV.

9b24.

The resistivity of the n-GaN wurtzite modification is $\rho = 0{,}1$ kOhm.cm. Define the equilibrium concentration of electrons n_0. Assume that the mobilities of the carriers at the room temperature are equal to $\mu_n = 1000\,\mathrm{cm^2/Vs}$ and $\mu_p = 200\,\mathrm{cm^2/Vs}$ respectively, and the intrinsic concentration of the carriers is $n_i = 10^{10}\,\mathrm{cm^{-3}}$.

Answers to test questions and solutions of problems

1. DIGITAL INTEGRATED CIRCUITS

a) Test questions

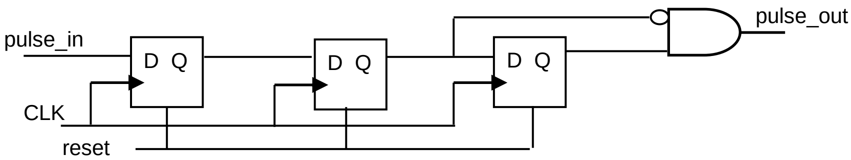
1a1.	B	1a60.	C	1a119.	D	1a178.	C	1a237.	E
1a2.	D	1a61.	B	1a120.	B	1a179.	B	1a238.	B
1a3.	E	1a62.	D	1a121.	D	1a180.	A	1a239.	C
1a4.	B	1a63.	C	1a122.	B	1a181.	A	1a240.	C
1a5.	A	1a64.	D	1a123.	D	1a182.	C	1a241.	A
1a6.	C	1a65.	C	1a124.	A	1a183.	C	1a242.	C
1a7.	B	1a66.	B	1a125.	C	1a184.	B	1a243.	C
1a8.	B	1a67.	B	1a126.	A	1a185.	B	1a244.	C
1a9.	D	1a68.	B	1a127.	D	1a186.	C	1a245.	D
1a10.	A	1a69.	C	1a128.	B	1a187.	A	1a246.	D
1a11.	A	1a70.	D	1a129.	B	1a188.	C	1a247.	C
1a12.	D	1a71.	A	1a130.	D	1a189.	B	1a248.	B
1a13.	C	1a72.	B	1a131.	C	1a190.	A	1a249.	A
1a14.	B	1a73.	D	1a132.	C	1a191.	C	1a250.	A
1a15.	E	1a74.	B	1a133.	B	1a192.	A	1a251.	C
1a16.	A	1a75.	A	1a134.	B	1a193.	D	1a252.	D
1a17.	C	1a76.	A	1a135.	A	1a194.	C	1a253.	C
1a18.	E	1a77.	B	1a136.	C	1a195.	A	1a254.	B
1a19.	A	1a78.	C	1a137.	B	1a196.	D	1a255.	A
1a20.	C	1a79.	B	1a138.	B	1a197.	D	1a256.	A
1a21.	D	1a80.	C	1a139.	A	1a198.	D	1a257.	D
1a22.	B	1a81	B	1a140.	B	1a199.	B	1a258.	B
1a23.	D	1a82.	B	1a141.	A	1a200.	B	1a259.	D
1a24.	E	1a83.	D	1a142.	C	1a201.	B	1a260.	C
1a25.	E	1a84.	C	1a143.	A	1a202.	E	1a261.	C
1a26.	B	1a85.	B	1a144.	C	1a203.	D	1a262.	B
1a27.	B	1a86.	D	1a145.	B	1a204.	C	1a263.	E
1a28.	B	1a87.	D	1a146.	B	1a205.	A	1a264.	A
1a29.	E	1a88.	A	1a147.	C	1a206.	B	1a265.	D
1a30.	C	1a89.	B	1a148.	B	1a207.	A	1a266.	B
1a31.	D	1a90.	D	1a149.	B	1a208.	C	1a267.	B
1a32.	B	1a91.	C	1a150.	C	1a209.	B	1a268.	A
1a33.	D	1a92.	D	1a151.	C	1a210.	A	1a269.	D
1a34.	D	1a93.	B	1a152.	D	1a211.	B	1a270.	D
1a35.	C	1a94.	C	1a153.	A	1a212.	C	1a271.	B
1a36.	D	1a95.	A	1a154.	B	1a213.	E	1a272.	A
1a37.	C	1a96.	B	1a155.	C	1a214.	A	1a273.	E
1a38.	C	1a97.	B	1a156.	A	1a215.	C	1a274.	C
1a39.	A	1a98.	A	1a157.	B	1a216.	B	1a275.	C
1a40.	D	1a99.	C	1a158.	C	1a217.	C	1a276.	B
1a41.	A	1a100.	B	1a159.	D	1a218.	D	1a277.	D
1a42.	D	1a101.	E	1a160.	B	1a219	B	1a278.	B
1a43.	D	1a102.	E	1a161.	B	1a220.	A	1a279.	A
1a44	B	1a103.	B	1a162.	D	1a221.	A	1a280.	E
1a45	E	1a104.	C	1a163.	C	1a222.	B	1a281.	C
1a46	E	1a105.	D	1a164.	B	1a223.	B	1a282.	A
1a47	B	1a106.	B	1a165.	B	1a224.	D	1a283.	B
1a48.	C	1a107.	D	1a166.	C	1a225.	D	1a284.	B
1a49.	B	1a108.	B	1a167.	C	1a226.	C	1a285.	B
1a50.	E	1a109.	D	1a168.	A	1a227.	D	1a286.	A
1a51.	A	1a110.	A	1a169.	C	1a228.	A	1a287.	C
1a52.	C	1a111.	A	1a170.	C	1a229.	B	1a288.	C
1a53.	C	1a112.	D	1a171.	D	1a230.	D		
1a54.	E	1a113.	A	1a172.	C	1a231.	C		
1a55.	B	1a114.	B	1a173.	B	1a232.	D		
1a56.	B	1a115.	C	1a174.	B	1a233.	C		
1a57.	D	1a116.	A	1a175.	A	1a234.	C		
1a58.	C	1a117.	B	1a176.	E	1a235.	A		
1a59.	C	1a118.	A	1a177.	D	1a236.	A		

b) Problems

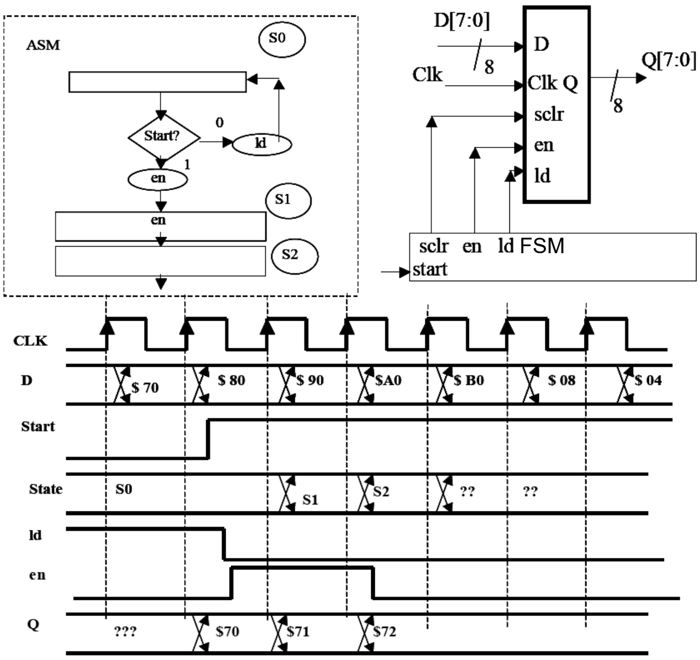
1b1.

$t_{suX}=t_{bf}+t_{nor}+t_{su}-t_{clkbf}=2+7+4-3=11$ ns
$t_{hdX}=t_{clkbf}+t_{hd}-t_{bf}-t_{nor}=3+5-2-7=-1$ ns
$t_L=t_{clkbf}+t_{CQ}+t_{or}=3+6+8=17$ ns
$t_{cycle}=t_{CQ}+t_{nor}+t_{su}=6+7+4=17$ ns

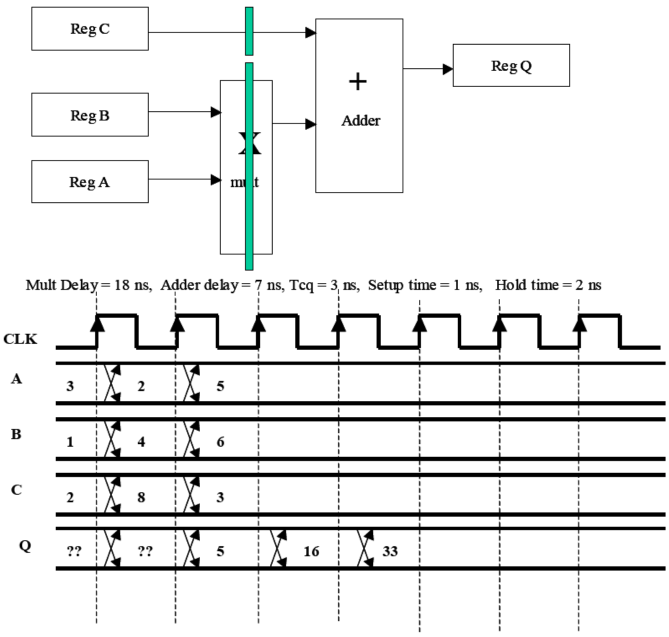
1b2.



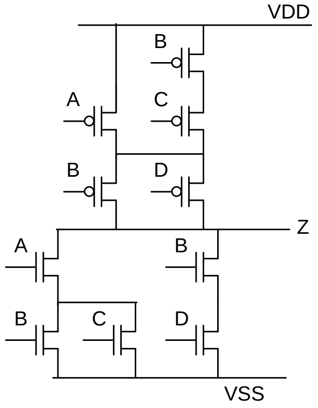
1b3.



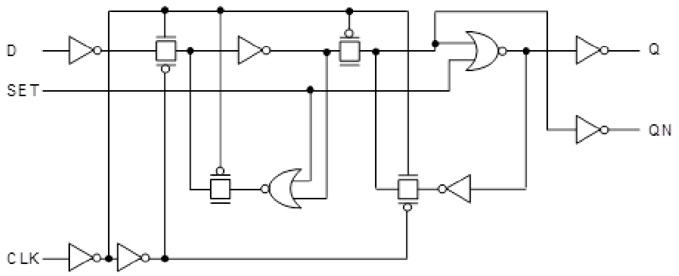
1b4.



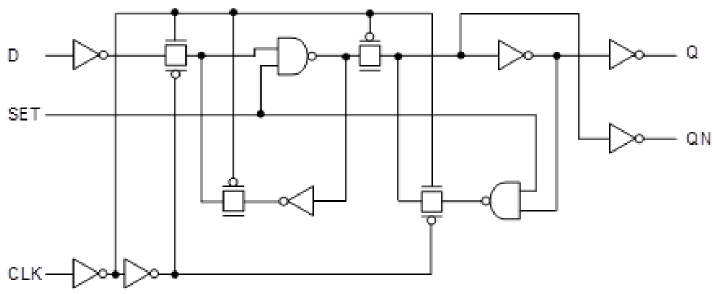
1b5.



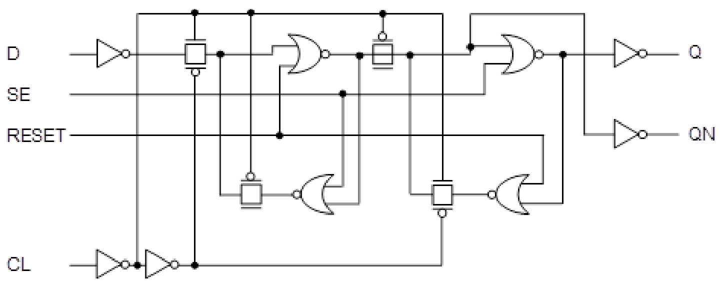
1b6.
D Flip Flop with High Active Set, v.1



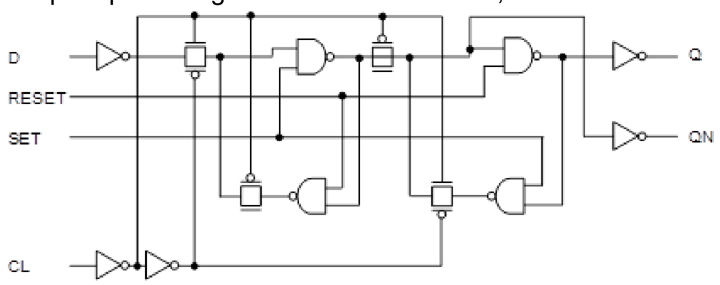
D Flip Flop with High Active Set, v.2



1b7.
D Flip Flop with High Active Set and Reset, v.1



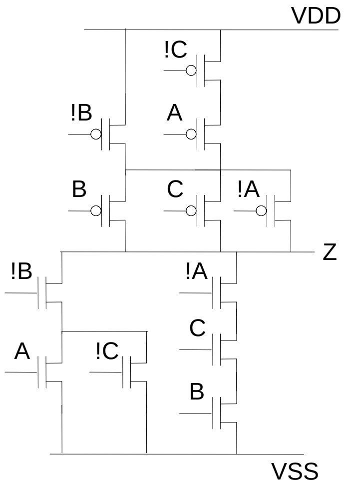
D Flip Flop with High Active Set and Reset, v.2



1b8.

A	B	C	Z	!Z
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Z=A&B+!C&B+!A&!B&C=!(!B(A+!C)+!A&B&C)



1b9.

$$V_{SP}=\frac{\sqrt{\frac{\beta_n}{\beta_p}}\cdot V_{THN}+\left(VDD-V_{THP}\right)}{1+\sqrt{\frac{\beta_n}{\beta_p}}}\ ,\ \beta=kp\frac{W}{L}$$

$$V_{SP}=\frac{\sqrt{\frac{kpn}{kpp}\frac{\frac{W_n}{L_n}}{\frac{W_p}{L_p}}}\cdot V_{THN}+\left(VDD-V_{THP}\right)}{1+\sqrt{\frac{kpn}{kpp}\frac{\frac{W_n}{L_n}}{\frac{W_p}{L_p}}}}=\frac{\sqrt{\frac{kpn}{kpp}}\cdot\sqrt{\frac{W_n}{W_p}}\cdot V_{THN}+\left(VDD-V_{THP}\right)}{1+\sqrt{\frac{kpn}{kpp}}\cdot\sqrt{\frac{W_n}{W_p}}}=$$

$$=\frac{\sqrt{\frac{kpn}{kpp}}\cdot\sqrt{\frac{W_n}{W_p}}\cdot 0.6+\left(5-0.8\right)}{1+\sqrt{\frac{kpn}{kpp}}\cdot\sqrt{\frac{W_n}{W_p}}}\approx\frac{\sqrt{\frac{1}{3}}\cdot 0.6\cdot\sqrt{\frac{W_n}{W_p}}+4.8}{1+\sqrt{\frac{1}{3}}\cdot\sqrt{\frac{W_n}{W_p}}}\approx\frac{4.8}{1+\sqrt{\frac{1}{3}}\cdot\sqrt{\frac{W_n}{W_p}}}$$

1. W_n=3 um

$$V_{SP3}=\frac{4.8}{1+\sqrt{\frac{1}{3}}\cdot\sqrt{\frac{3}{10}}}=3.64\text{ V}$$

2. W_n=12 um

$$V_{SP12}=\frac{4.8}{1+\sqrt{\frac{1}{3}}\cdot\sqrt{\frac{12}{10}}}=3.93\text{ V}$$

$$V_{SP12}<V_{SP3}$$

$$\frac{W_p}{W_n}=\frac{10}{12}\qquad\qquad \frac{W_p}{W_n}=\frac{10}{3}$$

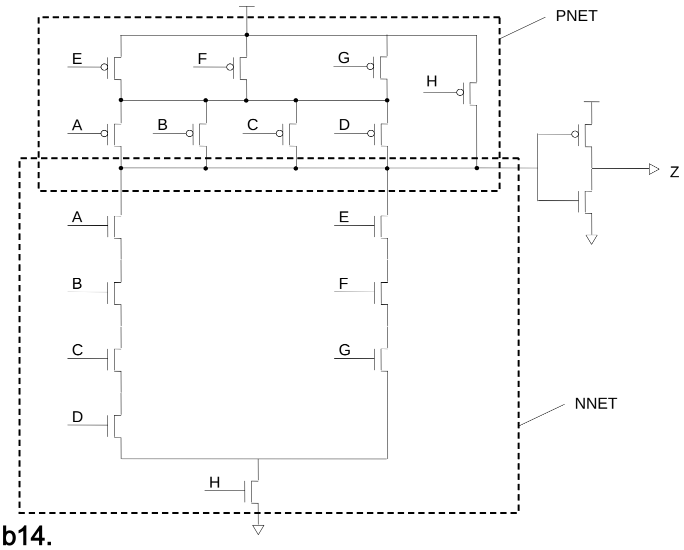
Therefore, the inverter corresponds to the left curve for which W_n=12 um.

1b10.
For both circuits the best case delay is the delay from input C to output Y.
For the shown NAND cell the delay from A input to Y output is smaller than from B input. Therefore, the best case delay of the 2nd circuit is smaller.

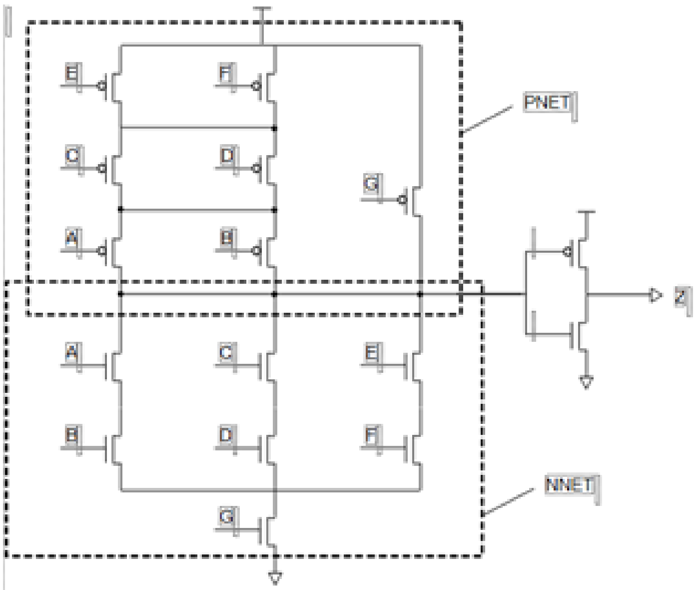
1b11.
The frequency of the ring oscillator is defined by $f = \dfrac{1}{(t_{PHL1}+t_{PLH1})+(t_{PHL2}+t_{PLH2})+\ldots+(t_{PHLn}+t_{PLHn})}$,
where t_{PHLi} and t_{PLHi} are the delays of i-th inverter's output and fall accordingly.
The number of inverters in a ring oscillator must be odd, so the 1st and the 2nd circuits are not included in the ring oscillator (in operation, logic "1" is given to set input and the output NAND cell operates as an inverter).
The delay from "a" input to the output of the used NAND cell is smaller than the delay from "b" input to the output, so the 4th ring oscillator is the fastest.

1b12.
a. In order to get the signal from I12 in Q and QN, it is necessary to have the correct logic state in I22 and I23 feedback until CK fall transition. To say it otherwise, it is necessary to keep CK constant until the signal "passes" I3-I17-I23-I22 path. The signal level in I22 and I23 cells' outputs must be either 0.9 VDD or 0.1 VDD (VDD is supply voltage).
Thus, CK mustn't switch at max(t_{PHL}I3+t_{PLH}I17, t_{PLH}I3+t_{PHL}I17)+max(t_{rise}I23+t_{fall}I22,t_{fall}I23+t_{rise}I22)=1650 ps.
b. As explained in item a., in this case D also must remain constant at max(t_{PHL}I1+t_{PLH}I11, t_{PLH}I1+t_{PHL}I11)+max(t_{rise}I13+t_{fall}I12, t_{fall}I13+t_{rise}I12)- t_{PLH}I12=1250 ps.

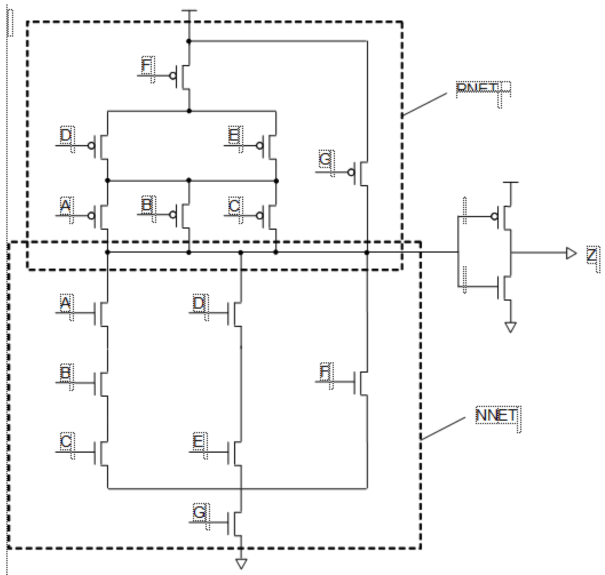
1b13.



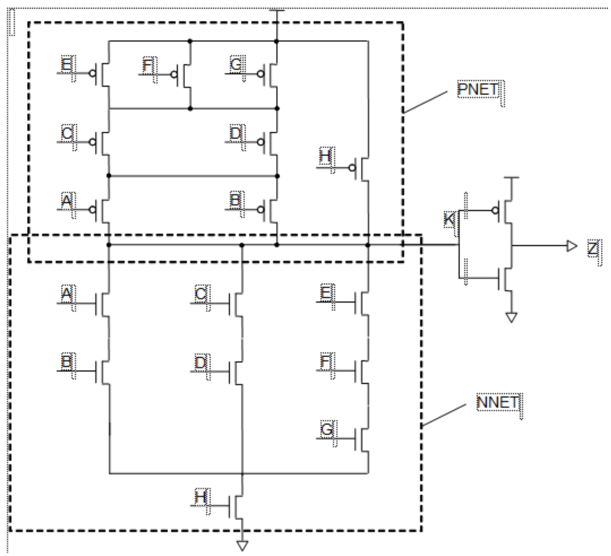
1b14.



1b15.



1b16.



P and N parts of the given circuit do not have common Euler path. For P net, Euler path is the following: H, E, F, G, C, A, B, D. For N net - H, B, A, C, D, E, F, G.

1b17.

The total charge of C_s and C_{BL} before M1 is on.

$$Q = C_s V_s + C_{BL} VDD/2$$

After M1 is on, the voltages across C_s and C_{BL} are equalized to V_{BL}.

$$V_{BL}(C_S+C_{BL})=C_S V_S+C_{BL}VDD/2$$

When reading "1", $V_s=V_{DD}-V_t=1.2-0.3=0.9V$

$$V_{BL} = \frac{C_s V_s + C_{BL} VDD/2}{C_s + C_{BL}} = (0.9Cs+0.6*10Cs)/(Cs+10Cs)=6.9/11=0.63V$$

When reading "0", $V_s=0$

$$V_{BL}=0.6*10Cs/11Cs=0.55V$$

1b18.

$R=2V_{DD}\cdot L/W\cdot k\ (V_{DD}-V_t)^2$; $R_1=2\cdot 2.5\cdot 0.25/4\cdot 115\cdot 4=0.68$ kOhm

$R_2=2\cdot 2.5\cdot 0.25/0.5\cdot 30\cdot 2.1^2=19$ kOhm

a) $V_{OH}=V_{DD}=2.5V$, $V_{OL}=R_1/(R_1+R_2)=0.68/(0.68+19)\cdot 2.5=0.87$ mV

b) 1. V_{in}=Low, $I_n=0$, $P_{diss}=0$,
   2. V_{in}=High=2.5V, $I_n=I_p=(W/L)_p\cdot k_p(V_{DD}-|V_{tp}|)^2/2=133.2\ \mu A$. $P_{static}=V_{DD}\cdot I_p=2.5*133.2=333\mu W$.

c) $t_{pLH}=0.7R_pC_L=0.7*19*1=13.3$ ns; $t_{pHL}=0.7R_nC_L=0.7*0.68*1=0.476$ ns

1b19.

a) Y=!(CD(A+B))

NMOS $(W/L)_A=(W/L)_B=(W/L)_C/2=(W/L)_D/2$; $(W/L)_C=(W/L)_D=4*3=12$; $(W/L)_A=(W/L)_B=6$
PMOS $(W/L)_A=(W/L)_B=2(W/L)_C=2(W/L)_D$; $(W/L)_C=(W/L)_D=8/3$; $(W/L)_A=(W/L)_B=16/3$

b) tpHL: ABCD=1010 -> 1011 or 1010 -> 0111; transistor discharges the caps in all nodes of the pull-down network, before transition all caps are charged. If D were on before transition then D's drain node cap would be discharged, so tpHL would be less.
tpLH: ABCD=1111 -> 0011; before transition all caps are charged, AB path discharges these caps.

1b20.

$$P(Y=1)=(1-P(A=1)P(C=1)P(D=1))\ (1-P(B=1)P(C=1)P(D=1))=$$
$$=(1-0.5*0.3*0.8)(1-0.2*0.3*0.8)=0.88*0.952=0.83776$$
$$P(Y=0)=1-P(Y=1)=1-0.83776=0.16224$$
$$P_{0\text{-}1}=P_{1\text{-}0}=P(Y=0)*P(Y=1)=0.1359181824=0.136$$
$$\alpha_{sw}=P_{0\text{-}1}$$
$$P_{sw}=\alpha_{sw}\,VDD^2F_{clk}C_{out}=0.136*2.5^2*250*10^6*30*10^{-15}=0.659*10^{-5}W=6.59\mu W$$

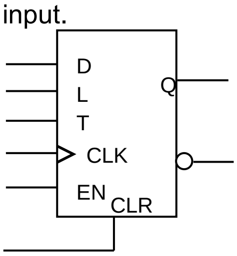
1b21.

<u>Verilog Description</u>

```
module counter_rev(clk,ce,clr,load,d,up,q,tc);
input clk, ce, clr,load,up;
input[7:0] d;
output tc;
reg tc;
output[7:0] q;
reg[7:0] q;
always @(posedge clk or posedge clr)
       begin
       if(clr==1) q<=8'b0;
       else if(load) q<=d;
              else if (ce==0)
                     q<=q;
              else if (up==1)
                     q<=q+1;
              else q<=q-1;
       end
always @(q or up)
       begin if((q==8'd255)&&(up==1))
       tc=1;
              else if((q==8'b0)&&(up==0))
              tc=1;
       else  tc=0; end

endmodule
```

<u>Constructing a counter circuit diagram based on T Flip-Flop</u>

To construct a circuit diagram use T flip-flops with asynchronous reset, synchronous loading and enable input.



T- toggling enable input
L – load enable
D – data input
CCLK– clock input
EN - clock enable input
CLR – asynchronous reset

Truth table of FF:

CLR	EN	L	D	T	CLK	Q	Mode
1	x	x	x	x	x	0	Reset
0	x	1	0	x	↑	0	Syn. „0" writing
0	x	1	1	x	↑	1	Syn. „0" writing
0	0	0	x	x	x	Q_{last}	Hold
0	1	0	x	0	↑	Q_{last}	Hold
0	1	0	x	0	x	Q_{last}	Hold
0	1	0	x	1	↑	$\sim Q_{last}$	Switching

Definition of reversive counter's excitation function

Present_state				Input	Next_state				Excitation Function			
q3	q2	q1	q0	up	q3	q2	q1	q0	t3	t2	t1	t0
0	0	0	0	0	1	1	1	1	1	1	1	1
				1	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1
				1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	0	0	1	0	0	1	1
				1	0	0	1	1	0	0	0	1
0	0	1	1	0	0	0	1	0	0	0	0	1
				1	0	1	0	0	0	1	1	1
0	1	0	0	0	0	0	1	1	0	1	1	1
				1	0	1	0	1	0	0	0	1
0	1	0	1	0	0	1	0	0	0	0	0	1
				1	0	1	1	0	0	0	1	1
0	1	1	0	0	0	1	0	1	0	0	1	1
				1	0	1	1	1	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0	0	1
				1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
				1	1	0	0	1	0	0	0	1
1	0	0	1	0	1	0	0	0	0	0	0	1
				1	1	0	1	0	0	0	1	1
1	0	1	0	0	1	0	0	1	0	0	1	1
				1	1	0	1	1	0	0	0	1
1	0	1	1	0	1	0	1	0	0	0	0	1
				1	1	1	0	0	0	1	1	1
1	1	0	0	0	1	0	1	1	0	1	1	1
				1	1	1	0	1	0	0	0	1
1	1	0	1	0	1	1	0	0	0	0	0	1
				1	1	1	1	0	0	0	1	1
1	1	1	0	0	1	1	0	1	0	0	1	1
				1	1	1	1	1	0	0	0	1
1	1	1	1	0	1	1	1	0	0	0	0	1
				1	0	0	0	0	1	1	1	1

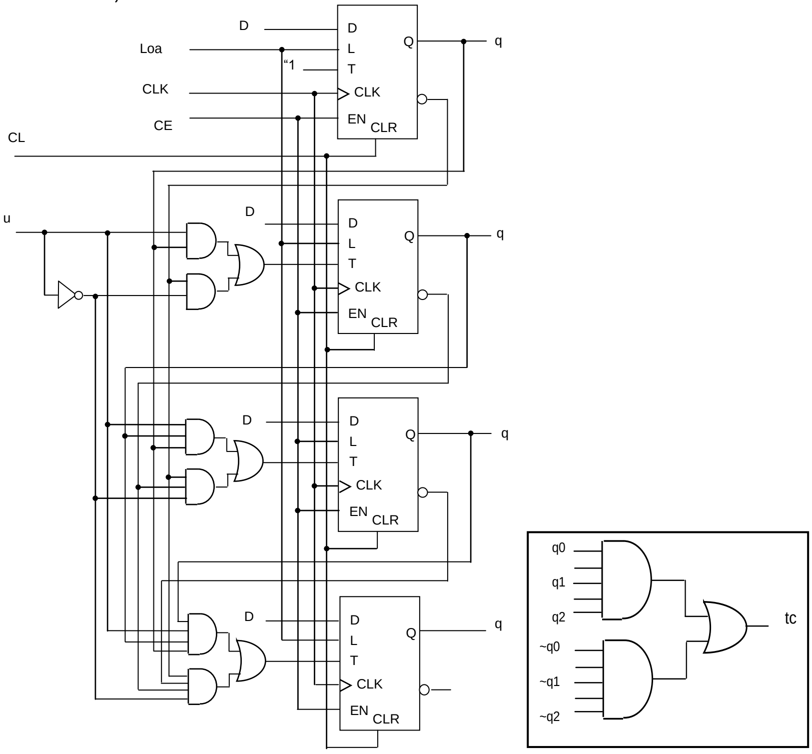
$t0 = 1$; $t1 = q0 \cdot up + \sim q0 \cdot \sim up$;

$t2 = q0 \cdot q1 \cdot up + \sim q0 \cdot \sim q1 \cdot \sim up$;

$t3 = q0 \cdot q1 \cdot q2 \cdot up + \sim q0 \cdot \sim q1 \cdot \sim q2 \cdot \sim up$;

$tc = q0 \cdot q1 \cdot q2 \cdot q3 \cdot up + \sim q0 \cdot \sim q1 \cdot \sim q2 \cdot \sim q3 \cdot \sim up$;

Based on the obtained results, construct the counter circuit.



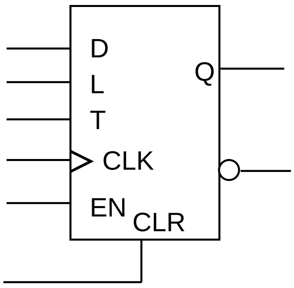
1b22.

Verilog Description

```
module counter_dec(clk,ce,reset,load,d,q,tc);
input clk, ce, reset,load;
input[3:0] d;
output tc;
reg tc;
output[3:0] q;
reg[3:0] q;
always @(posedge clk)
begin
if(reset==1) q<=4'b0;
else if(load) begin if (d>= 4'd10) q<=4'b0;
else q<=d; end
else if ((ce==1)&&(q==4'd9))  q <= 4'b0;
else if(ce==1)  q<=q+1;
else q<=q;
end
always @(q)
if(q==4'd9) tc=1;
else  tc=0;
endmodule
```

Constructing a counter circuit diagram based on T Flip-Flop

To construct a circuit diagram use T flip-flops with asynchronous reset, synchronous loading and enable input.



T- toggling enable input
L – load enable
D – data input
CLK– clock input
EN - clock enable input
CLR – synchronous reset

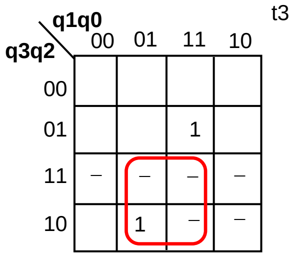
Truth table of FF:

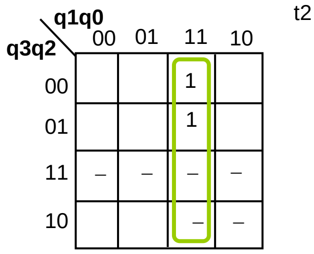
CLR	EN	L	D	T	CLK	Q	Mode
1	x	x	x	x	↑	0	Reset
1	x	1	0	x	↑	0	Syn. „0” writing
1	x	1	1	x	↑	1	Syn. „0” writing
1	0	0	x	x	x	Q_{last}	Hold
1	1	0	x	0	↑	Q_{last}	Hold
1	1	0	x	0	x	Q_{last}	Hold
1	1	0	x	1	↑	$\sim Q_{last}$	Switching

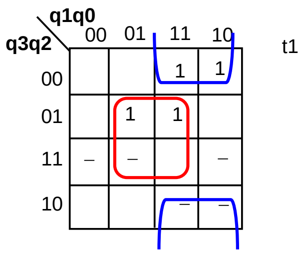
Definition of binary-coded decimal counter's excitation function:

q3	q2	q1	q0	t3	t2	t1	t0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	1	1	1
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	1
0	1	1	0	0	0	0	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1
1	0	0	1	1	0	0	1

Exitation Function's Minimization using Karnaugh Maps



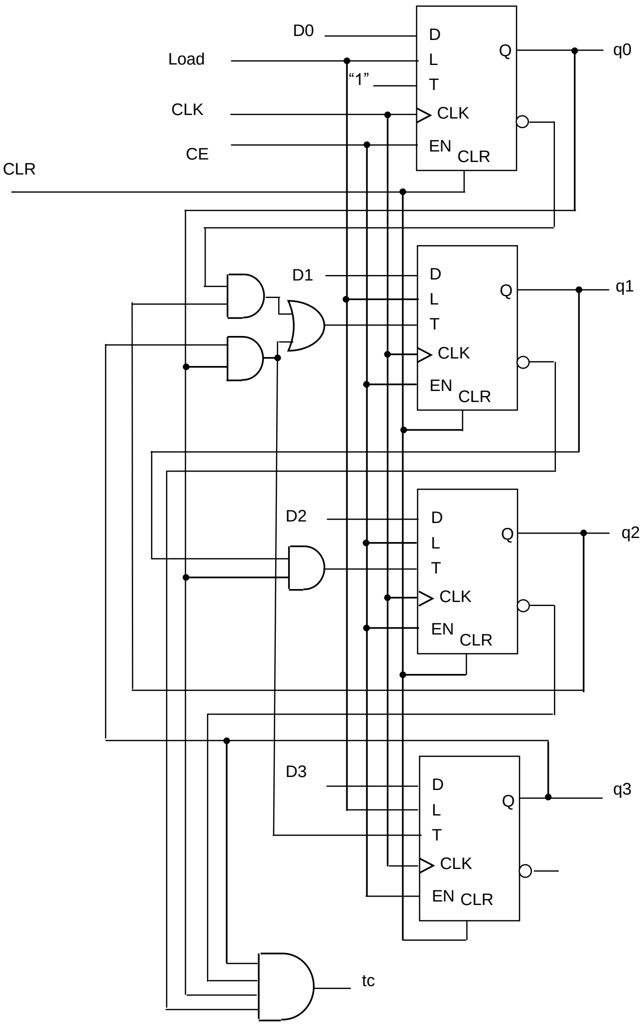




$t0 = 1$
$t1 = q0 \cdot q3 + \sim q0 \cdot q2$
$t2 = q0 \cdot q1$
$t3 = q0 \cdot q3$

$t0 = 1$
$t1 = q0 \cdot q3 + \sim q0 \cdot q3$
$t2 = q0 \cdot q1$
$t3 = q0 \cdot q3$

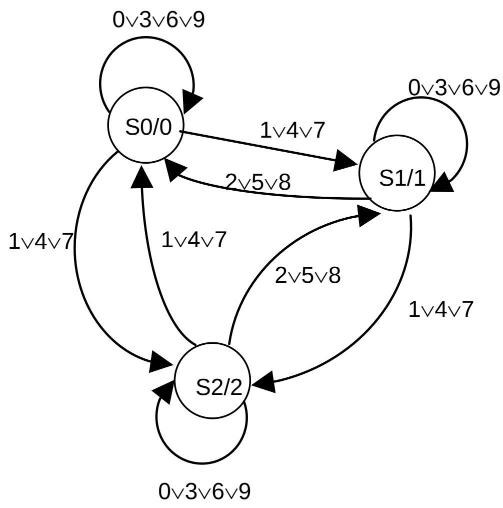
Circuit diagram is constructed based on the obtained results.



1b23.

Creation of State Transition Graph of FSM

The digits of entering decimal number are given on the entries of FSM sequentially.The remainder of division of a decimal number by 3 is equal to the remainder of division of the sum of decimal digits of this number by 3.



FSM is given by means of the following five sets: A = { X, Y, S, δ , λ}, where:
X = {X1, X2 . . . XM} – set of input symbols;
Y = {Y1, Y2 . . . YN} – set of output symbols;
S = {S0, S1 . . . SK-1} – set of internal states of FSM;
δ – next state (transition) function,
λ - output function.

The considered FSM has 3 states S = {S0,S1,S2}, where, S0 – the remainder equal to 0,S1 – the remainder equal to 1,S2 – the remainder equal to 2.
X = {0,1,2,3,4,5,6,7,8,9}
Y = {0,1,2}, S = {S0,S1,S2}

Verilog Description of FSM

```
module fsm_remainder(in,clk,reset,out);
input[3:0] in;
input clk, reset;
output[1:0] out;
reg [1:0] out;
reg[1:0] state, next_state;
parameter S0=2'b00, S1=2'b01, S2=2'b10;

      always @(posedge clk or negedge reset)
             if(!reset) state <= S0;
             else state<=next_state;

      always @(in or state)
             begin
             case(state)
               S0: case(in)
                  4'd0,4'd3,4'd6,4'd9: next_state=S0;
                  4'd1, 4'd4, 4'd7:    next_state=S1;
                  4'd2, 4'd5, 4'd8:    next_state=S2;
                  default: next_state=S0;
                  endcase
               S1: case(in)
                  4'd0,4'd3,4'd6,4'd9:  next_state=S1;
                  4'd1, 4'd4, 4'd7:     next_state=S2;
                  4'd2, 4'd5, 4'd8:     next_state=S0;
                  default: next_state=S0;
               endcase
               S2: case(in)
                  4'd0,4'd3,4'd6,4'd9: next_state=S2;
                  4'd1, 4'd4, 4'd7:     next_state=S0;
                  4'd2, 4'd5, 4'd8:     next_state=S1;
                  default: next_state=S0;
               endcase
               default: next_state=S0;
             endcase
             end

      always @(state)
             if(state==S0) out=2'b00;
             else if (state==S1) out = 2'b01;
             else if (state ==S2) out = 2'b10;
             else out=2'bxx;
endmodule
```

Synthesis of FSM Using JK Flip-Flops

1. Definition of input and output signals
To code decimal digits n = ⌈log$_2$10⌉ = 4 input variables are required, as x3, x2, x1, x0.
Binary-coded decimal digits: Y = {0, 1, 2}.

Decimal digit	x3 x2 x1 x0
"0"	0 0 0 0
"1"	0 0 0 1
"2"	0 0 1 0
"3"	0 0 1 1
"4"	0 1 0 0
"5"	0 1 0 1
"6"	0 1 1 0
"7"	0 1 1 1
"8"	1 0 0 0
"9"	1 0 0 1

To code output signals two variables are required, as y1, y0.

Output	y1 y0
"0"	0 0
"1"	0 1
"2"	1 0

So, FSM has 4 inputs and 2 outputs.
2. State assignment
The number of required state variables k is defined as follows:
3 □ k □ log$_2$3. Accept k=2.
S0 – 00
S1 – 01
S2 – 10
Unused state – 00 (solution of minimal-value)

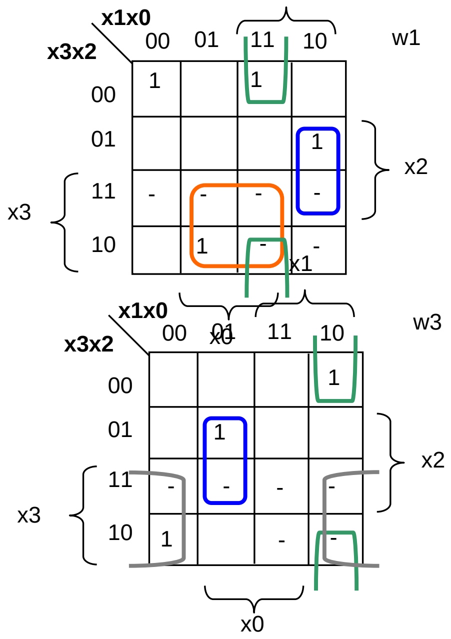
Definition of excitation function

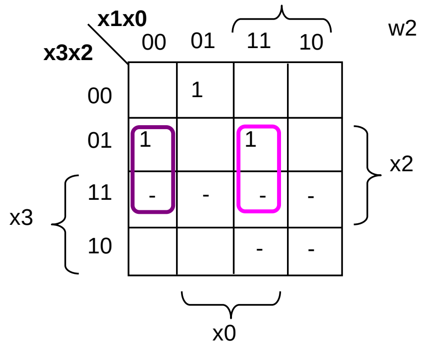
Transition	J K
0 - 0	0 x
0 - 1	1 x
1 - 0	x 1
1 - 1	x 0

State and output table

Present_state	Output	Input	Next_State	Excitation Functions
q1 q0	y1 y0	X	q1 q0	j1 k1 j0 k0
0 0	0 0	0v3v6í9	0 0	0 - 0 -
		1í4í7	0 1	0 - 1 -
		2□5□8	1 0	1 - 0 -
0 1	0 1	0v3v6v9	0 1	0 - - 0
		1v4v7	1 0	1 - - 1
		2v5v8	0 0	0 - - 1
1 0	1 0	0v3v6v9	1 0	- 0 0 -
		1v4v7	0 0	- 1 0 -
		2v5v8	0 1	- 1 1 -

Excitation functions depend on 6 variables: q1,q2,x0,x1,x2,x3.
To simplify the process of designing w1, w2, w3 extra variables are inserted:
0v3v6v9 - w1;
1v4v7 - w2;
2v5v8 - w3;
Karnaugh maps for w1,w2,w3.





w1 = ~x3·~x2·~x1·~x0 + ~x2·x1·x0 + x2·x1·~x0 + x3·x0
w2 = ~x3·~x2·~x1·x0 + x2·~x1·~x0 +x2·x1·x0
w3 = x3·~x0 + x2·~x1·x0 + ~x2·x1·x0

Definition of j1,k1,j2,k2 excitation functions as function of w1,w2,w3,q1,q0.
j1=w1f1 +w2f2+w3f3; k1=w1g1+w2g2+w3g3
j0=w1p1+w2p2+w3p3, k0=w1t1+w2t2+w3t3, where f1…f3,g1,…g3, p1…p3, t1... t3 depend on q1,q2 variables.

As follows from the above table, f1 and g1 are equal to 0.

Maps for definition f2,g2,p2,t2
(factors for w2)

j1

q1 \ q0	0	1
0	0	1
1	-	-

f2 = q2

k1

q1 \ q0	0	1
0	-	-
1	1	-

g2=1

J0

q1 \ q0	0	1
0	1	-
1	0	-

p2=1

K0

q1 \ q0	0	1
0	-	1
1	-	-

t2=1

Maps for definition f3,g3,p3,t3
(factors for w3)

J1

q1 \ q0	0	1
0	1	0
1	-	-

f3=~q2

k1

q1 \ q0	0	1
0	-	-
1	1	-

g3=1

J0

q1 \ q0	0	1
0	0	-
1	1	-

p3=q1

K0

q1 \ q0	0	1
0	-	1
1	-	-

t3=1

So,
j1=w2q2 + w3~q2;
k1 = w2 + w3;
j0=w2~q1+ w3q1;
k0=w2 + w3;

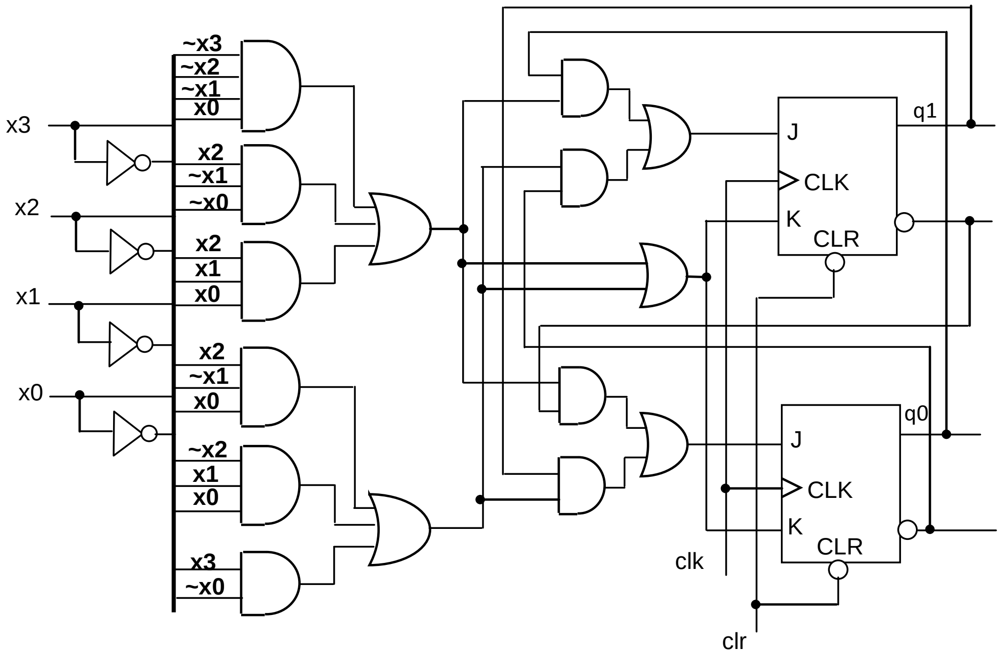
Maps for defining y1, y0

q1 \ q0	0	1
0	0	0
1	1	-

q1 \ q0	0	1
0	0	1
1	0	-

y1=q1; y0=q0;

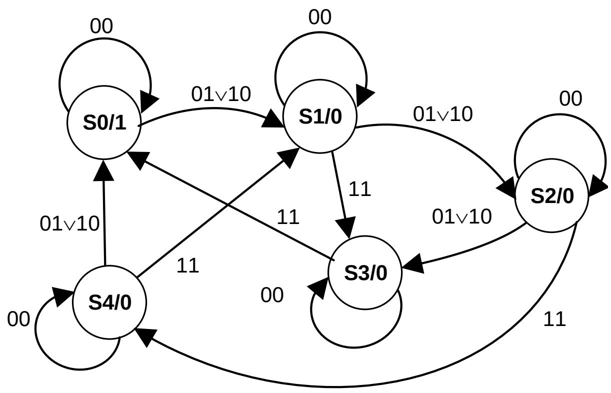
FSM circuit diagram



1b24.

<u>Creation of State Transition Graph of FSM</u>

FSM is given by means of the following five sets: A = { X, Y, S, δ , λ}, where X = {X1, X2 . . . XM} – set of input symbols;
Y = {Y1, Y2 . . . YN} – set of output symbols;
S = {S0, S1 . . . SK-1} – set of internal states of FSM;
δ – next state (transition) function,
λ - output function
X={00,01,10,11}
Y={0,1}



S0 – got zero 1s (modulo 5)
S1 – got one 1 (modulo 5)
S2 – got two 1s (modulo 5)
S3 – got three 1s (modulo 5)
S4 – got four 1s (modulo 5)

<u>Verilog Description of FSM</u>

```
module moore_countmod5(data,clock,reset,out);
       input reset, clock;
       input[1:0] data;
       output out;
       reg out;
       reg [2:0] state, next_state;
       parameter st0 = 3'b000, st1 = 3'b001, st2 = 3'b010, st3=3'b011, st4=3'b100;
       //FSM register
              always @(posedge clock or negedge reset)
              begin: statereg
                     if(!reset) //asynchronous reset
                     state <= st0;
                     else state <= next_state;
                     end //statereg
       //FSM next_state logic
       always @(state or data)
              begin: fsm
              case (state)
              st0: case (data)
                     2'b00: next_state = st0;
```

```
                2'b01,2'b10: next_state = st1;
                2'b11: next-state = st2;
                default: next_state = st0;
                endcase
         st1:case(data)
                2'b00: next_state =st1;
                2'b01, 2'b10: next_state=st2;
                2'b11: next_state = st3;
                default: next_state = st0;
                endcase
         st2: case(data)
                2'b00: next_state = st2;
                2'b01, 2'b10: next_state=st3;
                2'b11: next_state = st4;
                default: next_state = st0;
                endcase
         st3: case(data)
                2'b00: next_state = st3;
                2'b01, 2'b10: next_state=st4;
                2'b11: next_state = st0;
                default: next_state = st0;
                endcase
         st4: case(data)
                2'b00: next_state = st4;
                2'b01, 2'b10: next_state=st0;
                2'b11: next_state = st1;
                default: next_state = st0;
                endcase
         default: next_state = st0;
         endcase
         end//fsm
  //Moore output definition using pres_state only
         always @(state)
         begin: def_out
         if (state == st0)
         out = 1'b1;
         else out = 1'b0;
         end//def_out
         endmodule
```

<u>Synthesis of FSM using D flip-flops</u>

1. State Assignment (first example)

Number of flip-flops: $n=\lceil loq_2 5 \rceil = 3$.

S0 – 000

S1 – 001

S2 – 010

S3 – 101

S4 – 100

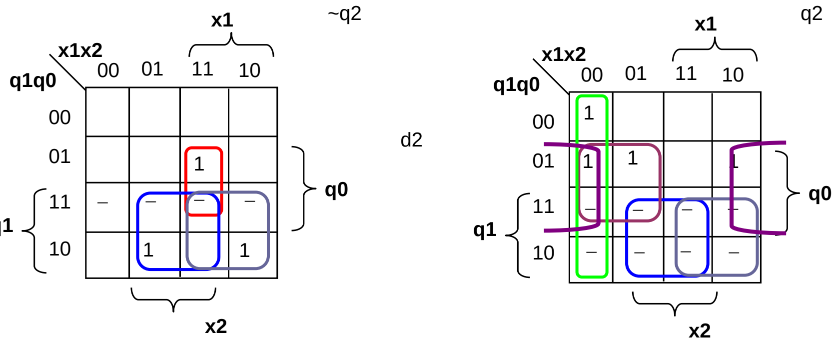
FSM inputs are designated as x1, x2.

FSM output is designated as y.

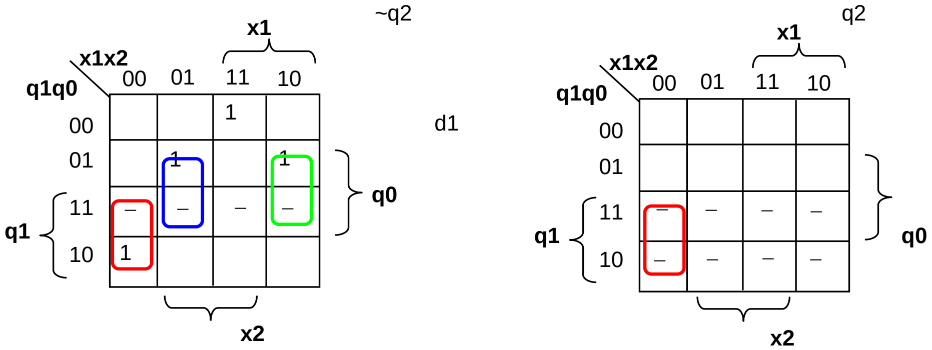
2. Transition and output table

Present_state		Input	Next_state	Excitation Functions
q2 q1 q0	y	x1 x2	q2 q1 q0	d2 d1 d0
0 0 0	1	00	0 0 0	0 0 0
		01v10	0 0 1	0 0 1
		11	0 1 0	0 1 0
0 0 1	0	00	0 0 1	0 0 1
		01v10	0 1 0	0 1 0
		11	1 0 1	1 0 1
0 1 0	0	00	0 1 0	0 1 0
		01v10	1 0 1	1 0 1
		11	1 0 0	1 0 0
1 0 1	0	00	1 0 1	1 0 1
		01v10	1 0 0	1 0 0
		11	0 0 0	0 0 0
1 0 0	0	00	1 0 0	1 0 0
		01v10	0 0 0	0 0 0
		11	0 0 1	0 0 1

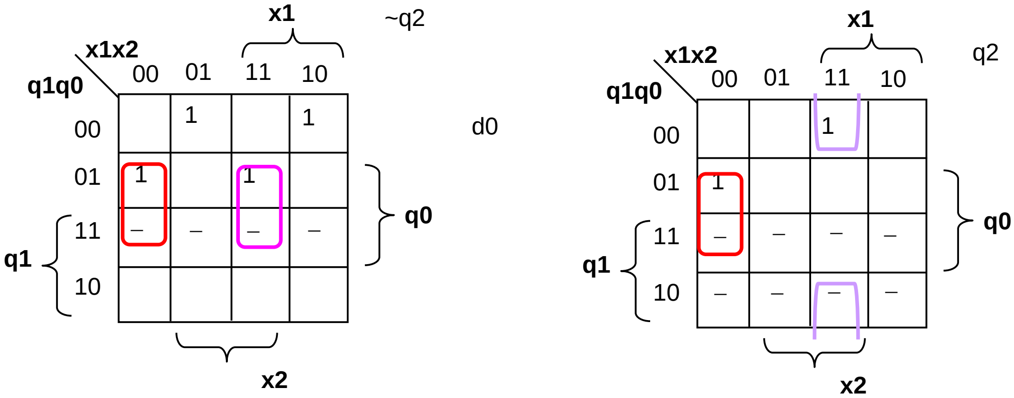
3. Minimization of Excitation Functions
d2, d1, d0 depend on 5 variables: q2,q1,q0,x1,x2.
Unused states: 011, 110, 111. (solution of minimal-value)



d2=q1 ·x2 +q1 ·x1+~q2q0x1x2+q2~x1~x2+q0q2~x1+q2q0~x2



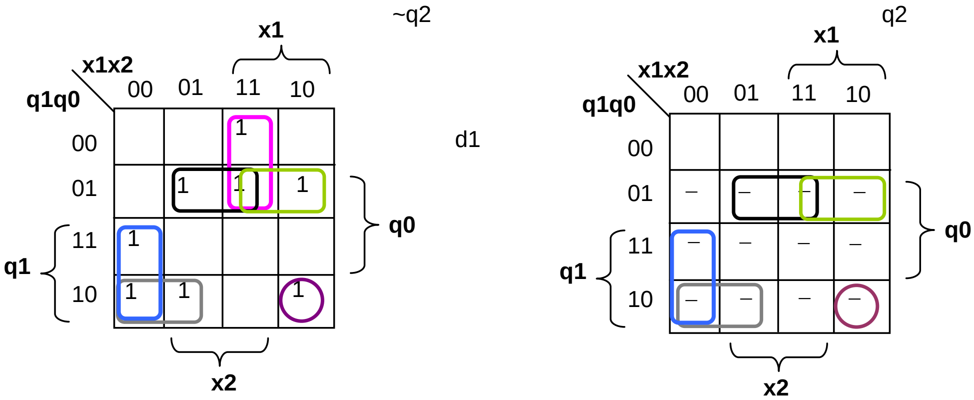
d1=q1~x1~x2+q0~q2~x1x2+q0~q2x1~x2+~q2~q1~q0x1x2

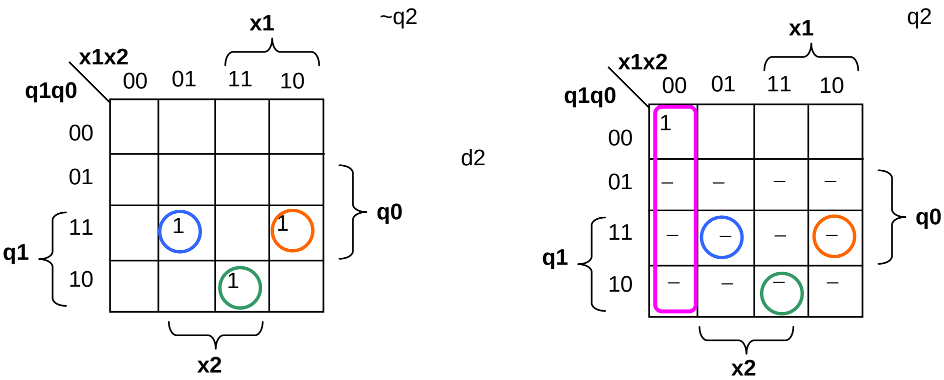


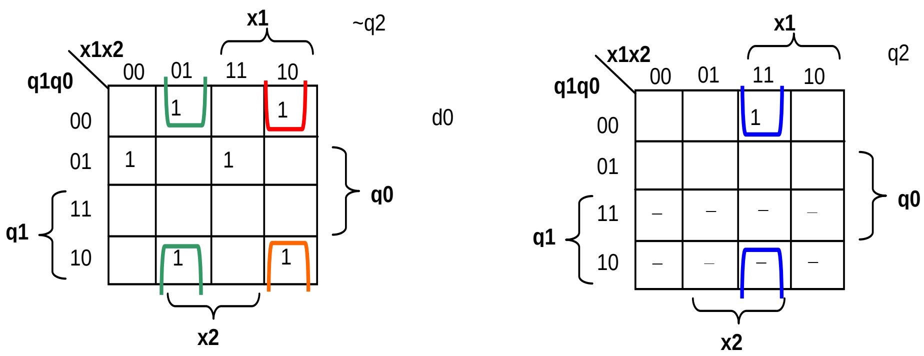
d0=q0~x1~x2+q0~q2x1x2+~q0~q1~q2~x1x2+~q0~q1~q2x1~x2+~q0q2x1x2
The number of inputs of gates is equal to 69.
4. The second example of states assignment using D flip-flops
S0 – 000, S1 – 001, S2 – 010, S3 - 011, S4 – 100.
Unused states. 101, 110, 111 (minimal-value solution)

Present_state		Input	Next_state	Excitation Functions	Excitation Functions
q2 q1 q0	y	x1 x2	q2 q1 q0	t2 t1 t0	d2 d1 d0
0 0 0	1	00	0 0 0	0 0 0	0 0 0
		01v10	0 0 1	0 0 1	0 0 1
		11	0 1 0	0 1 0	0 1 0
0 0 1	0	00	0 0 1	0 0 0	0 0 1
		01v10	0 1 0	0 1 1	0 1 0
		11	0 1 1	0 1 0	0 1 1
0 1 0	0	00	0 1 0	0 0 0	0 1 0
		01v10	0 1 1	0 0 1	0 1 1
		11	1 0 0	1 1 0	1 0 0
1 0 1	0	00	0 1 1	0 0 0	0 1 1
		01v10	1 0 0	1 0 0	1 0 0
		11	0 0 0	0 1 1	0 0 0
1 0 0	0	00	1 0 0	0 0 0	1 0 0
		01v10	0 0 0	1 0 0	0 0 0
		11	0 0 1	1 0 1	0 0 1

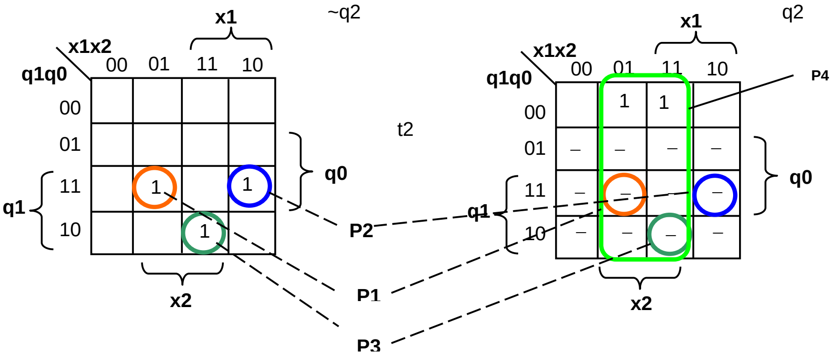
Minimization of Excitation Functions

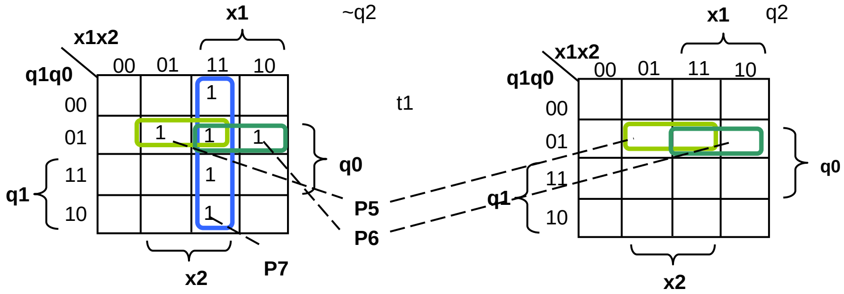


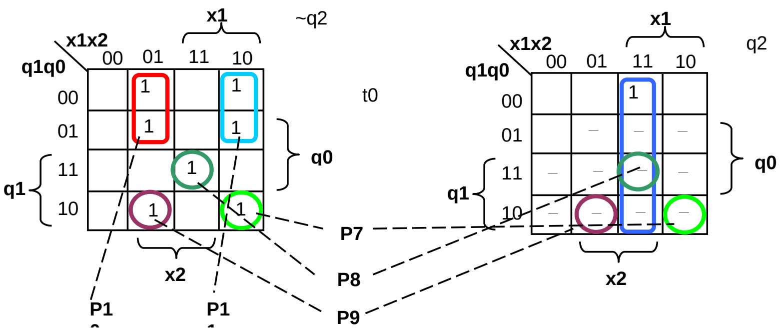




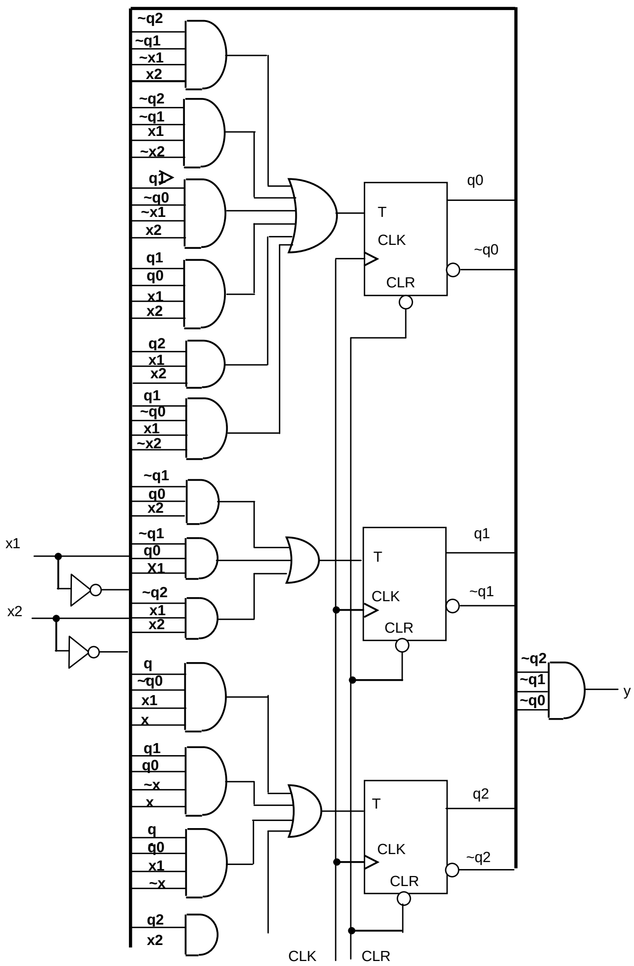
d2 = q1 ·q0 ·~x1 ·x2 + q1 ·~q0 ·x1 ·x2 + q2 ·x1 ·x2 + q1 ·q0 ·x1 ·~x2
d1= q1 ·~x1 ·~x2 + q0 ·~q1 ·x2 +q1 ·~q0 ·~x1 + ~q1 ·~q2 ·x1 ·x2 +q0 ·~q1 ·x1+q1~q0x1~x2
d0 =~q2 ·~q0 ·~x1 ·x2+~q2 ·~q0 ·x1 ·x2 +~q0 ·q2 ·x1 ·x2+~q1 ·~q2 ·q0 ·~x1 ·x2+
+~q2 ·~q1 ·q0 ·x1 ·x2
The number of gates' inputs is equal to 72.
The values of both examples are approximately the same.
Synthesis of FSM using T flip-flops
Excitation functions are shown in the table above.







t2=q1q0~x1x2 + q1~q0x1x2 + q1q0x1~x2 + q2x2;
t1=~q1q0x2 + ~q1q0x1 + ~q2x1x2
t0=~q2~q1~x1x2 + ~q2~q1x1~x2 + q2x1x2 + q1~q0~x1x2 + q1q0x1x2 + q1~q0x1~x2
The number of gates' inputs is equal to 63.
Definition of y=f(q2,q1,q0)
y= ~q2 ~q1 ~q0
The last variant of implementation should be chosen.



FSM circuit diagram

1b25.

The minimum signal formation time in some i-th net is defined by the following formula:

$$t_{bi}=\max[t_{b(i-1)} + t_{(i-1,\, i)}],$$

where t_{bi} and $t_{b(i-1)}$– minimum limit times of i-th and (i-1)-th nets correspondingly; $t_{(i-1,\, i)}$- is the delay of the element for which (i-1)-th net is input and i-th net – output.

The maximum signal formation time in some i-th net is defined by the following formula:

$$t_{ri}=\min[t_{r(i+1)} - t_{(i+1,\, i)}],$$

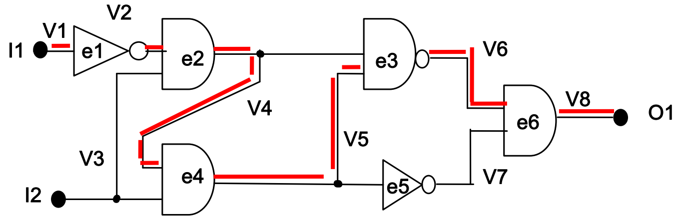
where t_{ri} and $t_{r(i+1)}$– maximum limit times of i-th and (i+1)-th nets correspondingly; $t_{(i+1,\, i)}$- is the delay of the element for which (i+1)-th net is output and i-th net – input.

Time reserve for i-th net will be:

$$h_i = t_{maxi} – t_{mini}.$$

Calculation results are shown in the table

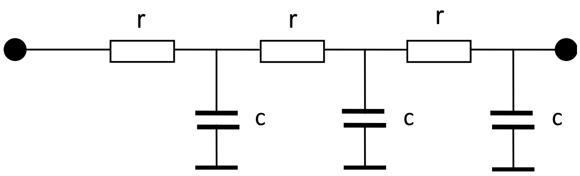
Net	V1	V2	V3	V4	V5	V6	V7	V8
t_{mini}	0	10	0	30	50	65	60	85
t_{maxi}	0	10	10	30	50	65	65	85



Critical path passes through all the nets for which $t_{bi}=t_{ri}$, i.e. V1, V2, V4, V5, V6, V8. The total delay of that path is 85.

1b26.

The equivalent circuit of interconnect's 3-segment, R,C distributed parameters will look like this:



The delay in it will be

$$\tau= rc + 2rc + 3rc = 6rc:$$

$$r =[(300:3):0{,}2]x0{,}1 = 50 \text{ Ohm},$$

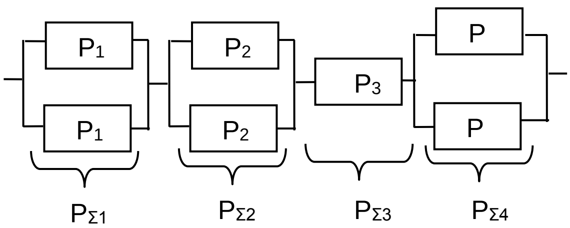
$$c = \frac{300}{3}\cdot 0.1 = 10 \text{ fF}$$

$$c = (300:3)x0{,}1 = 10 \text{ fF},$$

$$\tau= 6x50x10 = 3000 \text{ OhmfF} = 3 \text{ ns}.$$

1b27.

Present the given circuit in the view of 4 sequentially connected regions:



Designate faultness probabilities of those regions

$$P_{\Sigma 1},\ P_{\Sigma 2},\ P_{\Sigma 3},\ P_{\Sigma 4}.$$

Using probability summing, multiplication and full probability laws, the following can be written:

$$P_{\Sigma 1} = P_1P_1 + 2P_1(1-P_1)= P_1(2-P_1)=0{,}5(2-0{,}5)=0{,}75$$

$$P_{\Sigma 2} = P_2(2-P_2)=0{,}84$$

$$P_{\Sigma 3} = P_3=0{,}8$$

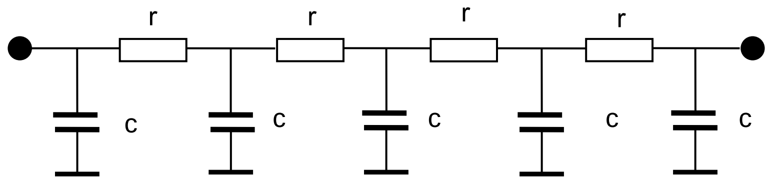
$$P_{\Sigma 4} = P_4(2-P_4)=0{,}64$$

The faultness probability of the circuit will be:

$$P= P_{\Sigma 1} \cdot P_{\Sigma 1} \cdot P_{\Sigma 1} \cdot P_{\Sigma 1}=0{,}75\cdot 0{,}84\cdot 0{,}8\cdot 0{,}64=0{,}32256.$$

1b28.

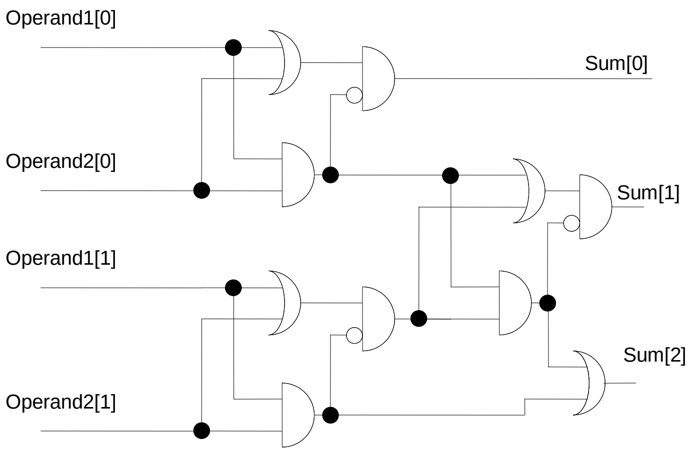
R, C equivalent circuit of interconnect will look as follows:



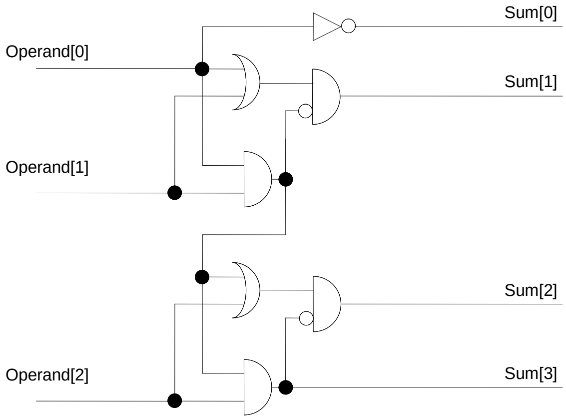
The delay in the transmission line connecting two contacts will be:

$$\tau= rc + 2rc + 3rc + 4rc = 10rc=10\cdot 1\cdot 100=1000 \text{ OhmfF} = 10 \text{ ns}.$$

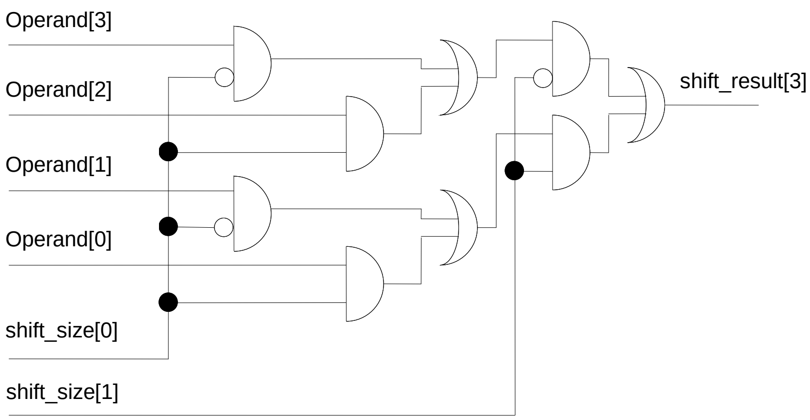
1b29.



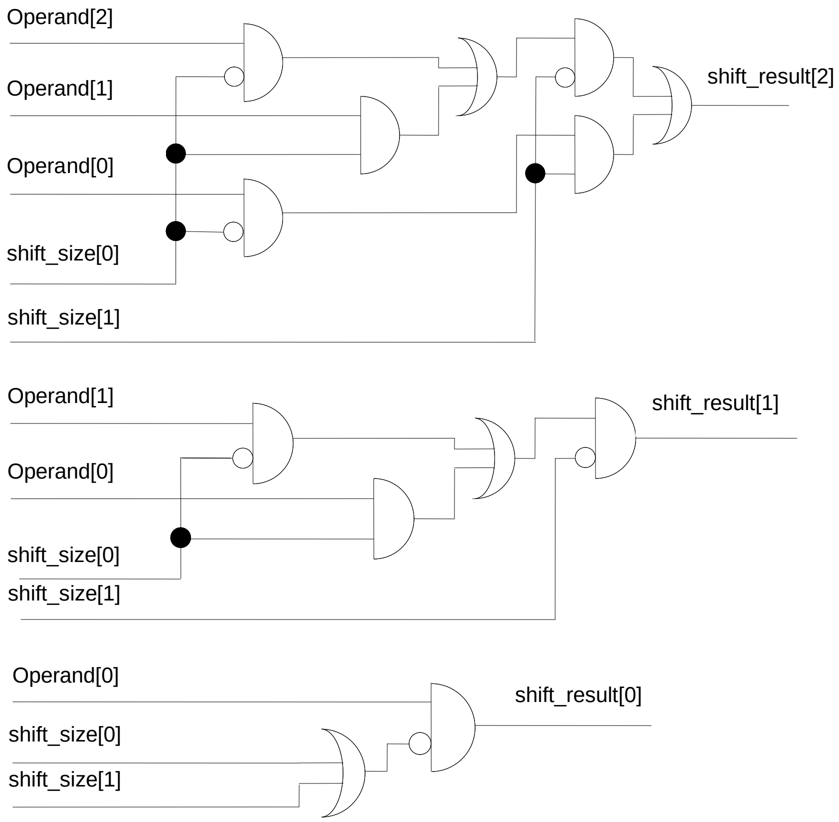
1b30.



Yes, given logic is a pure combinatorial logic as it doesn't contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

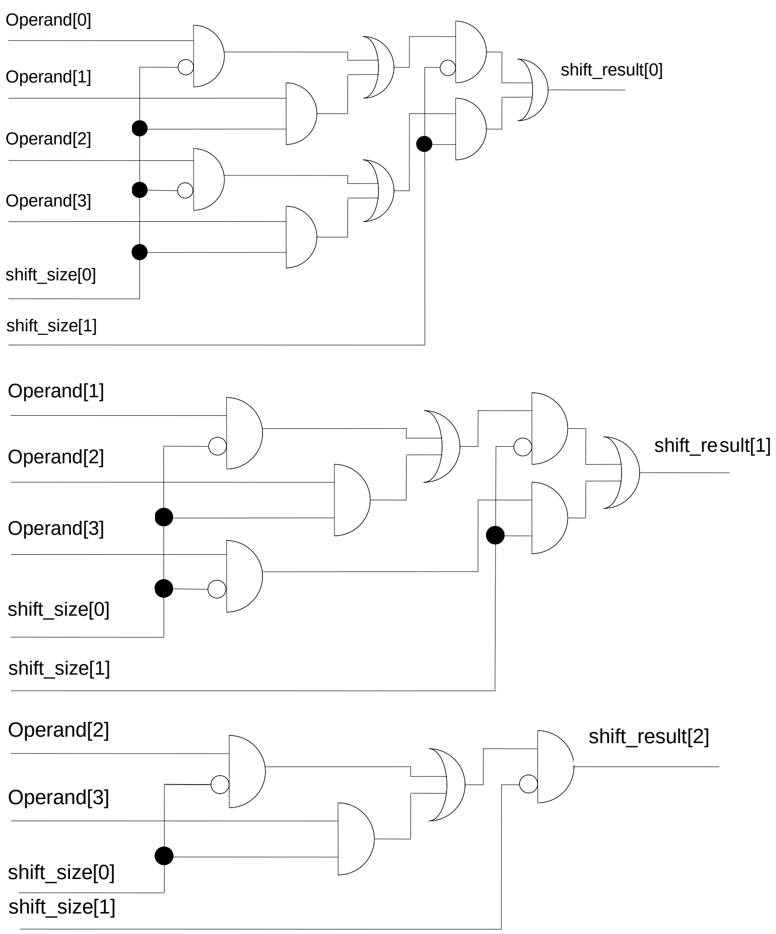


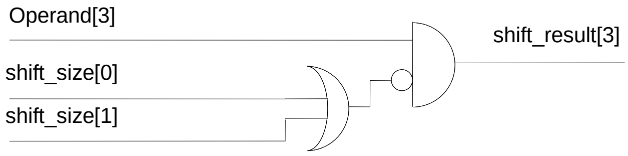
1b31.



Yes, given logic is a pure combinatorial logic as it doesn't contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

1b32.





Yes, given logic is a pure combinatorial logic as it does not contain any memory elements and any logical feedbacks. Also, the outputs are only and only dependent from the inputs (from the combinations of inputs).

1b33.

$t_{d1}=R_1C_{L1}=R_12yC_{in1}=2yR_1C_{in1}=2yR_1C$

$t_{d2}=R_2C_{L2}=(R_1/y)3z\ C_{in1}=3zR_1C/y$

$t_{d3}=R_3C_{L3}=(R_1/z)4.5C_{in1}=4.5R_1C/z$

$t_d=t_{d1}+t_{d2}+t_{d3}=R_1C(2y+3z/y+4.5/z)$

$\partial t_d/\partial z= R_1C(3/y-4.5/z^2)=0$

$\partial t_d/\partial y= R_1C(2-3z/y^2)=0$

From the solution of system y=1.275; z=1.084.

1b34.

Answer: 0.29 V

1b35.

When $V_{in}=V_H$, NMOS is in active mode, and PMOS is in saturated mode.

$$C_{ox}=\frac{\varepsilon_{ox}\varepsilon_0}{T_{ox}}=\frac{3.9\cdot 8.854\cdot 10^{-14}}{10^{-6}}=3.45\cdot 10^{-7}\,F/cm^2$$

$k_p=\mu_pC_{ox}= 241*10^{-7}A/V^2=24.1\mu A/V^2$; $k_n=\mu_nC_{ox}= 93.15\mu A/V^2$;

a.$V_{OH}=V_{DD}=1.8$ V,

$$\beta_p(VDD-V_{TP})^2/2=\beta_n((VDD-V_{TN})V_{OL}-V_{OL}^2/2)$$

$$V_{OL}=(VDD-V_T)(1-\sqrt{1-\frac{\beta_p}{\beta_n}})$$

a. $\beta_p=k_p(W/L)p= 669.4\ \mu A/V^2$

$\beta_n=k_n(W/L)n= 10350\ \mu A/V^2$

$V_{OL}=(1.8-0.5)(1-(1-669.4/10350)^{0.5})=0.043$ V

$V_{OL}=0.043V$; $V_{OH}=VDD=1.8$ V,

b. $b_n=4k_n(W/L)n= 41400\ \mu A/V2$

$V_{OL}=(1.8-0.5)(1-(1-669.4/41400)^{0.5})=0.011$ V

$V_{OL}=0.011V$; $V_{OH}=VDD=1.8$ V

1b36.

Minimum range of clock pulses in digital circuits is defined from the condition of not violating setup time of flip-flop:

$T_{CLKmin}= t_{c2q}+t_{pinv}+t_{su}=100+30+20=150ps$

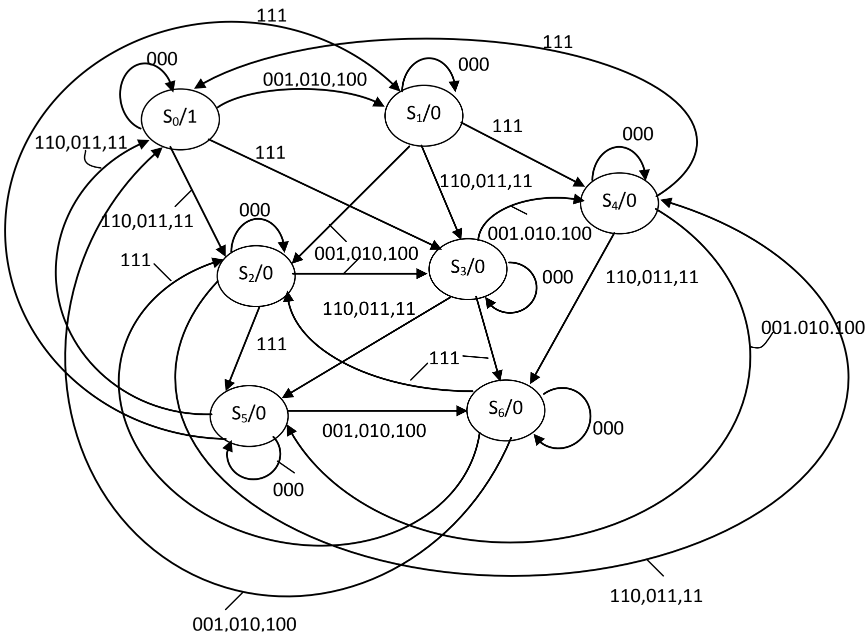
1b37.

a. $\Delta V_V=\frac{C_{AV}}{C_V+C_{AV}}\Delta V_A=\frac{100}{60+100}\cdot 1=0.625\text{V}$

b. $C_{Vsw}=C_V+2C_{AV}$=60+2Ē100=260 fF

1b38.

Design of Moore's FSM:



Description of FSM by Verilog

```
module  fsm(in,out,clk,reset);
input  clk,reset;
input[2:0] in;
output  out;
reg  out;
reg[2:0]  state, next_state;
parameter  s0=3'b000, s1=3'b001, s2=3'b010, s3=3'b011, s4=3'b100,s5=3'b101,s6=3'b110;
//state register
always @(posedge clk or negedge reset)
       begin
       if (!reset) state=s0;
              else state=next_state;
       end
//next state logic
always @(state or in)
       begin
              case (state)
              s0: case (in)
              3'b000:       ßnext_state=state;
              3'b001,3'b010,3'b100: next_state=s1;
              3'b011,3'b101,3'b110: next_state=s2;
              3'b111:             next_state=s3;
              default:            next_state=s0;
              endcase
s1: case (in)
       3'b000:             next_state=state;
       3'b001,3'b010,3'b100: next_state=s2;
       3'b011,3'b101,3'b110: next_state=s3;
       3'b111:             next_state=s4;
       default:            next_state=s0;
       endcase
 s2: case (in)
              3'b000:             next_state=state;
              3'b001,3'b010,3'b100: next_state=s3;
              3'b011,3'b101,3'b110: next_state=s4;
              3'b111:             next_state=s5;
              default:            next_state=s0;
              endcase
       s3: case (in)
       3'b000:             next_state=state;
       3'b001,3'b010,3'b100: next_state=s4;
       3'b011,3'b101,3'b110: next_state=s5;
       3'b111:             next_state=s6;
       default:            next_state=s0;
       endcase
              s4: case (in)
```

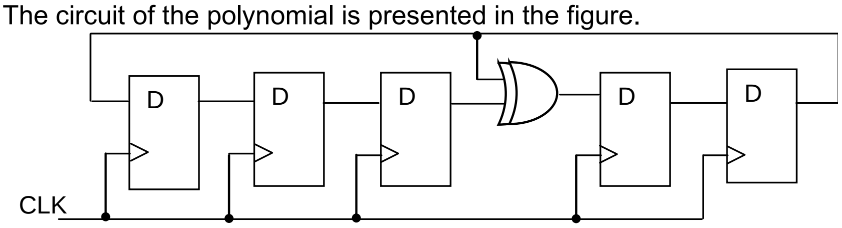
```
                    3'b000:             next_state=state;
                    3'b001,3'b010,3'b100: next_state=s5;
                    3'b011,3'b101,3'b110: next_state=s6;
                    3'b111:             next_state=s0;
                    default:            next_state=s0;
                    endcase
s5: case (in)
          3'b000:             next_state=state;
          3'b001,3'b010,3'b100: next_state=s6;
          3'b011,3'b101,3'b110: next_state=s0;
          3'b111:             next_state=s1;
          default:            next_state=s0;
          endcase
                    s6: case (in)
                    3'b000:             next_state=state;
                    3'b001,3'b010,3'b100: next_state=s0;
                    3'b011,3'b101,3'b110: next_state=s1;
                    3'b111:   next_state=s2;
                    default:            next_state=s0;
                    endcase
default: next_state=s0;
endcase
end
          //output logic
always @(state)
          if (state==s0)
          out=1'b1;
else out=1'b0;
endmodule
```

Testbench

```
module stimulus;
reg[2:0] in;
reg clk, reset;
fsm test(in,out,clk,reset);
initial begin
     clk=0;
     reset=1;
     #10 reset = 0;
     in=0;
     #13 reset = 1;
     #10 in = 3'd0;
     #10 in = 3'd2;
     #10 in = 3'd1;
     #10 in = 3'd3;
     #10 in = 3'd5;
     #10 in = 3'd0;
     #10 in = 3'd4;
     #10 in = 3'd7;
     #10 in = 3'd1;
     #10 in = 3'd7;
     #10 in= 3'd0;
     #10 $finish;
end
always #5 clk = ~clk;endmodule
```

1b39.

The circuit of the polynomial is presented in the figure.



The description of the counter by Verilog

```
module polynomial_counter (clk, preset, q);
input   clk, preset;
output[0:4] q;
reg [0:4]  q;
always  @(posedge clk or negedge preset)
```

```
        if     (!preset)
        q= 5'b10000;
        else q={q[4], q[0], q[1],q[2]^q[4], q[3]};
endmodule
```

Testbench

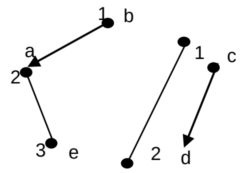
```
module stimulus;
reg clk, preset;
wire[0:4] q;
polynomial_counter  test(clk,preset,q);
       initial begin
          clk=0;
          preset=1;
          #3 preset=0;
          #20 preset = 1;
          #200 $finish;
       end
always #5 clk=~clk;
endmodule
```

1b40.

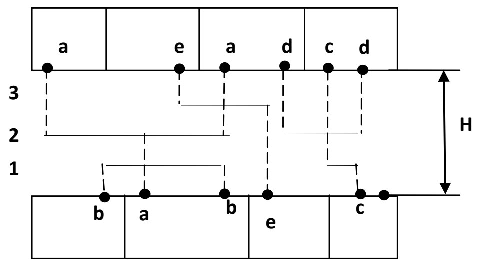
The problem is solved in two phases:

- Definition of minimum number of horizontal channels;
- Calculation of minimum H distance between two rows of cells.

Construct horizontal and vertical limitations graph of a, b, c, d, e nets and heuristically define its chromatic number, as shown in the figure below.



As seen from the figure, chromatic number of the graph equals 3. Hence it follows that for two-layer reciprocally perpendicular routing of the given nets, at least 3 horizontal channels are needed, as shown in the figure.



Thus, the minimum H distance between two rows of cells will be defined by the formula, shown below.
H= 3*0,1 + 2*0,1 + 2*0,2=0,9 um.

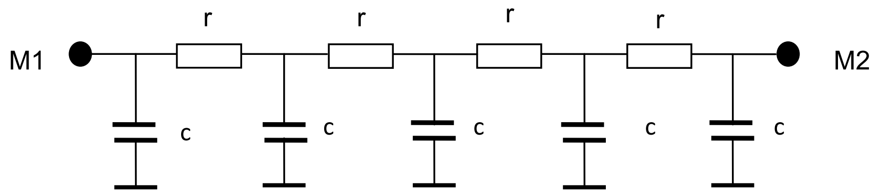
1b41.

The solution of the problem is based on the fact that N-MOS transistor is open, if “1” logic level signal is given to its gate, and P-MOS transistor - “0” logic level signal. Therefore the solution of the problem is the following:

a) T1, T2, T3, T4, T5, T6 →“0”;
b) T1, T3 →“0” ; T2, T4, T5, T6 →“1”.

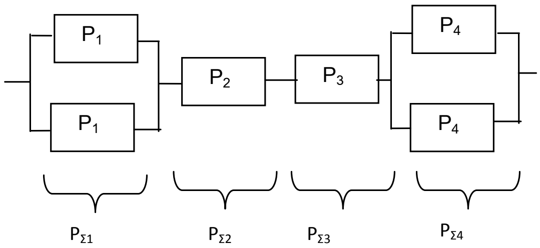
1b42.

R, C equivalent circuit of M1-M2 transmission line will look as follows:



The delay in the transmission line, connecting two modules, will be:
τ= rc + 2rc + 3rc + 4rc = 10rc=10x10x100=10000 OhmfF = 10 ns.

1b43.
Present the given circuit in the form of 4 sequentially connected regions:



Designate the probabilities of faultless operation of those regions $P_{\Sigma1}$, $P_{\Sigma2}$, $P_{\Sigma3}$, $P_{\Sigma4}$.
Using the rules of addition, multiplication of probabilities and full probabilities, the following can be written:
$P_{\Sigma1} = P_1P_1 + 2P_1(1-P_1)= P_1(2-P_1)=0,5(2-0,5)=0,75$
$P_{\Sigma2} = P_2 =0,6$
$P_{\Sigma3} = P_3=0,8$
$P_{\Sigma4} = P_4(2-P_4)=0,64$
The probability of faultless operation of the circuit will be
$P= P_{\Sigma1}$ x$P_{\Sigma1}$ x$P_{\Sigma1}$ x$P_{\Sigma1}$=0,75x0,6x0,8x0,64=0,2304.

1b44.
The same current flows through both transistors. V_x<4V, the transistor below is not saturated $V_{DS}<V_{GS}-V_T$, and the one above is saturated $V_{DS}=V_{GS}=5-V_x$.

$$\frac{1}{2}[V_{GS} \;\; -V_t]^2 = [V_{GS} \;\; -V_{t0} - \frac{V_{DS2}}{2}]V_{DS2}$$
$$V_t = V_{t0} + \gamma(\sqrt{2\,|\,\Phi_F\,| + V_{SB}} - \sqrt{2\,|\,\Phi_F\,|}) = 1 + 0.39(\sqrt{1.2+V_x} - \sqrt{1.2})$$
$$\frac{1}{2}[5 - V_x - (1 + 0.39(\sqrt{1.2+V_x} - \sqrt{1.2}))]^2 = [5 - 1 - \frac{V_x}{2}]V_x$$

Solving these equations, for example graphically, the following will be obtained V_x=1.09V.
Taking W/L=1,

$$I_D = K_P[5 - 1 - \frac{V_x}{2}]V_x = 25\cdot(4-0.24)\cdot 0.48 = 45.12uA$$

1b45.

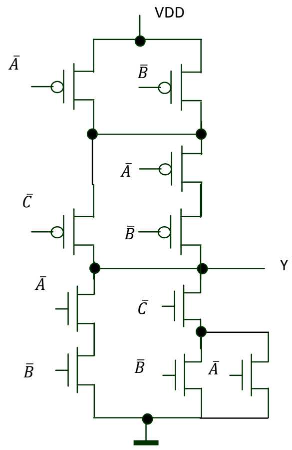
a. $A = (C_L/C_{in1})^{1/N}$
 $A=(20\cdot10^3/10)^{1/3}=12.6$
 $(W/L)_1=1$, $(W/L)_2=12.6$, $(W/L)_2=158.7$
 $t_d=0.7N(R_{n1}+R_{p1})(C_{out1}+AC_{in1})=2.1R_1(C_{out1}+12.6C_{in1})\approx26.5R_1C_{in1}$

b. $N=\ln(C_L/C_{in1})= \ln(20\cdot10^3/10)=7.6$
 N=7
 $A=(20\cdot10^3/10)^{1/7}=2.96$
 $(W/L)_1=1$, $(W/L)_2=A^2,\ldots, (W/L)_7=A^7$
 $t_d=0.7N(R_{n1}+R_{p1})(C_{out1}+AC_{in1})=4.9R_1(C_{out1}+2.96C_{in1})\approx14.5R_1C_{in1}$

c. $P=V_{DD}^2F\, C_{in1}\Sigma(A+A^2+..+A^7)$

1b46.

$F = \overline{\bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}} = \overline{\bar{A}\bar{B} + \bar{C}(\bar{A} + \bar{B})}$



$R_{Pnetmin}$=7R_P/6, when ABC=111; $R_{Pnetmax}$=2.5R_P, when ABC=110,
$R_{Nnetmin}$=6R_N/7, when ABC=000; $R_{Nnetmax}$=2R_N, when ABC=001
$R_{Pnetmax}$= $R_{Nnetmax}$ => R_P=4R_N/5 => Wp=8W_N/5

1b47.

a.

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	1

$Out = \overline{A \oplus B}$

b. Out=V_{OL}, when NMOS conducts V_{DSn}=0.3V, V_{GSn}=2.5V, NMOS is in linear mode.
PMOS is saturated V_{DSp}=2.5-0.3=2.2V > V_{GSp}-V_t=2.5-5=2V.
$I_D=0.5\beta_p(V_{GSp}-V_T)^2= \beta_n((V_{GSn}-V_T)V_{DSn}-0.5V_{DSn}^2)$
$0.5W_pk_p(2.5-0.5)2=W_nk_n((2.5-0.5)*0.3-0.5*0.3^2)$, $k_n=2k_p$
$W_p=0.6W_n$=0.9um.

1b48.

a. V_x changes from 2.5V to 0V. The time of V_x charge up to 1.25V will be t=CR_{Mn}ln(2.5/2).

b. The final voltage of x node will be (2.5-V_{Tn})=2.07V, the initial voltage is 0 V. The change time of V_x will be t= CR_{Mn}ln(2.07/(2.07-1.25))

c. V_{Bmin}=1.25-V_{Tn}=0.82V.

1b49.

a. $V_{SBM3}=V_x$, $V_x=V_{DD}-V_t=V_{DD}-V_{t0}-\gamma((2|\Phi_F|+V_{SB})^{0.5}-(2|\Phi_F|)^{0.5}))$
V_x= 2.5-0.5-0.5$((0.6+V_x)^{0.5}-(0.6)^{0.5}))$
V_x= 1.61-0.5$(0.6+V_x)^{0.5}$

b. When $V_{in}=V_L$, $V_{DS2}=V_{DD}-(Vx-V_t)=2V_t$=1V, $V_{GSM2}=V_x=V_{DD}-V_t$=2.0V, M2 is in linear mode.
When $V_{in}=V_H$, $V_{DS2}=V_{DD}-V_{DS1}$, M2 is saturated if $V_{DS1}<2V_t$.

c. V_{in}=0, V_{out}= $V_{GSM2}-V_t=V_{DD}-2V_t$=1.5V.

d. When $V_{in}=V_{SP}$, $V_{out}=V_{in}$, considering that M1 and M2 are saturated.
$0.5\beta_2(V_{DD}-2V_t)^2=0.5\beta_1(V_{SP}-V_t)^2$,

$$V_{SP} = \frac{\sqrt{\frac{\beta_1}{\beta_2}}V_T + (V_{DD} - 2V_T)}{\sqrt{\frac{\beta_1}{\beta_2}}}$$

If $W_1>>W_2$, $\beta_1>>\beta_2$, $V_{SP}=V_T$=0.5V.
If W1<<W2, $\beta_1<<\beta_2$, $V_{SP}=V_{DD}-2V_T$=1.5V, M2 is not saturated $V_{DSM2}=V_{DD}-V_{SP}$=1.0V, $V_{GSM2}=V_{DD}-V_t$=2.0V.
But for M2 to conduct, V_{out} must be smaller or equal to 1.5V. Considering W1<<W2, the output voltage will have the maximum possible value 1.5V.

1b50.

a. When $V_{in}=V_H$, NMOS is in active mode, PMOS - saturated.
$I_D=0.5\beta_p(V_{GSp}-|V_{Tp}|)^2= \beta_n((V_{GSn}-V_{Tn})V_{DSn}-0.5V_{DSn}^2)$
$0.5\beta_p(2.5-0.4)^2= \beta_n((2.5-0.5)V_{OL}-0.5V_{OL}^2)$;
$\beta_n/\beta_p=(W_n/W_p)(k_n/k_p)$=(4/0.5)(120/30)=64
V_{OL}=0.01V,

$V_{OH}=V_{DD}=2.5V$.

b. $V_{SP}=V_{in}=V_{out}$.

First consider the transistors are saturated.

$0.5\beta_p(V_{DD}-|V_{tp}|)^2=0.5\beta_n(V_{SP}-V_{tn})^2$,

$$V_{SP}=\frac{\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}+(V_{DD}-|V_{Tp}|)}{\sqrt{\frac{\beta_1}{\beta_p}}}=0.7625V$$

But when $V_{out}=0.7625V$, $V_{DS}=2.5-0.7625<V_{GS}-|V_{TP}|=2.1V$. Therefore PMOS is not saturated. Then V_{SP} must be calculated from the following equation:

$\beta_p((V_{DD}-|V_{tp}|)V_{SP}-V_{SP}^2/2)=0.5\beta_n(V_{SP}-V_{tn})^2$,

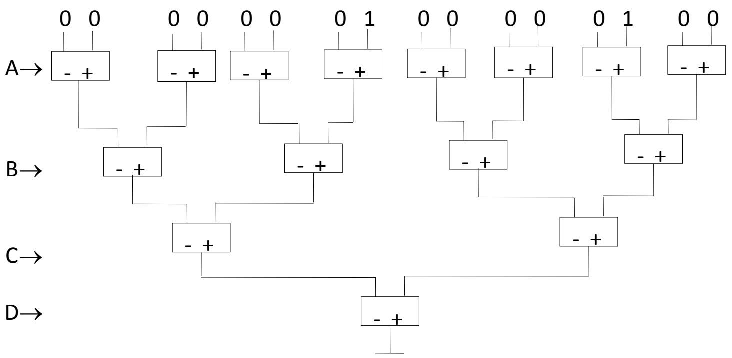
$(2.5-0.4)V_{SP}-V_{SP}^2/2=32(V_{SP}-0.5)^2$,

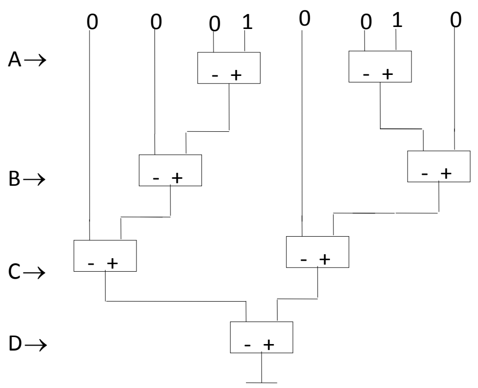
$V_{SP}=0.695V$.

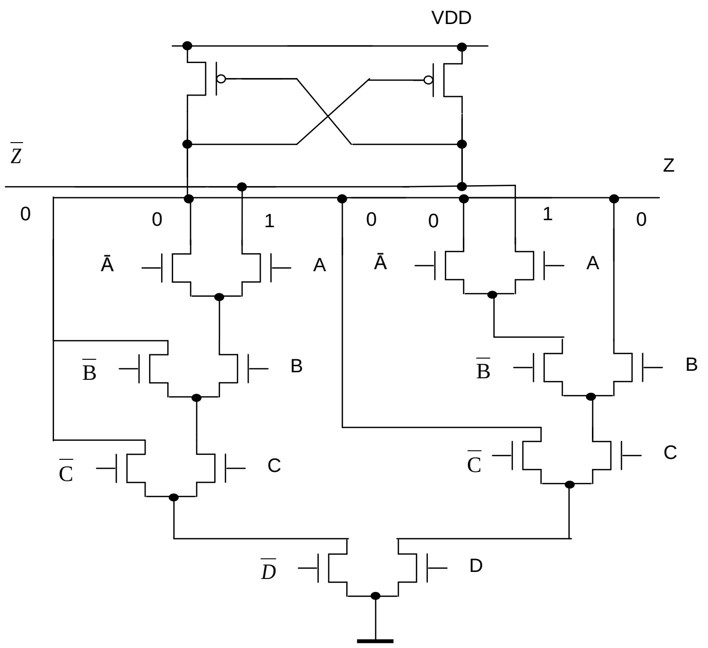
1b51.

The truth table of $F = ABC\bar{D} + A\bar{B}CD$ function, the initial and simplified graphs of NMOS and the circuit are shown below.

F	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1







1b52.

1. S1 = 0; S2 = 1; S3= 0;
2. S1 = 1; S2 = 1; S3= 0;
3. S1 = x; S2 = x; S3= 1;
4. S1 = x; S2 = 0; S3= 0;

Verilog description of the circuit.

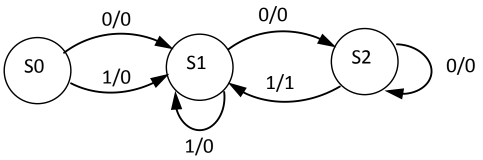
```
module  task_1(data, clk, S1,S2, S3, reset, out);
     input data, clk, S1,S2, S3, reset;
     output out, q1, q2, q3;

always @(posedge clk)
             if (reset==0) q1=0; //synchronous reset
             else  if (S1==1) q1=q1^data;//T flip-flop
             else q1=data;       //D-flip-flop

always @ (data or q1)
           if (S2)  q3=q1;
           else q3=data;

always @ (clk or data)
          if (clk) q2=data;
          else q2=q2;

always @(q2 or q3)
          if (S3) out=q2;
          else out = q3;

endmodule
```

1b53.

The characteristic equation of D flip-flop is q* = d;
d1 = $\bar{x}\cdot q2$; d2=1;
Hence q1*= $\bar{x}\cdot q2$; q2* =1; y=x·q1;

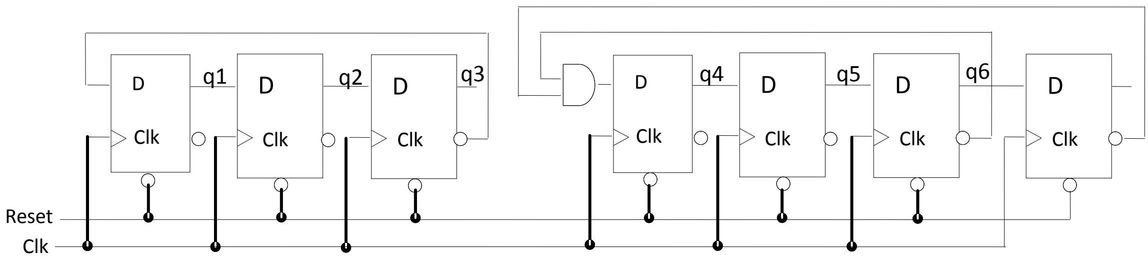
State	X=0	X=1
0 0	0 1, 0	0 1, 0
0 1	1 1, 0	0 1, 0
1 1	1 1, 0	0 1, 1

FSM has three states 00, 01, 11. The naming of states is 00 = S0, 01 = S1, S2=11.
The state diagram of FSM is shown.
The derived FSM is a detector of input sequencies 001 and 101.



1b54.

To obtain the module of count equal to 42, use two Johnson's counters with modules 6 and 7.
Counter are moving in count independent. The circuit is represented below.



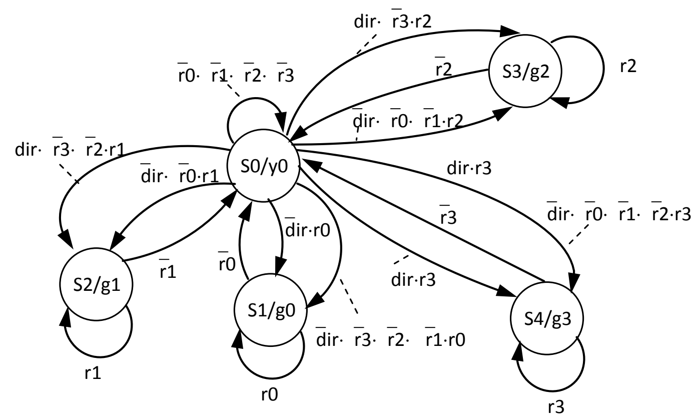
The state 1111 (d4= $\bar{q}6\cdot \bar{q}7$) is skipped. The S5 state decoding function is f = $\bar{q}2\cdot q3 + \bar{q}5\cdot q6$

1b55.

Consruction arbiter state diagram. FSM input alphabet X={r0, r1, r2, r3, dir}, where r0,r1,r2,r3 are service request from devices. The input dir sets device priorities. If dir=0, the request r0 has the highest priority, then r1,r2,r3 are followed.
If dir=1, priorities have inverse order. The state diagram of FSM is shown below.

Verilog description of the arbiter

```
module arbiter(r,g,clk,reset, dir);
input [0:3] r;
input reset,clk,dir;
output [0:3] g;
parameter s0=3'b000,s1=3'b001,
s2=3'b010,s3=3'b011,s4=3'b100;
reg [2:0] next_state,state;
always @(posedge clk)
if(!reset) state=s0;
else state=next_state;
always @(r or state)
begin
case (state)
```




```
s0:casex({r,dir})
5'b0000x: next_state=s0;
5'b1xxx0,5'b10001: next_state=s1;
5'b01xx0,5'bx1001: next_state=s2;
5'b001x0,5'bxx101: next_state=s3;
4'b00010,5'bxxx11: next_state=s4;
default: next_state=s0;
endcase
s1: if (r[0]) next_state=s1;
       else next_state=s0;
s2: if (r[1]) next_state=s2;
       else next_state=s0;
s3: if (r[2]) next_state=s3;
       else next_state=s0;
s4: if(r[3]) next_state=s4;
       else next_state=s0;
       default:next_state=s0;
       endcase
       end
assign g[0]=(state==s1);
assign g[1]=(state==s2);
assign g[2]=(state==s3);
assign g[3]=(state==s4);
endmodule
```

S0 - initial state of FSM, requests are absent
S1 - execution of request r0
S2 - execution of request r1
S3 - execution of request r2
S4 - execution of request r3

1b56.

a. data_out[0] = (data_in == 8'b0000_0010)
|| (data_in == 8'b0000_1000)
|| (data_in == 8'b0001_0000)
|| (data_in == 8'b1000_0010)

Therefore the answer will look like this.
assign data_out[0] = data_in[1] | data_in[3] | data_in[5] | data_in[7];

b. assign data_out[1] = data_in[2] | data_in[3] | data_in[6] | data_in[7];

c. assign data_out[2] = data_in[4] | data_in[5] | data_in[6] | data_in[7];

1b57.

In1, In2	P(0) at X net	P(1) at X net	Switching activity
AB	0.4	0.6	0.24
AC	0.45	0.55	0.248
BC	0.72	0.28	0.201

a. BC
b. AC
c. 0.201, 0.248

1b58.

a. $P(Y=0)=n_0/2^n=4/8=0.5$, n_0 is the number of rows in the truth table with Y=0, n is the number of inputs; $P(Y=1)=0.5$; $P_{0\text{-}1}=0.5*0.5=0.25$; $P_{1\text{-}0}=0.5*0.5=0.25$.
b. P(Y=1)=P(A=1)P(B=1)P(C=1)+ P(A=1)P(B=0)P(C=0)+ P(A=0)P(B=1)P(C=0)+ +P(A=0)P(B=0)P(C=1)=0.2*0.4*0.8+0.2*0.6*0.4+0.8*0.4*0.4+0.8*0.6*0.6=0.512; P(Y=0)=1- -P(Y=1)=0.488; $P_{0\text{-}1}=0.488*0.512=0.249856$; $P_{1\text{-}0}=0.512*0.488=0.249856$.

1b59.
!X=!(((!A+!B)(!C+!D+!E)+!F)!G)=!(!(AB)!(CDE)+!F)+G=)=!(!(AB)!(CDE) F+G=(AB+CDE)F+G
PMOS: $(W/L)_G=6*2=12$, $(W/L)_F=6*2/2=6$, $(W/L)_{CDE}=6*2/3=4$, $(W/L)_{AB}=6*2/2=6$
NMOS: $(W/L)_G=2/2=1$, $(W/L)_F=1*2=2$, $(W/L)_{CDE}=2*3/2=3$, $(W/L)_{AB}=2*2/2=2$

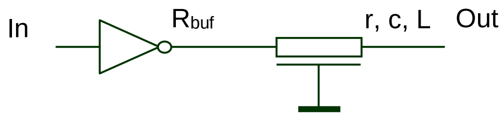
1b60.
$P_1=V_{DD}^2C_{load1}F=V_{DD}^2F(C_{out}+C_{in})=800\cdot10^6\cdot25\cdot10^{-15}=20uW$
$P_2=V_{DD}^2C_{load2}F=V_{DD}^2F(C_{out}+C_{load})=800\cdot10^6\cdot110\cdot10^{-15}=88uW$
$P=P_1+P_2=108uW$.

1b61.
$C_{ox}=\varepsilon_0\varepsilon_{ox}/Tox=8.85\cdot10^{-12}\,3.97/1.5\cdot10^{-8}=2.34fF/um2$
$\beta_n=\mu_nC_{ox}(W/L)_n=550\ sm^2/Vs\cdot2.34fF/um^2\cdot14=1.8mA/V^2$
$\beta_p=\mu_pC_{ox}(W/L)_n=180\ sm^2/Vs\cdot2.34fF/um^2\cdot12=0.505mA/V^2$

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{4\beta_p}} V_{Tn} + (V_{DD} - V_{Tp})}{1 + \sqrt{\frac{\beta_n}{4\beta_p}}}$$

V_{SP}=((1.8/(4·0.505))$^{0.5}$·0.7+3.3-0.8)/(1+(1.8/(4·0.505))$^{0.5}$)=(0.94·0.7+2.5)/1.94=1.63V

1b62.

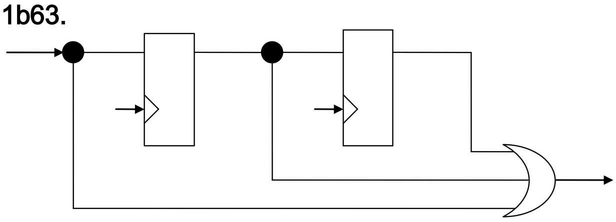


c=c_{ov}W+c_{fg}=30Ē0.5+40=55 aF/u,
r=R_{sh}/W=0.08/0.5=0.16 Ohm/u,
C=Lc=22500 aF,
R=Lr=80 Ohm,
t_D=0.7(R_{buf}+R)C=0.7(R_{buf}+Lr)cL=0.7(100+500*0.16)500*55 =3465000 as=3.465 ps,

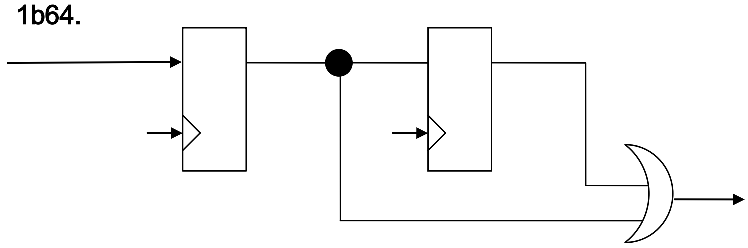
$$t_D = 0.7(rc\frac{L^2}{2} + L\cdot c\cdot R_{buf}) = 0.7(0.16\cdot 55\cdot \frac{500^2}{2} + 500\cdot 55\cdot 100) = 269.5\cdot 10^4 as = 2.695 ps$$

$$t_{DN} = 0.7(C\cdot Rbuf + RC\frac{N+1}{2N}) = 0.7(27500\cdot 100 + 80\cdot 27500\frac{11}{20}) = 2772000 as = 2.772 ps$$

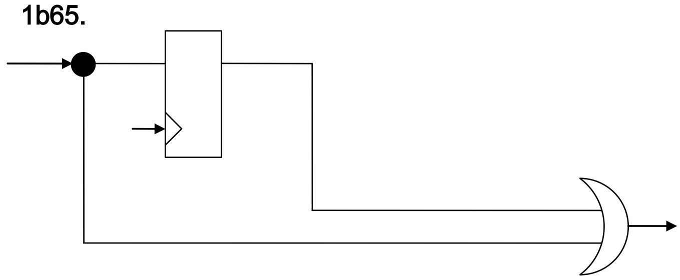
1b63.



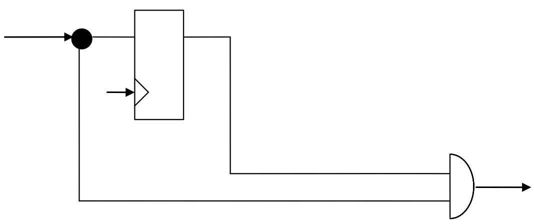
1b64.



1b65.



1b66.



1b67.

The assignment of counter states is the following: S0 – 00, S1 – 01, S2 – 10. The code 11 is not used. The matrix of excitation functions is represented below.

Transition	J	K
$0 \to 0$	0	-

$0 \rightarrow 1$	1 -
$1 \rightarrow 0$	- 1
$1 \rightarrow 1$	- 0

The table of excitation functions of JK flip-flops is given below.
q1, q2 – flip-flops outputs.

State	q1 q2	J1 K1	J2 K2
S0	0 0	0 -	1 -
S1	0 1	1 -	- 1
S2	1 0	- 1	0 -

Repeated States

The minimization of excitation functions is performed using Karnaugh maps.

J1

q1 \ q2	0	1
0		1
1	-	-

K1

q1 \ q2	0	1
0	-	-
1	1	-

J2

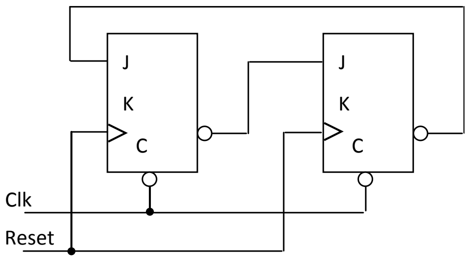
q1 \ q2	0	1
0	1	-
1		-

K2

q1 \ q2	0	1
0	-	1
1	-	-

J1= q2; K1= K2=1; J2= $\bar{q}1$;

On the basis of these expressions the following circuit is constructed.



1b68.

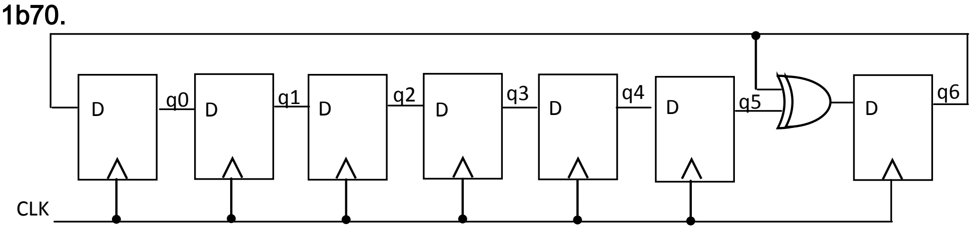
```
module Mealy_fsm (in,yout, clk, reset);
       input in, clk, reset;
       output yout;
       reg yout;
       reg [1:0] state, next_state;
              // state register
              always  @(posedge clk or negedge reset)
                     if (!reset)
                     state<= 2’b00;
                     else state<=next_state;
                     //next_state logic
              always @(in or state)
              case (state)
                     2’b00: next_state=in? 2’b10: 2’b01;
                     2’b01: next_state=in? 2’b00: 2’b10;
                     2’b10: next_state=in? 2’b01: 2’b00;
                     default: next_state=2’b00;
              endcase
                     //output logic
always @(in or state)
              case (state)
                     2’b00: yout=in;
```

```
                  2'b01, 2'b10: yout=1;
            default: yout=0;
            endcase
endmodule
```

1b69.

```
module up_down_counter(up, down, clk, reset, count);
      parameter N=8;
      input up, down, clk,reset;
      output [N-1:0] count;
      reg [N-1:0] count;
            always @(negedge clk)
            if(reset) count<=0;
            else
            case ({up, down})
      0: count<=count;
      1: count<=count-1;
      2: count<= count+1;
      default: count<=0;
            endcase
endmodule
```

1b70.



Galois LFSR Description in Verilog

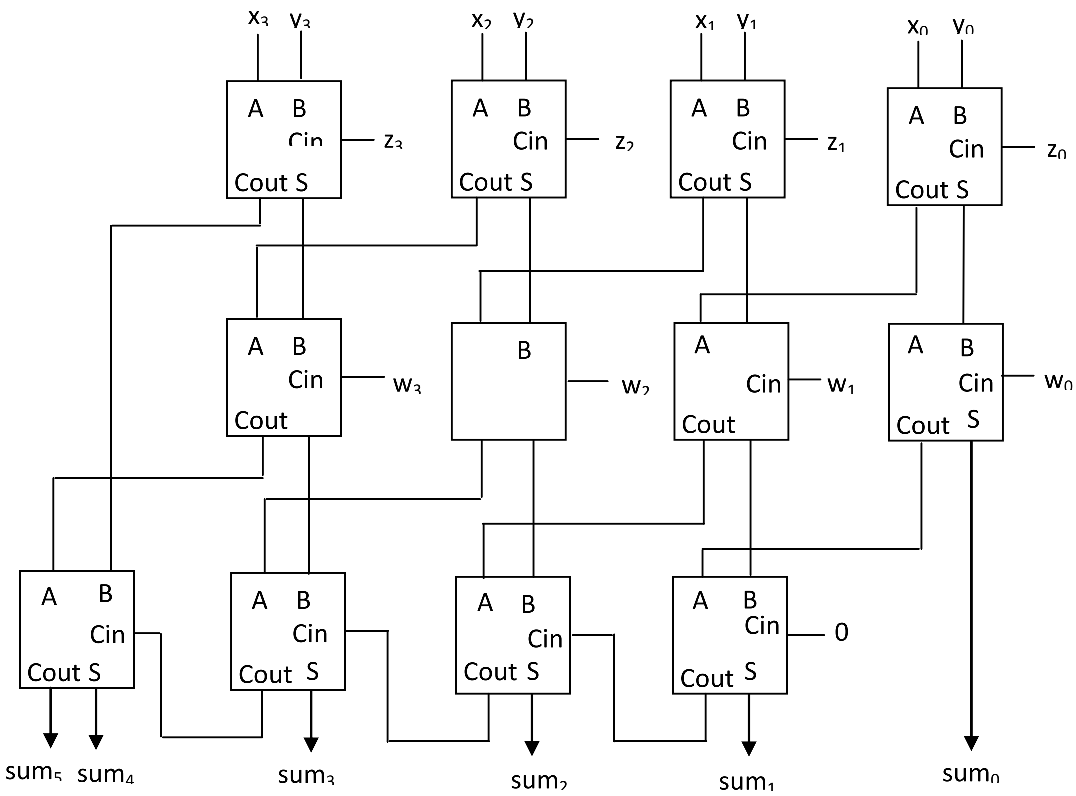
```
module Galois_LFSR(clk,  load, en, q, data);
      input clk, load, en;
      input [0:6] data;
      output reg [0:6] q;
      always @(posedge clk or posedge load)
      begin
      if (load)  q<=data; //can be anything except zero
      else if (en)
      q<={q[6],q[0:4], q[6]^q[5]};
      end
      endmodule
```

1b71.

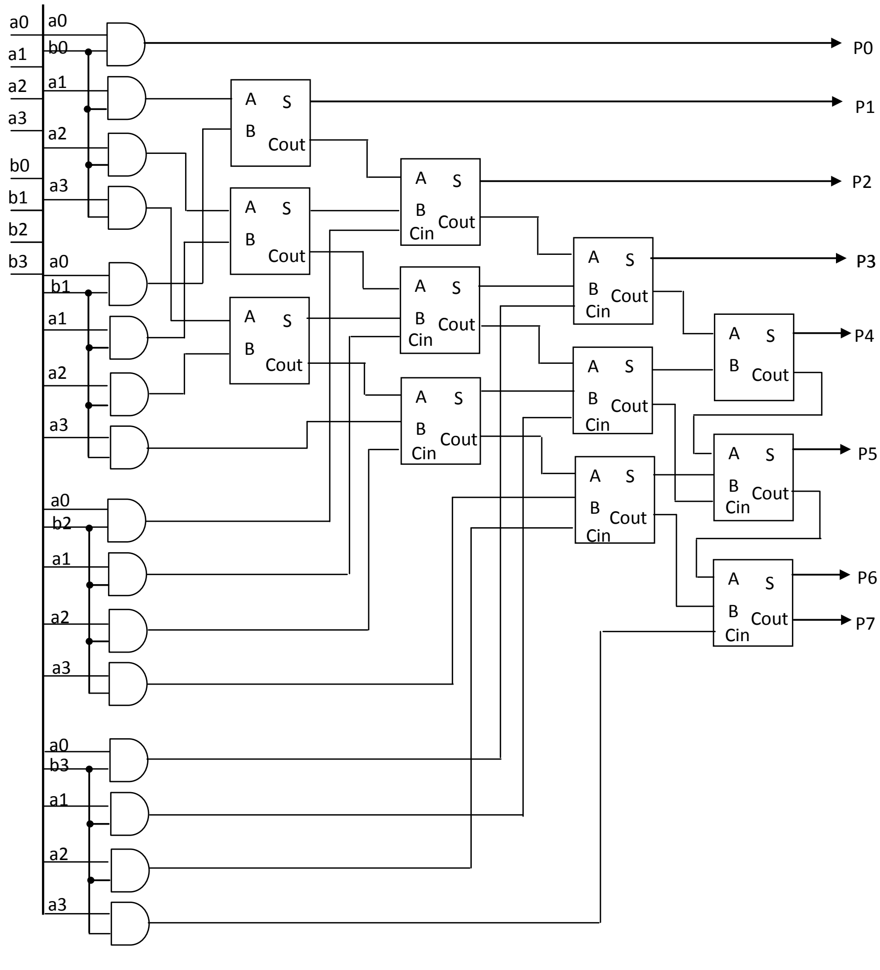
```
module ALU (A, B, F, Y);
      parameter n=8;
      input [n-1:0] A,B;
      input[2:0] F;
      output [n-1:0] Y;
      reg [n-1:0] Y;
            always @(A or B or F)
                  begin
                        case (F)
                  0: Y= A&B;
                  1: Y= A|B;
                  2: Y= A+B;
                  4: Y= A^B;
                  5: Y= A-B;
                  6: Y= A| (~B);
                  7: Y = ~A;
                  default: Y=0;
                        endcase
                  end
endmodule
```

1b72.

S= X + Y + Z +W



1b73.

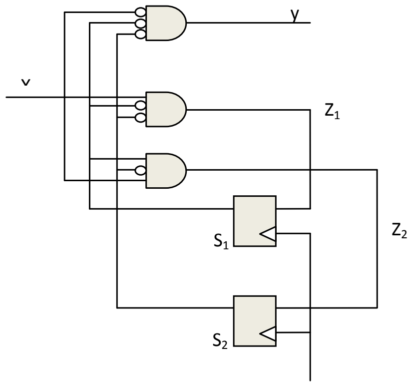


1b74.

$Z_1 = \overline{S_1}\ \overline{S_2}\ X$

$Z_1 = S_1\ S_2\ X$

$Y = \overline{S_1}\ \overline{S_2}\ \overline{X}$

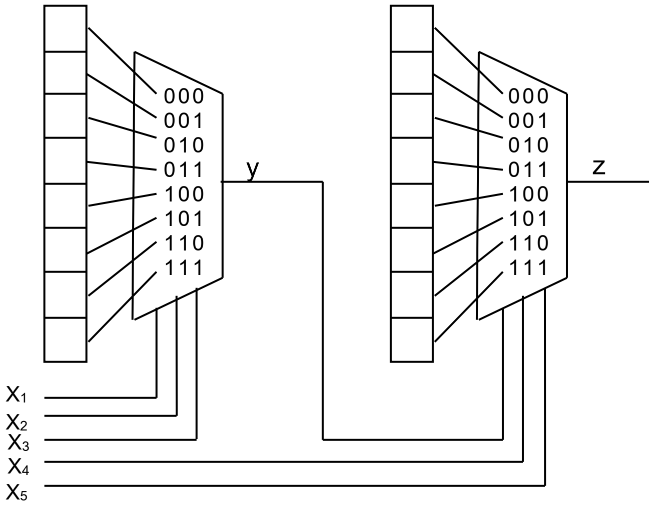


1b75.

	x=0	x=1
S_1	S_2/0	S_1/0
S_2	S_4/1	S_1/1
S_3	S_2/1	S_4/1
S_4	S_2/0	S_2/1

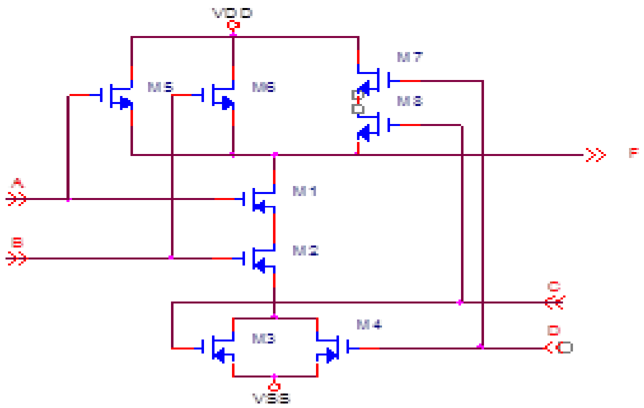
S_3 cannot be reached.

1b76.



1b77.

a)

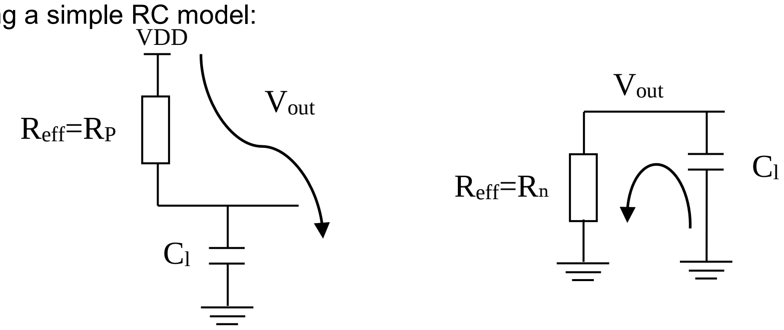


b)

M1, M2, M3, M4: Wn/Ln=3*6□/2□
M5, M6: Wp/Lp=3*6□/2□
M7, M8: Wp/Lp=6*6□/2□

1b78.
a)
C_{in1}=10C
C_{in2}=X*C,
C_{in3}=Y*C
Branching factors at nodes B and C are b_B=4X/X=4; b_C=3Y/Y=3.
Total branching on path A-D is B= b_B* b_C=12.
Logical effort on path A-D: G=g_1*g_2*g_3=(4/3)*3*(5/3)=20/3
Total electrical effort on path A-D: H=C_{LOAD}/C_{in}=27C/(10C)=27/10
Total stage effort on path A-D: F=B*G*H=12*(20/3)*(27/10)=216
Particular stage effort f_i=$(F)^{1/3}$=6
Total parasitic delay on path A-D: P=p_1+p_2+p_3=9
Total normalized minimal delay on path A-D: D=P+3* f_i=9+18=27
b)
Particular stage effort for each stage is
f_i=$(F)^{1/3}$=6= f_1= f_2=f_3.
NAND3
h_3=C_{3out}/C_{3in}=(27*C)/(Y*C)= 27/Y
f_3= g_3*h_3=g_3*(27/Y)=> Y=g_3*27/f_3=(5/3)*27/6=15/2
W_{pNAND2}=W_{nNAND2}=2W_{no} for NAND3 comparable with unit inverter
C_{ino}=4C (2C from pMOS and 2C from nMOS)
K=C_{1in}/C_{ino}=10C/4C=2.5
Wp=Wn=2.5W_{no}
NOR4
h_2=C_{2out}/C_{2in}=(3*Y*C)/(X*C)= 3*Y/X
f_2= g_2*h_2=g_2*(3*Y/X)=> X=g_2*3*Y/f_2=(3)*(3*15/2)/6=45/4
W_{pNOR4}=8W_{no} ; W_{nNOR4}=W_{no} for NOR4 comparable with unit inverter
C_{ino}=9C (8C from pMOS and 1C from nMOS)
K=C_{2in}/C_{ino}=(45/4)C/(9C)=5/4
Wp=8*(5/4)*W_{no}=10*W_{no}
Wn=1*(5/4)*W_{no}
NAND2:
W_{pNAND2}=W_{nNAND2}=2W_{no} for NAND2 comparable with unit inverter
C_{ino}=4C (2C from pMOS and 2C from nMOS)
K=C_{1in}/C_{ino}=10C/4C=2.5
Wp=Wn=2.5W_{no}
check for NAND2
h_1=C_{1out}/C_{1in}=(4*X*C)/(10*C)= 4*(45/4)/10=45/10=9/2
f_1= g_1*h_1=(4/3)*9/2=6

1b79.
a)
Assuming a simple RC model:



t_{PHL} = $0.7R_NC_L$ = 50ps $\Rightarrow$ R_N = $t_{PHL}/(0.7\times C_L)$ = $R_{eqn} \times L/W_n$ $\Rightarrow$ W_n =875nm
t_{PLH} = $0.7R_PC_L$ = 70ps $\Rightarrow$ R_P = $t_{PLH}/(0.7\times C_L)$ = $R_{eqp} \times L/W_p$ $\Rightarrow$ W_p =1500nm
b)

Consider the Vs equation:

$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1+\chi}$$

$$\chi = \sqrt{\frac{\mu_{en} W_N}{\mu_{ep} W_P}} = \sqrt{2.25} = 1.5$$

$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1+\chi} = \frac{1.2 - 0.4 + 1.5 * 0.4}{1+1.5} = 0.56$$

c)

Vs = Vdd/2 $\Rightarrow$ X = 1

$$\chi = \sqrt{\frac{\mu_{en} W_N}{\mu_{ep} W_P}} = 1 \Rightarrow W_p = \frac{\mu_{en} W_N}{\mu_{ep}} = 3375\text{nm}$$

t_{PHL} = $0.7 R_N C_L$ = 50ps

t_{PLH} = $0.7 R_P C_L$ = 70ps $\Rightarrow$ $R_P = t_{PLH}/(0.7 \times C_L) = R_{eqp} \times L/W_p \Rightarrow W_p$ =1500nm

$$t_{PLH} = 0.7 \cdot R_{eqp} \cdot \frac{L}{W_p} \cdot C_L = 31\text{ps}$$

1b80.

a)

First calculate the path effort:

$$PE = LE_{inv} BE_{inv} \frac{C_{nand}}{C_{in}} \times LE_{nand} \frac{C_{inv2}}{C_{nand}} \times LE_{inv} \frac{C_{nor}}{C_{inv2}} \times LE_{nor} \frac{C_{inv3}}{C_{nor}} \times LE_{inv} \frac{C_{load}}{C_{inv3}}$$

$$= 1 \times 2 \times \frac{5}{3} \times 1 \times \frac{9}{3} \times 1 \times \frac{200}{20} = 100$$

$$SE = LE_{inv} BE_{inv} \frac{C_{nand}}{C_{in}} = LE_{nand} \frac{C_{inv2}}{C_{nand}} = LE_{inv} \frac{C_{nor}}{C_{inv2}} = LE_{nor} \frac{C_{inv3}}{C_{nor}} = LE_{inv} \frac{C_{load}}{C_{inv3}}$$

$$= \sqrt[5]{PE} = \sqrt[5]{100} = 2.51$$

$$C_{inv3} = LE_{inv} \times \frac{C_{load}}{SE} = 80\text{fF} \Rightarrow W = \frac{C_{inv3}}{3C_g} = 13.34\text{um}$$

$$C_{nor} = LE_{nor} \times \frac{C_{inv3}}{SE} = 96\text{fF} \Rightarrow W = \frac{C_{nor}}{9C_g} = 5.34\text{um}$$

$$C_{inv2} = LE_{inv} \times \frac{C_{nor}}{SE} = 38.2\text{fF} \Rightarrow W = \frac{C_{inv2}}{3C_g} = 6.37\text{um}$$

$$C_{nand} = LE_{nand} \times \frac{C_{inv2}}{SE} = 25.36\text{fF} \Rightarrow W = \frac{C_{nand}}{5C_g} = 2.53\text{um}$$

$$C_{in} = LE_{inv} \times BE_{inv} \times \frac{C_{nand}}{SE} = 20\text{fF} \Rightarrow W = \frac{C_{in}}{3C_g} = 3.34\text{um}$$

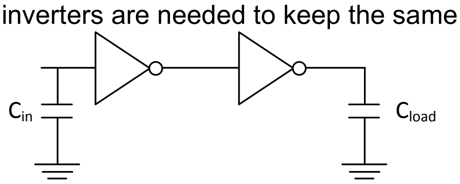
$$D = N_{stages} (PE)^{1/N_{stages}} + P_{inv} + P_{nand} + P_{inv} + P_{nor} + P_{inv}$$

$$= 5\left(1 \cdot 2 \cdot \frac{5}{3} \cdot 1 . \frac{9}{3} . 1 . \frac{200}{20}\right)^{1/5} + 0.5 + 1.5 + 0.5 + 2 + 0.5 = 17.5$$

$$\text{Delay} = D \times t_{inv} = 17.5 \times 7.5\text{ps} = 131\text{ps}$$

b)

Two inverters are needed to keep the same functionality, the C_{load} is equal to C_{nand}:



C_{load} = 2*C_{nand} = 51fF and C_{in} = 20fF

$$PE = LE_{inv} \frac{C_{invA}}{C_{in}} \times LE_{inv} \frac{C_{load}}{C_{invA}} = 1 \times 1 \times \frac{51}{20} = 2.55$$

$$SE = LE_{inv}\frac{C_{invB}}{C_{in}} = LE_{inv}\frac{C_{load}}{C_{invB}} = \sqrt{PE} = 1.6$$

$$C_{invB} = LE_{inv}\times\frac{C_{load}}{SE} = 31.87fF => W = \frac{C_{invB}}{3C_g} = 5.3um$$

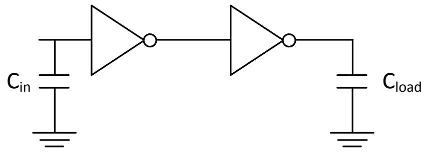
$$C_{invA} = LE_{inv}\times\frac{C_{invB}}{SE} = 20fF => W = \frac{C_{invA}}{3C_g} = 3.34um$$

$$D = N_{stages}(PE)^{1/N_{stages}} + P_{inv} + P_{inv} = 2\left(1.1.\frac{51}{20}\right)^{1/2} + 0.5 + 0.5 = 4.2$$

$$Delay = D\times t_{inv} = 4.2\times 7.5ps = 31ps$$

c)

$C_{inw} = C_{inx} = C_{iny} = C_{inz} = C_{nand} = 25.36fF$



C_{in} = 10fF; and $C_{load} = C_{nand}$ = 25.36fF

$$PE = LE_{inv}\frac{C_{invA}}{C_{in}}\times LE_{inv}\frac{C_{load}}{C_{invA}} = 1\times 1\times\frac{25.36}{10} = 2.536$$

$$SE = LE_{inv}\frac{C_{invB}}{C_{in}} = LE_{inv}\frac{C_{load}}{C_{invB}} = \sqrt{PE} = 1.6$$

$$C_{invl2} = LE_{inv}\times\frac{C_{load}}{SE} = 15.85fF => W = \frac{C_{invl2}}{3C_g} = 2.64um$$

$$C_{invl1} = LE_{inv}\times\frac{C_{invB}}{SE} = 10fF => W = \frac{C_{invA}}{3C_g} = 1.67um$$

1b81.

a)

ρ_{Cu} = 1.7uΩ-cm, L = 40mm, C_g = 2fF/um, C_{eff} = 1fF;

W = 0.17um, T = 0.8um, Cint = 0.2fF/um, R_{eqn} = 12.5kΩ/[]

For a minimum sized inverter => Wn=0.1um (this is because Rn = R_{eqn} = 12.5kΩ/[] is used otherwise if Wn=0.2um is used, Rn = R_{eqn} /2= 6.25kΩ/[]) has to be used.

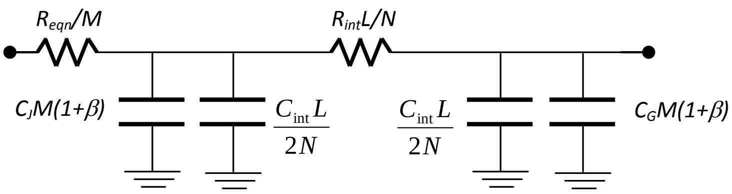
C_G = 0.1um*2fF/um = 0.2fF; and C_J = 0.1um*1fF/um = 0.1fF

$$R_{int} = \frac{\rho_{Cu}}{TW} = \frac{1.7u\Omega - cm}{0.8um\times 0.17um} = 125m\Omega/um$$

$$N = \sqrt{\frac{R_{int}C_{int}L^2/2}{R_{eqn}(C_G + C_J)(1+\beta)}} = \sqrt{\frac{125m\Omega/um.0.2fF/um.(28000um)^2/2}{12.5k\Omega(0.2fF+0.1fF)(1+2)}} \cong 30$$

$$M = \sqrt{\frac{R_{eqn}C_{int}}{C_G(1+\beta)R_{int}}} = \sqrt{\frac{12.5k\Omega.0.2fF/um}{C_G(1+2)\cdot 125m\Omega/um}} \cong 183$$

b)



RC Π Model for one segment

ρ_{Cu} = 1.7um-cm, L = 28mm, C_g = 2fF/um, C_{eff} = 1fF;

W = 0.17um, T = 0.8um, Cint = 0.2fF/um, Wn = 0.1μm, R_{eqn} = 12.5kΩ/[]

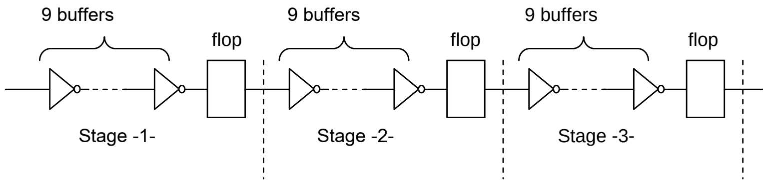
M = 140; N = 55; R_{int} = 212.5kΩ

$$t_{segment} = \frac{R_{eqn}}{M}\left(C_J M(1+\beta) + \frac{C_{int}L}{2N}\right) + \left(\frac{R_{eqn}}{M} + \frac{R_{int}L}{N}\right)\left(\frac{C_{int}L}{2N} + C_G M(1+\beta)\right) = 47.7ps$$

$$t_{total} = N\times t_{segment} = 1.43ns$$

t_{total} = 1.43ns which means that the maximum frequency is 0.7GHz.

For the segment delay, the maximum frequency is about 21GHz.
In order to run this logic at 2GHz, there should be pipelining. To figure out the number of pipeline stages:
$t_{segment}$ = 47.7ps ≈ 50ps (assume worst case) and the required time cycle is $t_{required}$ = 0.5ns = 500ps, define K as the number of stages which can be covered by $t_{required}$
k = 500ps / 50ps = 10.
Consider K to be 10, i.e. the 10^{th} buffer in every 10 stages of the original design should be replaced by a flipflop that has the identical fanout ratio.
Number of pipelines needed is:
N/K = 30/10 = 3. So 3 flip-flops are needed to replace the buffer after every 9 segments to pipeline and make this wire run at 2GHz.



Final schematic

To recalculate the buffers: 3 × 9 + 3 (flops with identical fanout as buffers) = 30 = N

1b82.

The static power consumed due to sub-threshold leakage (given Vgs = 0):

$$P_{static} = \left(I_s e^{\frac{q(V_{gs}-V_t-V_{offset})}{nkT}} \left(1 - e^{\frac{-qV_{ds}}{kT}} \right) \right).V_{DD} = \left(I_s e^{\frac{-qV_t}{nkT}} \left(1 - e^{\frac{-qV_{ds}}{kT}} \right) \right).V_{DD}$$

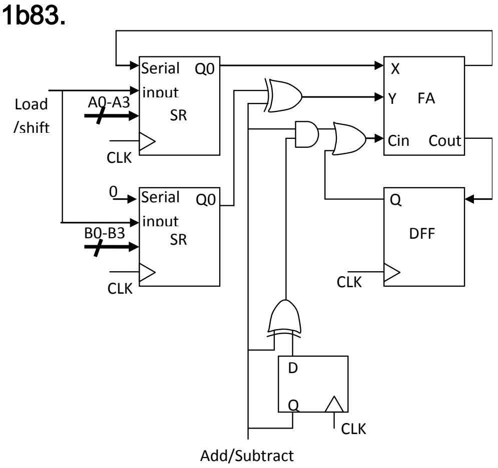
The ratio of the slow to the typical (considering Vt = 0.4 – 0.00002*(100) = 0.398V)

$$\frac{P_{slow}}{P_{typical}} = \frac{\left(I_s e^{\frac{-qV_{tS}}{nkT_S}} \left(1 - e^{\frac{-qV_{dsS}}{kT_S}} \right) \right).V_{DDs}}{\left(I_s e^{\frac{-qV_{tT}}{nkT_T}} \left(1 - e^{\frac{-qV_{dsT}}{kT_T}} \right) \right).V_{DDT}} = 39.7$$

The ratio of the fast to the typical (considering Vt = 0.4 – 0.00002*(-30) = 0.4006V)

$$\frac{P_{Fast}}{P_{typical}} = \frac{\left(I_s e^{\frac{-qV_{tF}}{nkT_F}} \left(1 - e^{\frac{-qV_{dsF}}{kT_s}} \right) \right).V_{DDF}}{\left(I_s e^{\frac{-qV_{tT}}{nkT_T}} \left(1 - e^{\frac{-qV_{dsT}}{kT_T}} \right) \right).V_{DDT}} = 0.21$$

1b83.

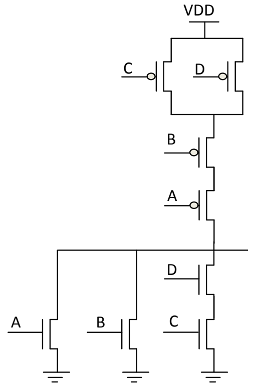


1b84.

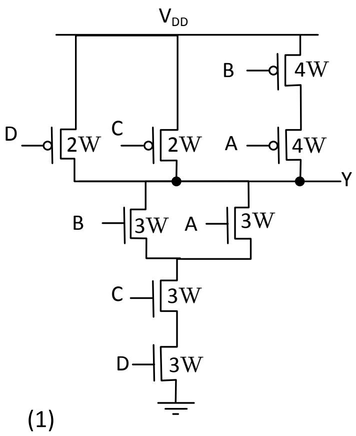
A (I0)	B (I1)	C (I2)	D (I3)	Y1	Y0	IDLE	W	X	Y	Z
0	0	0	0	0	0	1	0	0	0	0
0	0	0	1	1	1	0	0	0	0	1
0	0	1	0	1	0	0	0	0	1	0
0	0	1	1	1	0	0	0	0	1	0
0	1	0	0	0	1	0	0	1	0	0

0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	1	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	1	0
1	0	0	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0
1	0	1	0	1	0	0	0	0	1	0
1	0	1	1	1	0	0	0	0	1	0
1	1	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	1	0	0	0
1	1	1	0	1	0	0	0	0	1	0
1	1	1	1	1	0	0	0	0	1	0

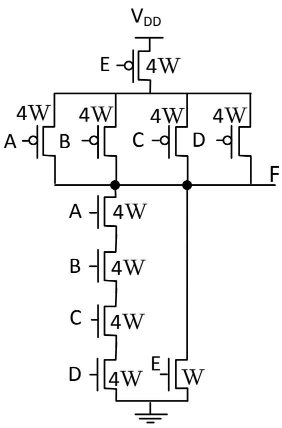
1b85.



1b86.
a)



(1)



(2)

b)
Gate (1):
$C_{inA} = C_{inB} = C_g(W_n+W_p) = C_g(3W+4W) = C_g(7W) = 2fF/\mu m\ (7*0.2\mu m) = 2.8fF$
$C_{inC} = C_{inD} = C_g(W_n+W_p) = C_g(3W+2W) = C_g(5W) = 2fF/\mu m\ (5*0.2\mu m) = 2.0fF$
Gate (2):
$C_{inA} = C_{inB} = C_{inC} = C_{inD} = C_g(4W+4W) = C_g(8W) = 2fF/\mu m\ (8*0.2\mu m) = 3.2fF$
$C_{inE} = C_g(W_n+W_p) = C_g(W+4W) = C_g(5W) = 2fF/\mu m\ (5*0.2\mu m) = 2.0fF$
c)
Gate (1):
$C_{self} = C_{eff}(W_{nA}+ W_{nB} + W_{pD} + W_{pC} + W_{pA}) = C_{eff}(3W+3W+2W+2W+4W) = C_{eff}(14W) = 1fF/\mu m\ (14*0.2\mu m) = 2.8fF$
Gate (2):
$C_{self} = C_{eff}(W_{nA}+ W_{nE} + W_{pA} + W_{pB} + W_{pC} + W_{pD}) = C_{eff}(4W+W+4W+4W+4W+4W) = C_{eff}(21W) = 1fF/\mu m\ (21*0.2\mu m) = 4.2fF$

1b87.
```
reg [2:0] counter;
reg [3:0] internal_counter;
always @ (posedge clk or negedge reset) begin
    if (!reset) begin
        internal_counter <= 3'd0;
```

```
        end
        else if (internal_counter == 3'd11) begin
            internal_counter <= 3'd0;
        end
        else begin
            internal_counter <= internal_counter + 3'd1;
        end
    end
    always @ (posedge clk or negedge reset) begin
        if (!reset) begin
            counter <= 3'd0;
        end
        else if (     ((internal_counter > 3'd3) && (internal_counter < 3'd8))
                      || (internal_counter > 3'd9)
                  ) begin
            counter <= counter - 3'd1;
        end
        else begin
            counter <= counter + 3'd1;
        end
    end
```

1b88.

```
    reg [2:0] counter;
    reg [1:0] internal_counter;
    always @ (posedge clk or negedge reset) begin
        if (!reset) begin
            internal_counter <= 2'd0;
        end
        else if (internal_counter == 2'd2) begin
            internal_counter <= 2'd0;
        end
        else begin
            internal_counter <= internal_counter + 2'd1;
        end
    end
    always @ (posedge clk or negedge reset) begin
        if (!reset) begin
            counter <= 3'd0;
        end
        else if (internal_counter[1]) begin  // which means (internal_counter > 2'd1)
            counter <= counter - 3'd1;
        end
        else begin
            counter <= counter + 3'd1;
        end
    end
```

1b89.

```
    reg [2:0] counter;
    reg [1:0] internal_counter;
    wire increment_internal_counter = (({1'b0,internal_counter} + 3'd1) == counter);
    always @ (posedge clk or negedge reset) begin
        if (!reset) begin
            internal_counter <= 2'd0;
        end
        else if (increment_internal_counter) begin
            internal_counter <= internal_counter + 2'd1;
        end
        else begin
            internal_counter <= internal_counter; // keep the same value
        end
    end
    always @ (posedge clk or negedge reset) begin
        if (!reset) begin
            counter <= 3'd0;
        end
        else if (increment_internal_counter) begin
            counter <= 3'd0;
        end
        else begin
```

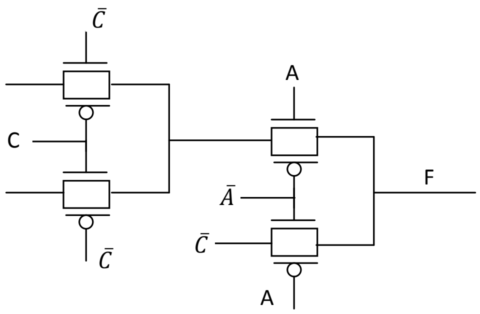
```
            counter <= counter + 3'd1;
        end
    end
```

1b90.

```
reg [2:0] counter;
reg [2:0] internal_counter;
always @ (posedge clk or negedge reset) begin
    if (!reset) begin
        internal_counter <= 3'd0;
    end
    else if (internal_counter == 3'd6) begin
        internal_counter <= 3'd0;
    end
    else begin
        internal_counter <= internal_counter + 3'd1;
    end
end
always @ (posedge clk or negedge reset) begin
    if (!reset) begin
        counter <= 3’d0;
    end
    else if (internal_counter > 3'd4) begin
        counter <= counter – 3'd1;
    end
    else begin
        counter <= counter + 3'd1;
    end
end
```

1b91.

Modify the given function into $F=AB+AC+\bar{A}\bar{C}$ form, implement the function in the structure of dual 4:1 multiplexor, using A and C as selection variables.



1b92.

ABCD	Z	ABCD	Z
0000	0	1000	0
0001	0	1001	0
0010	0	1010	0
0011	1	1011	1
0100	0	1100	1
0101	0	1101	1
0110	0	1110	1
0111	1	1111	1

$P_1=7/16$; $P_0=9/16$

$P_{01} = P_0\bar{E}\, P_1=7/16*9/16=63/256=0.246$

1b93.

For static implementation, energy is consumed in case of 01 transitions of outputs, for dynamic implementation – when the previous state of the output is 0.

$P=P_{01}V_{DD}^2C\bar{E}F$

a) $P= P_{01AND}V_{DD}^2C\bar{E}F+ P_{01AND}V_{DD}^2C\bar{E}F+ P_{01MUX}V_{DD}^2C\bar{E}F=(3/16+3/16+1/4)\bar{E}2.5^2\,\bar{E}0.3\bar{E}10^{\ 12}\bar{E}100\bar{E}10^6=$
$=1.17\bar{E}10^{-4}$ W,

b) $P= P_{0AND}V_{DD}^2C\bar{E}F+ P_{0AND}V_{DD}^2C\bar{E}F+ P_{0MUX}V_{DD}^2C\bar{E}F=(3/4+3/4+1/2)\bar{E}2.5^2\,\bar{E}0.3\bar{E}10^{-12}\bar{E}100\bar{E}10^6=$
$=3.75\bar{E}10^{-4}$ W.

1b94.

The same current flows through both transistors. V_x<4V, the transistor below is not saturated: $V_{DS}<V_{GS}-V_T$, and the transistor above is saturated: $V_{DS}=V_{GS}=5-V_x$.

$$\frac{1}{2}[V_{GS} \;\; - V_t]^2 = [V_{GS} \;\; - V_{t0} - \frac{V_{DS2}}{2}]V_{DS2}$$

$$V_t = V_{t0} + \gamma(\sqrt{2\,|\,\Phi_F\;| + V_{SB}} - \sqrt{2\,|\,\Phi_F\;|}) = 1 + 0.39(\sqrt{1.2 + V_x} - \sqrt{1.2})$$

$$\frac{1}{2}[5 - V_x - (1 + 0.39(\sqrt{1.2 + V_x} - \sqrt{1.2}))]^2 = [5 - 1 - \frac{V_x}{2}]V_x$$

Solving this equation, for example by graphical method, this is obtained: V_x=1.09V.

Taking W/L=1,

$$I_D = K_P[5 - 1 - \frac{V_x}{2}]V_x = 25 \cdot (4 - 0.24) \cdot 0.48 = 45.12mk$$

1b95.

Switching point voltage is computed by the following formula:

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn} + (V_{DD} - V_{Tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Putting switching point and threshold values, denoting β_n/β_p ratio by x^2, this is obtained:

1.2=(0.5x+(3.0-0.7))/(1+x), x=1.57, $\beta_n/\beta_p=x^2=2.47$,

$\beta_n/\beta_p = (W_n k_{pn}/L_n)/(W_p k_{pp}/L_p) = (W_n k_{pn})/(W_p k_{pp}) = (W_n \mu_n)/(W_p \mu_p) = 3W_n/W_p = 2.47$

$W_p=3W_n/$ 2.47=3Ē 0.5/2.47=0.61 mkm

1b96.

Represent the function in the following form:

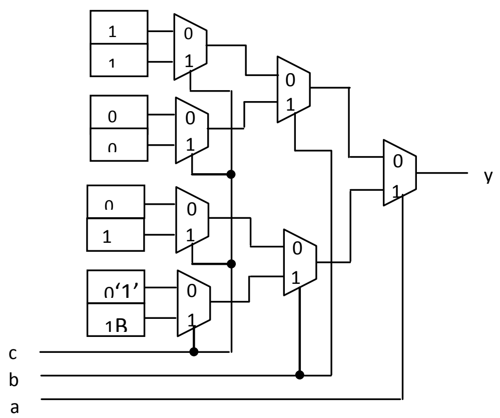
f(a, b,c) =~a·~b + a·c + b·c = a·~b + (a+b)·c: On the basis of this expression, the block can be programmed as follows:

f(a,b,c) = (a+b)·Mux1 + (a+b)·Mux2 = (a+b)·c +~a~b.

1b97.

Implement a function of three variables f(a,b,c) = a·c + ~a·~b. The scheme on the 2:1 multiplexer corresponds to BDD function. To solve the problem, set up a table of the given function. Then, transfer the values of the given function to the scheme on multiplexers.

a b c	f
0 0 0	1
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	0
1 0 1	1
1 1 0	0
1 1 1	1



1b98.

Analyze the given scheme.

d1 = ~q1; d2 = q1; t3= q2;

Define the characteristic equation of flip-flops: q1*, q2*, q3*.

q1* = d1 =~q1; q2* = d2 = q1; q3* = t3⊕q3= q2⊕q3;

On the basis of the characteristic equations, the sequence of states of the scheme is defined.

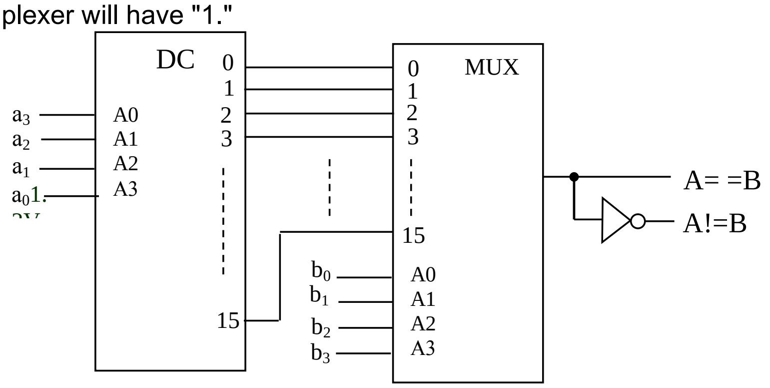
Table of states of the scheme will have the following form:

q1 q2 q3
0 0 0
0 1 0
1 0 1
0 1 1
1 0 0
0 1 0

After the state 010, the sequence of states is repeated.

1b99.

Code of one of the numbers, for example A, is given to the input of the decoder, implementing all the minterms of the function of four variables. To construct a scheme, outputs Yi should be connected to the inputs of Di multiplexer which have the same name. The code of the second number is given to address inputs of the multiplexer (in this case B). At coincidence of the codes of numbers A and B, the output of the multiplexer will have "1."



1b100.

First transistor groups that connect load transistor with grounding are defined (1 and 3 groups in Figure a). Afterwards taking the sequential or parallel connections of transistors into account, the graph model of logic connections of the circuit is built (Figure b). The logic circuit, corresponding to the obtained graph model is shown in Figure c.

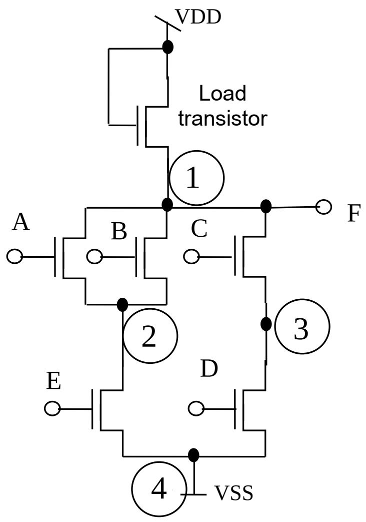
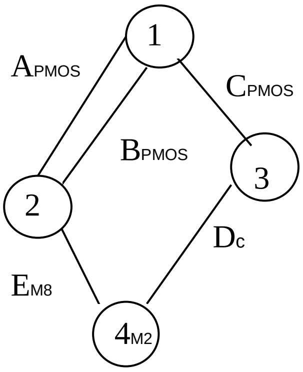
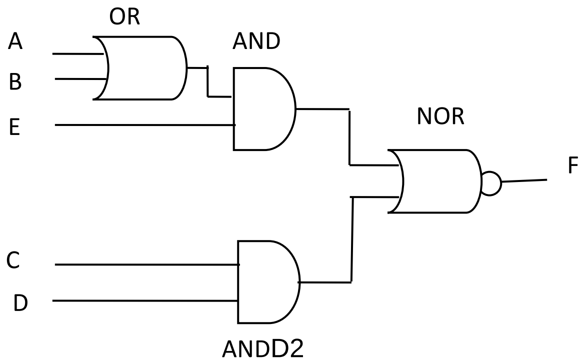


Figure a





1b1

Figure b

Figure c

Logic 1 is given to C input of D FF. Therefore it level repeater, given to D input. In this case there is 0 in its direct output, and 1 in its inv 0 will be formed in the output of “XOR” cell, as the input levels are the same. As there are logic 0s in all address inputs of the decoder, A input signal will be repeated in its 0 output. There will be logic level 1 in all the remaining outputs.

1b102.

Logic 1 is always given to the input of an adder with 1 weight. For the LED to light it is necessary to have logic 0 in the output of the adder with 16 weight, i.e. A+ B ̃ +1<16 inequality occurs. As B̃=15−B, putting it in the previous inequality, it will turn out that the LED is lit in case of A < B condition.

1b103.

4-bit binary up counter with 16 coefficient is presented. It can change its states from 0 to 15. After getting 16 impulses to the input of a counter, it will again appear in 7 states. In the same state it will appear after 112 impulses the latter being divisible by 16 and the closest to 125. After 13 more impulses it will be in 4 state which will be s hown by the numerical indicator.

1b104.

The critical path of a combinatorial circuit is the path with maximum delay. The mobility of an operation is the difference of its as-soon-as-possible (ASAP) start time and as-late-as-possible (ALAP) start time. The critical path in high level synthesis is a path for which all operations on the path have mobility equals zero.

1b105.

1) If there is no data dependency and two functional units that can execute the operations in parallel. 2) If the operations are on alternative branches in the control flow.

1b106.

Node index	ASAP	ALAP	Mobility
0	1	3	2
1	1	5	4
2	1	3	2
3	1	4	3
4	1	4	3
5	2	6	4
6	3	5	2
7	3	6	3
8	5	7	2

1b107.

1) TLM communication by function calls, RTL communication by signal protocols
2) TLM offers many timing modeling styles (PV; PVT,…), RTL is always clock driven (cycle-accurate).

1b108.

L1: cyc_wait,L1 = roundup[(4ns-10ns)/10ns] = 0
L2: cyc_wait,L2=roundup[(45ns+4ns-10ns)/10ns]=4
Mem: cyc_wait,mem=roundup[(483ns+45ns+4ns-10ns)/10ns]=53

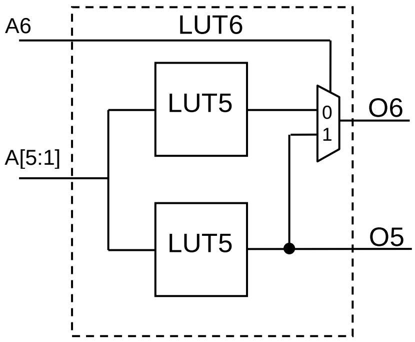
1b109.

cyc_wait,avg= α *0+(1- α)[β*4+(1- β)*53]
For α =β=50%: cyc_wait_avg=14.25

1b110.

t_exe =(500 000*CPI + 500 000 * 0.4 * cyc_wait,avg) * t_clock
= (500 000 * 1.6 + 500 000 0.4. * 14.25) * 10ns = 36.5 ms

1b111.



To make the LUT operate in its dual 5-input mode, A6 must be configured to '0' so O6 always takes the output of the upper LUT5.

1b112.

a) f = 1/T = 1/ (4*4ns) = 62.5 MHz
b) f = 1/T = 1/ (3*4ns) = 83.3 MHz
c) f = 1/T = 1/ (2*4ns) = 125 MHz

1b113.

Define:

$P_i = A_i \oplus B_i$ Carry propagate signal
$G_i = A_iB_i$ Carry generate signal

Then

$S_i = P_i \oplus C_{i-1}$
$C_{i+1} = G_i + P_iC_i$

For a 4-bit adder:

$C_1 = G_0 + P_0C_0$
$C_2 = G_1 + P_1C_1 = G_1 + P_1G_0 + P_1P_0C_0$
$C_3 = G_2 + P_2C_2 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$
$C_4 = G_3 + P_3C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$

1b114.

X_{i+1}	X_i	C	S2	S1	FFIN
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	0	1

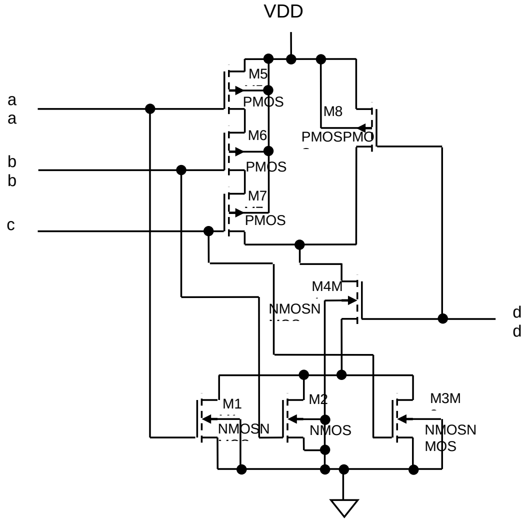
1b115.

$$LTE = \frac{1}{2}h^2|\ddot{v}_{\max}| \quad \Rightarrow \quad h = \sqrt{\frac{2 \cdot LTE}{|\ddot{v}_{\max}|}} = \sqrt{\frac{2 \cdot 10^{-4}}{|\ddot{v}_{\max}|}}$$

$$|\ddot{v}_{\max}| = \left|\frac{d^2(2\sin(10^3 t))}{dt^2}\right| = \left|2 \cdot 10^3 \frac{d(\cos(10^3 t))}{dt}\right| = \left|-2 \cdot 10^6 \sin(10^3 t)\ \big|_{\sin(10^3 t)=1}\right| = 2 \cdot 10^6$$

$$h = \sqrt{\frac{2 \cdot LTE}{|\ddot{v}_{\max}|}} = \sqrt{\frac{2 \cdot 10^{-4}}{2 \cdot 10^6}} = 10^{-5} s$$

1b116.



1b117.

In order to obtain the same delay of the rising and falling edge of an inverter it is necessary to provide the same resistivity for nMOS and pMOS transistor. That will happen if $W_p/L_p=(\mu_n/\mu_p)(W_n/L_n)= 2(W_n/L_n)$. The smallest inverter with equal delays at rising and falling edge (the unit inverter) will have $W_n/L_n = 3\lambda/2\lambda$ and $W_p/L_p = 6\lambda/2\lambda$.

In order to obtain the same falling edge delay for circuit in figure as for the unit inverter, one should provide that nMOS subcircuit has, in the worst case, the same resistivity as the nMOS transistor in the inverter. In the worst case the slowest falling edge will occur when M4 and at least one of M1, M2, and M3 conducts. Therefore the resistivity of series connection of M4 and (M1 or M2 or M3) should be the same as the resistivity of the unit nMOS. Therefore $W_1/L_1 = W_2/L_2 = W_3/L_3 = W_4/L_4 = 2(W_n/L_n) = 6\lambda/2\lambda$.

Similarly, to get the same rising edge delay pMOS subcircuit should have the same resistivity as the pMOS transistor of unit inverter. In the worst case the slowest rising edge will occur when M5, M6, and M7 conduct. Therefore the resistivity of series connection of M5, M6 and M7 should be the same as the resistivity of the unit pMOS. Therefore $W_5/L_5 = W_6/L_6 = W_7/L_7 = 3(W_p/L_p) = 18\lambda/2\lambda$. Simultaneously, when only M8 conducts, the same rising edge will provide $W_8/L_8 = W_p/L_p = 6\lambda/2\lambda$.

1b118.

For pMOS subcircuit:

$$F=\overline{(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)\,\mathrm{AND}\,d}=\overline{(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)}\ \mathrm{OR}\ \overline{d}=(\overline{a}\,\mathrm{AND}\,\overline{b}\,\mathrm{AND}\,\overline{c}\,)\,\mathrm{OR}\ \overline{d}$$

For nMOS subcircuit

$$\overline{F}=\overline{\overline{(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)\,\mathrm{AND}\,d}}=\overline{\overline{(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)}\,\mathrm{OR}\,\overline{d}}=\overline{\overline{(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)}}\,\mathrm{AND}\,\overline{\overline{d}}=(a\,\mathrm{OR}\,b\,\mathrm{OR}\,c)\,\mathrm{AND}\,d$$

1b119.

$$\Delta V_V=\frac{C_{AV}}{C_V+C_{AV}}\Delta V_A=\frac{60}{40+60}\cdot 1=0{,}6V$$

a.

b. CVsw=CV+2CAV=40+2Ē60=160 fF

1b120.

P(1)=P(A)P(B)P(C)+ P(A)(1-P(B))(1-P(C))+ (1-P(A))(1-P(B))P(C)+ (1-P(A))P(B)(1-P(C))

P(0)=1-P(1)

P=P(0)*P(1)

a) P(1)=0,5; P(0)=0,5;

P=0,25

b) P(1)=0,2*0,4*0,6+0,2*0,6*0,4+0,8*0,6*0,6+0,8*0,4*0,4=0,048+0,048+0,288+0,128= =0,512; P(0)= 0,488

P= 0,249856

1b121.

$$X=\left((\overline{A}+\overline{B})(\overline{C}+\overline{D}+\overline{E})+\overline{F}\right)\overline{G}=\overline{\overline{(\overline{A}+\overline{B})(\overline{C}+\overline{D}+\overline{E})+\overline{F}}+G}=\overline{\overline{(\overline{A}+\overline{B})(\overline{C}+\overline{D}+\overline{E})}F+G}$$
$$=\overline{\left(\overline{(\overline{A}+\overline{B})}+\overline{(\overline{C}+\overline{D}+\overline{E})}\right)F+G}=\overline{(AB+CDE)F+G}$$

In NMOS network:
For F-C-D-E path: WNF/L=4; WNC/L= WND/L= WNE/L= 12;
For F-A-B path: WNA/L= WNB/L=8
For G path: WNG/L=2
In PMOS network:
For G-C-A, G-D-A, G-E-A, G-C-B, G-D-B, G-E-B paths: WPC/L= WPD/L= WPE/L= WPA/L= WPB/L=24; WPG/L=12
For G-F path: WPF/L=12.

1b122.

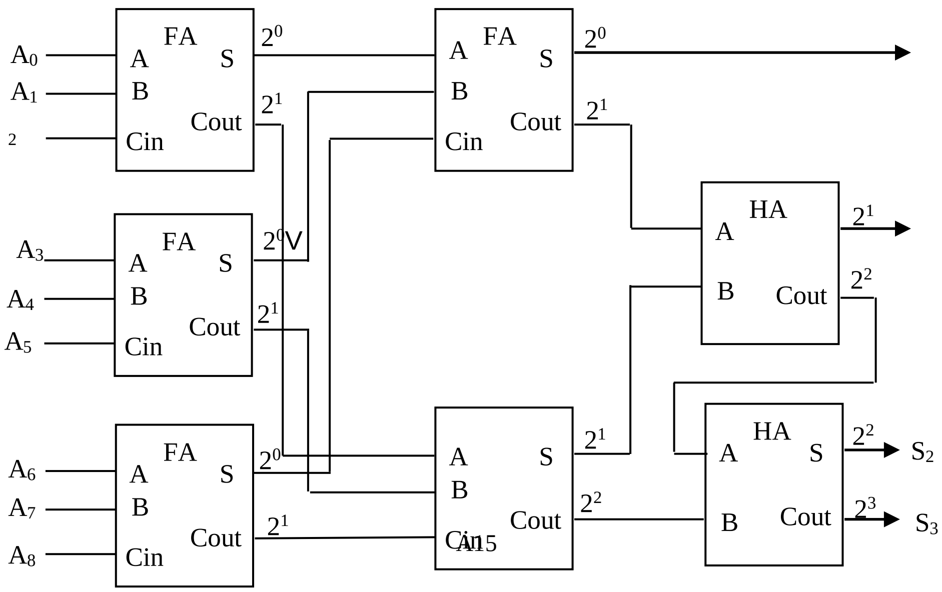
a. $Y = \overline{CD(A+B)}$
b. PMOS W/L = 8: $(W/L)_{pDC}$=8, $(W/L)_{pAB}$=16
NMOS W/L=4: $(W/L)_{nCD}$=8; $(W/L)_{nAB}$=4
c. t_{pHLmax} ABCD=0111 or 1011
t_{pLHmax} ABCD=0111 or 1011

1b123.

$$V_{SPH} = \frac{VDD + \sqrt{\frac{W_1 L_3}{W_3 L_1}} V_{tn}}{1 + \sqrt{\frac{W_1 L_3}{W_3 L_1}}} = \frac{3{,}3 + \sqrt{\frac{9}{7}} 0{,}6}{1 + \sqrt{\frac{9}{7}}} = 1{,}865 \text{ V}$$
$$V_{SPL} = \frac{(VDD - V_{tp})\sqrt{\frac{W_5 L_6}{W_6 L_5}}}{1 + \sqrt{\frac{W_5 L_6}{W_6 L_5}}} = \frac{(3{,}3 - 0{,}7)\sqrt{\frac{27}{22}}}{1 + \sqrt{\frac{27}{22}}} = 1{,}366 \text{ V}$$

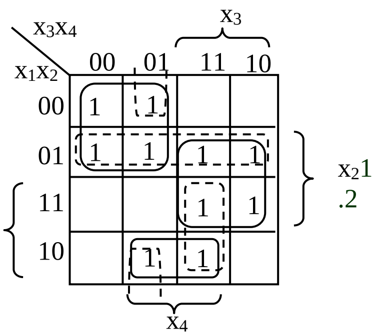
1b124.
$V_S = VDD - V_t = 5 - V_t$;
$V_t = V_{t0} + \gamma\left(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}\right)$;
VB=0 $V_t = 1 + 0{,}3\left(\sqrt{0{,}6 + 5 - V_t} - \sqrt{0{,}6}\right)$
Vt=1,384V.

1b125.
To compute the number of "1"s in the code, full adders or semiadders are used. Balances of bits are written in the inputs of adders. A8…A0 is input 9-bit code, S3, S2, S1, S0 – output code (number of "1"s in input code).



1b126.

Carnough map

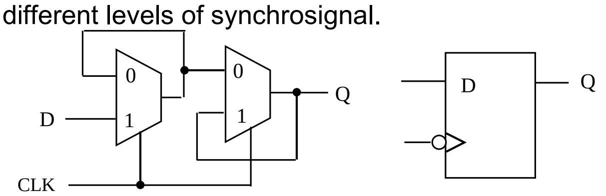


In case of changes of 0001↔1001, 0101↔0111, 1111↔1011 sets, the function has static hazard. To get rid of the hazard, implicants, mentioned in dot-lines need to be added on the map.

Without static hazard, the circuit will be constructed on the basis of $y = \overline{x1} \cdot \overline{x3} + x2 \cdot x3 + x1 \cdot \overline{x2} \cdot x4 + \overline{x1} \cdot x2 + x1 \cdot x3 \cdot x4 + \overline{x2} \cdot \overline{x3} \cdot x4$ expression.

1b127.

This type of flip-flop can be configured by sequentially connecting two multiplexors which are controlled by different levels of synchrosignal.



1b128.

Analyze the circuit.

d1 = ~q2; t2 = q1; t3= q2;

Define characterizing equations of flip-flops: q1*, q2*, q3*;

q1* = d1 =~q2; q2* = t2⊕q2= q1⊕q2; q3* = t3⊕q3= q2⊕q3;

Based on characterizing equations, the sequence of circuit states is defined. The table of circuit states will have the following view:

q1 q2 q3
0 0 0
1 0 0
1 1 0
0 0 1
1 0 1
1 1 1
0 0 0

After 000 state, the sequence of states is repeated.

1b129.

SUB	R2, R1, R2	data hazard
ADD	R4, R3, R2	
BNEZ	R1, B1	
ADD	R4, R4, R4	Control hazard
SUB	R2, R2, R1	data hazard
B1:	ADD	R4, R4, R2

1b130.

Branch not taken: 6 + 4 (data hazards) = 10

Branch taken: 4 + 2 (data hazards) + 2 (branch hazard) = 8

1b131.

Node:	ASAP Start Time
v_1	1
v_2	1
v_3	1
v_4	1
v_5	2
v_6	4
v_7	4

1b132.

Switching point voltage is computed by the following formula:

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} V_{Tn} + (V_{DD} - V_{Tp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Putting switching point and threshold values, denoting β_n/β_p ratio by x^2, this is obtained: 0,9=(0,5x+(1,8-0,6))/(1+x), x=0,75, $\beta_n/\beta_p=x^2=0{,}5625$, $\beta_n/\beta_p=(W_n k_{pn}/L_n)/(W_p k_{pp}/L_p)=(W_n k_{pn})/(W_p k_{pp})=(W_n \mu_n)/(W_p \mu_p)=3W_n/W_p=0{,}5625$ W_p=3Ē 0,5/0,5625=2,67 mkm

1b133.

$N=\ln(C_L/C_{in1})=\ln(200/2)=4{,}6>>4$

$A=(C_L/C_{in1})^{1/N}=(200/2)^{1/4}=3{,}16$

1b134.

a. $V_{OH}=V_{DD}-V_{tn0}=2$; $V_{OL}=|V_{tp0}|=0{,}6V$

b. $V_{SBn}=V_{outH}$, $V_{outH}=V_{dd}-V_{tn}$

$V_{tn}=V_{tn0}+\gamma(\sqrt{2|\Phi F|+V_{SB}}-\sqrt{2|\Phi F|})=0{,}5+0{,}5(\sqrt{0{,}6+V_{SB}}-\sqrt{0{,}6})$

$V_{outH}=V_{DD}-0{,}5-0{,}5(\sqrt{0{,}6+\mathrm{VoutH}}-\sqrt{0{,}6})=2-0{,}5(\sqrt{0{,}6+\mathrm{VoutH}}-0{,}775)$

$V_{outH}-2{,}3875+0{,}5\sqrt{0{,}6+\mathrm{VoutH}}=0$

$V_{outH}+0{,}6-2{,}9875+0{,}5\sqrt{0{,}6+\mathrm{VoutH}}=0$

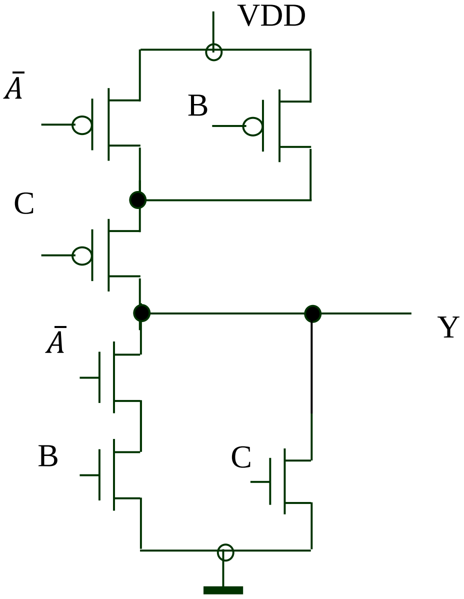
$x=\sqrt{0{,}6+\mathrm{VoutH}}$

$x^2+0{,}5x-2{,}9875=0$, x=1,496; $V_{outH}=1{,}638V$

1b135.

Truth table:

#	A B C	Y	$\overline{Y}$
0	0 0 0	1	0
1	0 0 1	0	1
2	0 1 0	0	1
3	0 1 1	0	1
4	1 0 0	1	0
5	1 0 1	0	1
6	1 1 0	1	0
7	1 1 1	0	1



$\overline{Y}=C+\overline{A}B$

$Y=\overline{C+\overline{A}B}$

1b136.

$$t_D = rc\frac{L^2}{2} + L\cdot r\cdot C = 0.1\cdot 2\cdot\frac{100^2}{2} + 100\cdot 0.1\cdot 1.5\cdot 10^3 = 16ps$$

1b137.
$P_1=P_{1A}P_{1B}P_{1C}$=0,25*0,50*0,75=3/32
P_{01} = P_0Ē P_1=(1-P_1)P_1=3/32*29/32=87/1024=0,085

1b138.
Z=A&B+C&D

ABCD	Z	ABCD	Z
0000	0	1000	0
0001	0	1001	0
0010	0	1010	0
0011	1	1011	1
0100	0	1100	1
0101	0	1101	1
0110	0	1110	1
0111	1	1111	1

P_1=7/16; P_0=9/16
P_{01} = P_0Ē P_1=7/16*9/16=63/256=0,246

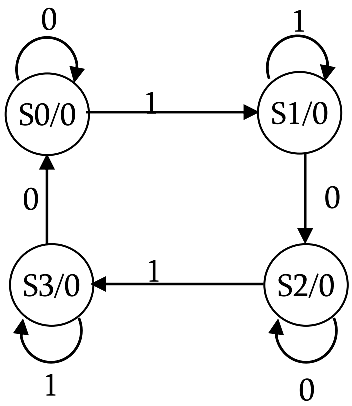
1b139.
$Y = \overline{CD(A + B)}$
$P_0=P_{C1}P_{D1}(P_{A1}+P_{B1}-P_{A1}P_{B1})$=0,3Ē0,8(0,5+0,2-0,5Ē0,2)=0,144,
$P_1=1-P_0$=0,856,
$P_{01}=P_0P_1$=0,144Ē 0,856=0,123264,
P_{sw}= $P_{01}V_{DD}^2F_{clk}C_{out}$=0,123264Ē2,5^{2}Ē250Ē10^{6}Ē30Ē10^{-15}=5,778μW.

1b140.
1b141.
1b142.
1b143.
(The same solution way for 1b140; 1b141; 1b142; 1b143 four variants of one problem are given. One of the possible solutions of the problem (the example is for variant 2).
<u>Possible Solution for 50% Duty-Cycle Frequency Division Problem</u>
// frequency division by rate 5 with 50% duty cycle:

```
module clk_div_by_5 (clk_i, reset_ni, clk5_o);
    input  clk_i;
    output clk5_o;
    wire       clk_neg0;
    reg  [2:0] counter_0, counter_1;
    reg        start_counter_1, half_clk5_0, half_clk5_1;
    ///////////////////////////////////////// preparing counters
    assign clk_neg0 = ~clk_i;
    always @(posedge clk_i or negedge reset_ni) begin
        if (reset_ni == 1'b0)        counter_0 <= 3'd0;
        else if (counter_0 == 3'd4)  counter_0 <= 3'd0;
        else                         counter_0 <= counter_0 + 3'd1;
    end
    always @(posedge clk_i or negedge reset_ni) begin
        if (reset_ni == 1'b0)        start_counter_1 <= 1'd0;
        else if (counter_0 == 3'd2)  start_counter_1 <= 1'd1;
        else                         start_counter_1 <= start_counter_1;
    end
    always @(posedge clk_neg0 or negedge reset_ni) begin
        if (reset_ni == 1'b0)        counter_1 <= 3'd0;
        else if (counter_1 == 3'd4)  counter_1 <= 3'd0;
        else if (start_counter_1)    counter_1 <= counter_1 + 3'd1;
        else                         counter_1 <= counter_1;
    end
    ////////////////////////////////////////////////////////////////////////
    // preparing half-clocks, they both are expected to have 10 times bigger
    // period than the original source clock's period. But these two clocks
    // (named half_clk5_0 and half_clk5_1) have phase offset to each other
```

```
    // which equals to 1/4 duration of their period:
    //   _   _   _   _   _   _   _   _   _   _   _   _   _   _   _   _   _
    // _/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/ \_/
    //   ___________________                     ___________________
    // _/                   \___________________/                   \________
    //             ___________________                     __________________
    // ___________/                   \___________________/
    always @(posedge clk_i or negedge reset_ni) begin
        if (reset_ni == 1'b0)        half_clk5_0 <= 3'd0;
        else if (counter_0 == 3'd4)  half_clk5_0 <= ~half_clk5_0;
        else                         half_clk5_0 <=  half_clk5_0;
    end
    always @(posedge clk_neg0 or negedge reset_ni) begin
        if (reset_ni == 1'b0)        half_clk5_1 <= 3'd0;
        else if (counter_1 == 3'd4)  half_clk5_1 <= ~half_clk5_1;
        else                         half_clk5_1 <=  half_clk5_1;
    end
    //Then XOR-ing these half-clocks to get the 50% duty-cycle divided by 5:
    //   ___________________                     ___________________
    // _/                   \___________________/                   \______
    //             ___________________                     ________________
    // ___________/                   \___________________/
    //   _________           _________           _________           ______
    // _/         \_________/         \_________/         \_________/
    assign clk5_o = half_clk5_0 ^ half_clk5_1;
endmodule
```

1b144.
The state diagram of FSM is the following:



Primitive flow table:

State	X=0	X=1	Output
S0	**S0**	S1	0
S1	S2	**S1**	0
S2	**S2**	S3	0
S3	S0	**S3**	1

State assignment table:

State	q1q2
S0	0 0
S1	1 0
S3	1 1
S3	0 1

Table of transitions of the FSM:

T \ q1q	00	01	11	10
0	00	00	11	11
1	10	01	01	10

The next state functions (Q1, Q2) are determined based on the table of transitions.

Q1

x \ q1q2	00	01	11	10
0			1	1
1	1			1

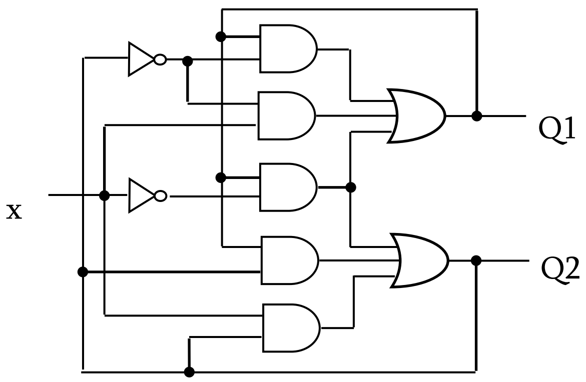
Q2

x \ q1q2	00	01	11	10
0			1	1
1		1	1	

Q1= $\bar{x} \cdot q1 + x \cdot \bar{q2} + q1 \cdot \bar{q2}$; Q2= $\bar{x} \cdot q1 + x \cdot q2 + q1 \cdot q2$;

To obtain circuits, free of logical hazards in Q1 expression added term $q2 \cdot \bar{q1}$ and in Q2 expression - term $q2 \cdot q1$.

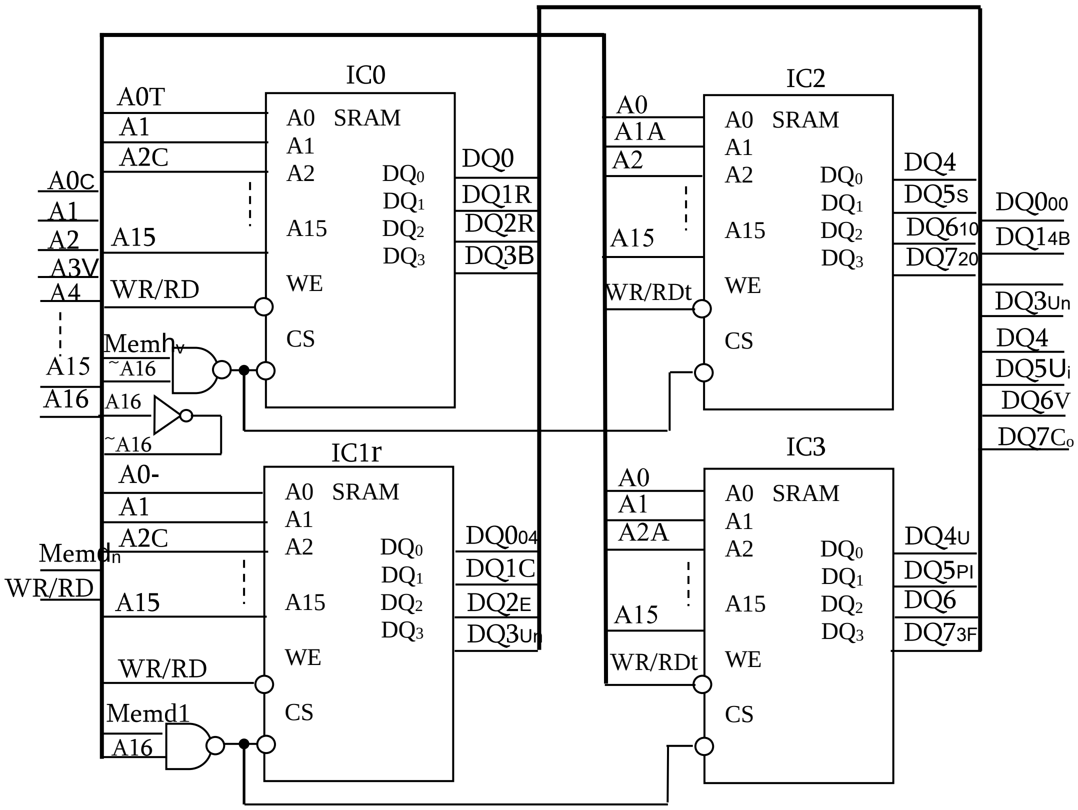
Asynchronous FSM circuit is presented below.



1b145.

The number of ICs, required to build a memory module is equal to N=128Kx8/64Kx4 = 4: two ICs - to form the word length, and two ICs - to get the memory size. Number of address inputs of the module is 17.

A16 A15 . . . A1 A0	IC
0 0 . . . 0 0	IC0, IC2
. . .	
0 1 1 1	
1 0 . . . 0 0	IC1, IC23
. . .	
1 1 1 1	



Mem input signal allows memory access, WR/RD signal determines the write operation (WR / RD = 0) or reading (WR / RD = 1).

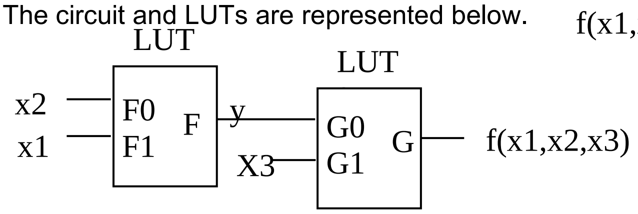
1b146.

Function of three variables is usually implemented using three-input LUT. To implement the function of two two-input LUTs, try to minimize it.

x1 \ x2x3	00	01	11	10
0		1	1	
1		1	1	1

The circuit and LUTs are represented below.

$f(x1,x2,x3)=x1\cdot x2 + x3$



LUT1

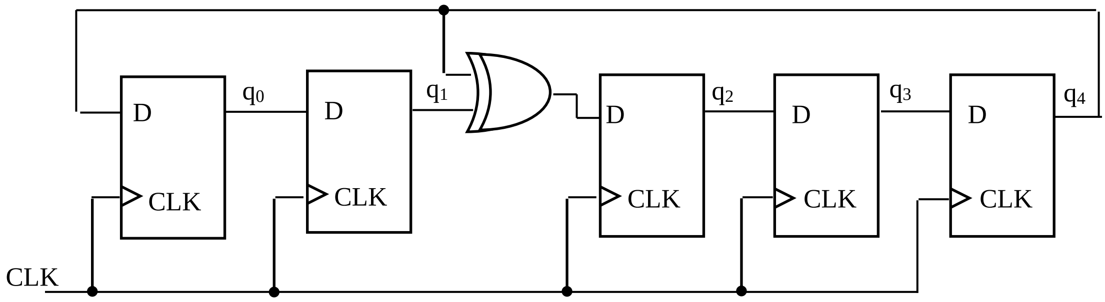
x1 x2	y
F1 F0	F
0 0	0
0 1	0
1 0	0
1 1	1

LUT2

y x1	F(x1,x2,x3)
G1 G0	G
0 0	0

0 1	1
1 0	1
1 1	1

1b147.
The circuit corresponding to the description is presented.



This circuit is the generator of the Galois field elements. Polynomial in the feedback loop

1b148.
Since the memory has the form of a sqare matrix, then the number of columns, as well as rows, can be estimated as O([✓n]). Since the base cell of the algorithm should pass over all n cells of the memory, and the Read operation should be done only in the row where the base cell is located, then (in all, O(✓n) Read operations) the overall number of operations will be O(n✓n).

1b149.
⇕ (W0, W1, R1, W0, R0).

1b150.
To detect those faults, solve the following well-known Boolean equations:

- For stuck-at-0 fault - g(A, S, B) dZ(A, S, B, g)/dg = 1;
- For stuck-at-1 fault - g'(A, S, B) dZ(A, S, B, g)/dg = 1.

There is Z=AS V S'B ;

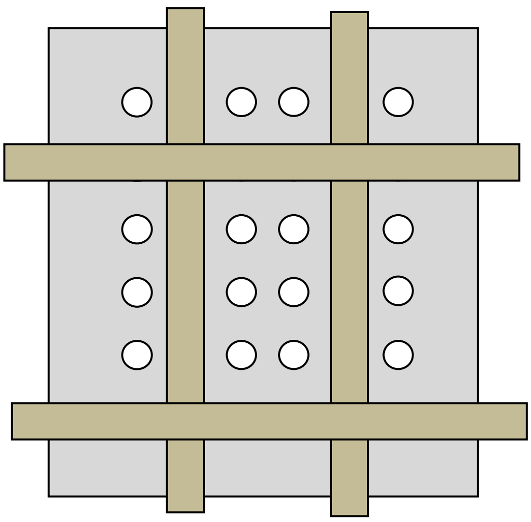
g=S' => Z = AS V gB => dZ/dg = AS ⊕ (AS V B) => dZ/dg = (AS)'B = (A' V S') B =>

- For stuck-at-0 fault - g dZ(A, S, B, g)/dg = S' ((A' V S')B) = S'B =1;
- For stuck-at-1 fault - g' dZ/dg = g' (A' V S') B = S (A' V S')B = A'SB = 1.

After solving the last two equations, get the sets T_1 and T_2 of all test patterns that detect stuck-at-0/1 faults:

- For stuck-at-0 fault - T_0 = {(0,0,1), (1,0,1)};
- For stuck-at-1 fault - T_1 = {(0,1,1)}.

1b151.
The second and fifth columns should be repaired with two spare columns, and the second and sixth rows are repaired with two spare rows. See the diagram below.



1b152.
Verilog RTL model for LFSR

```
module lfsr (clock,reset,lfsr_out);
input clock,reset;
output [2:0]lfsr_out;
reg [2:0]lfsr_r,lfsr_nxt;
assign lfsr_out = lfsr_r;
//Non-blocking assignment
always @ (posedge clock or posedge reset)
if(reset) lfsr_r <= 3'b001;
else lfsr_r <= lfsr_nxt;
//LFSR
always @ (lfsr_r)
lfsr_nxt = {lfsr_r[1:0],(lfsr_r[2]^lfsr_r[1])};
endmodule //lfsr
```

1b153.
Verilog RTL model for MISR

```
module misr (clock,reset,in,misr_out);
input clock,reset;
input [2:0]in;
output [2:0]misr_out;
reg [2:0]misr_r,misr_nxt;
assign misr_out = misr_r;
//Non-blocking assignment
always @ (posedge clock or posedge reset)
if(reset) misr_r <= 3'b0;
else misr_r <= misr_nxt;
//MISR
always @ (misr_r or in)
misr_nxt = {(misr_r[1]^in[2]),(misr_r[0]^in[1]),(misr_r[2]^misr_r[1]^in[0])};
endmodule //misr
```

1b154.
FSM containing 8 states will resolve the problem (8 internal states can be stored with 3 flip-flops). After reset the FSM gets initial state and then changes its state based on the serial input values. When the serial combination 1010110 is detected, the FSM gets STATE_7 internal value.
FSM state transition table for serial combination 1010110 is presented below.

Current states		Serial input value	Next state
Internal state	Detected combination		

STATE_0	7'b0000000	0	STATE_0
		1	STATE_1
STATE_1	7'b0000001	0	STATE_2
		1	STATE_1
STATE_2	7'b0000010	0	STATE_0
		1	STATE_3
STATE_3	7'b0000101	0	STATE_4
		1	STATE_1
STATE_4	7'b0001010	0	STATE_0
		1	STATE_5
STATE_5	7'b0010101	0	STATE_4
		1	STATE_6
STATE_6	7'b0101011	0	STATE_7
		1	STATE_1
STATE_7	7'b1010110	0	STATE_0
		1	STATE_3

Verilog RTL for a serial detector

```
//Serial FSM detector of '1010110'
combination
module detector_fsm (clk, rst, serial_data, match);
input clk, rst, serial_data;
output match;
//Variables
reg [2:0]state_r, state_nxt;
reg match_r,match_nxt;
//Internal states
parameter STATE_0 = 3'd0; //0000000 detected
parameter STATE_1 = 3'd1; //0000001 detected
parameter STATE_2 = 3'd2; //0000010 detected
parameter STATE_3 = 3'd3; //0000101 detected
parameter STATE_4 = 3'd4; //0001010 detected
parameter STATE_5 = 3'd5; //0010101 detected
parameter STATE_6 = 3'd6; //0101011 detected
parameter STATE_7 = 3'd7; //1010110 detected
```

```
//Assignments
assign match = match_r;
//Finite state machine for 7'b1010110 combination
always @ (state_r or serial_data)
case(state_r)
      STATE_0 : if(!serial_data) state_nxt = STATE_0;
                else             state_nxt = STATE_1;
      STATE_1 : if(!serial_data) state_nxt = STATE_2;
                else             state_nxt = STATE_1;
      STATE_2 : if(!serial_data) state_nxt = STATE_0;
                else             state_nxt = STATE_3;
      STATE_3 : if(!serial_data) state_nxt = STATE_4;
                else             state_nxt = STATE_1;
      STATE_4 : if(!serial_data) state_nxt = STATE_0;
                else             state_nxt = STATE_5;
      STATE_5 : if(!serial_data) state_nxt = STATE_4;
                else             state_nxt = STATE_6;
      STATE_6 : if(!serial_data) state_nxt = STATE_7;
                else             state_nxt = STATE_1;
      default : if(!serial_data) state_nxt = STATE_0;
                else             state_nxt = STATE_3;
endcase
//Detection logic
always @ (state_r)
match_nxt = (state_r == STATE_7);

//Non-blocking assignments
always @ (posedge clk or negedge rst)
if(!rst)
      begin
            state_r <= 3'd0;
            match_r <= 1'b0;
      end
else
      begin
            state_r <= state_nxt;
            match_r <= match_nxt;
      end
endmodule //module detector_fsm
```

1b155.

1）create_clock –name ICKA –period 4 [get_ports ICKA]

create_clock –name ICKB –period 5 [get_ports ICKB]

create_generated_clock –name ICKA_DIV2 –source [get_ports ICKA] –divided_by 2 [get_pins D1/Q]

create_generated_clock –name OCKA –source [get_pins D1/Q] –combinational [get_ports OCKA]

create_generated_clock –name OCKB –source [get_ports ICKB] –combinational [get_ports OCKB]

set_clock_group -asynchronous -name async -group {ICKA ICKA_DIV2 OCKA} -group {ICKB OCKB}

set_multicycle_path –from [get_pins B1/CP] –to [get_pins B2/D] –setup 2

set_multicycle_path –from [get_pins B1/CP] –to [get_pins B2/D] –hold 1

set_input_delay 1,8 –clock ICKA [get_ports IDA]

set_input_delay 1,2 –clock ICKA –clock_fall [get_ports IDB]

set_output_delay 0,8 –clock OCKA [get_ports ODA]

set_output_delay 1,3 –clock OCKB [get_ports ODB]

2）Answer: For clock domain ICKA, WNS is -0,3ns and max frequency is 233MHz. For clock domain ICKB, WNS is 0,8ns and max frequency is 238MHz.

3）Answer: WNS of clock domain ICKA is negative, and the critical path is from A1 to A2. Two approaches help - perform logic optimization on datapath, or increase the capture clock latency by adopting useful skew.

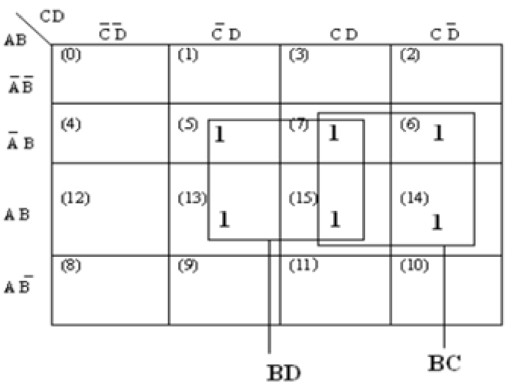
1b156.

- **The Truth Table**

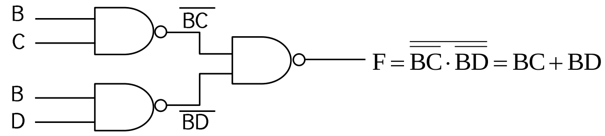
Inputs				Output (F)
A	B	C	D	
0	0	0	1	0
0	0	0	0	0
0	0	1	1	0
0	0	1	0	0
0	1	0	1	0
0	1	0	0	1
0	1	1	1	1
0	1	1	0	1
1	0	0	1	0
1	0	0	0	0
1	0	1	1	0
1	0	1	0	0
1	1	0	1	0
1	1	0	0	1
1	1	1	1	1
1	1	1	0	1

- **The Karnaugh Map**

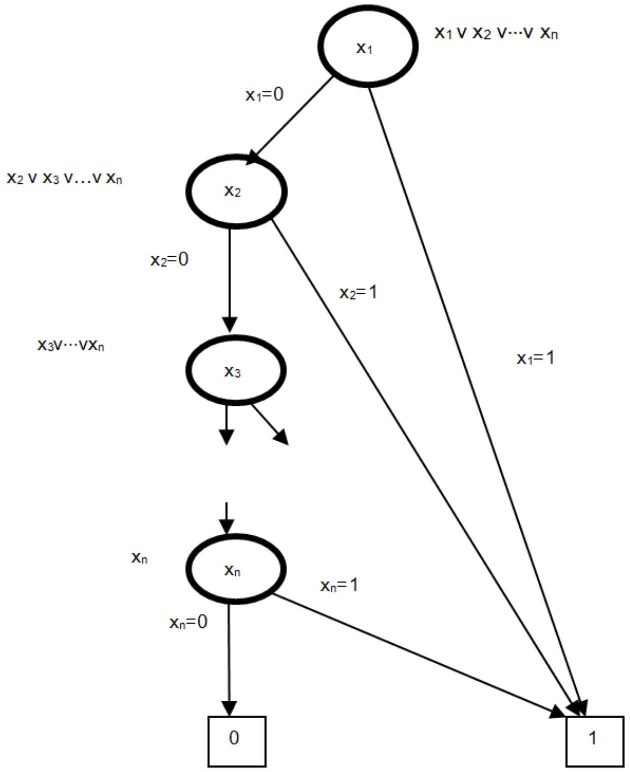
The simplified expression is F = BC + BD.



- The NAND-NAND implementation

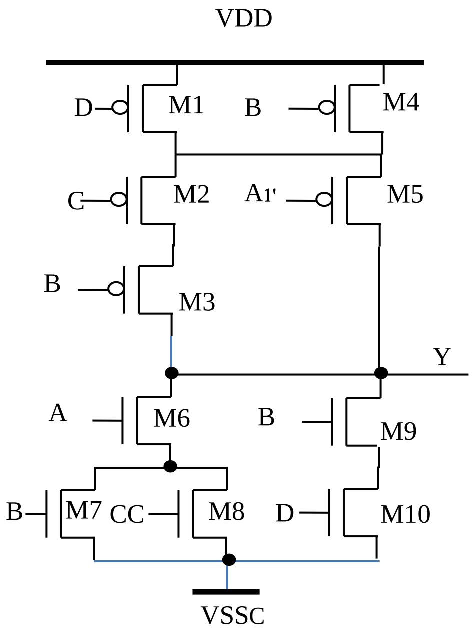


1b157.



1b158.
$\Updownarrow$ (W0), $\Uparrow$ (R0, W1), $\Downarrow$ (R1, W0)

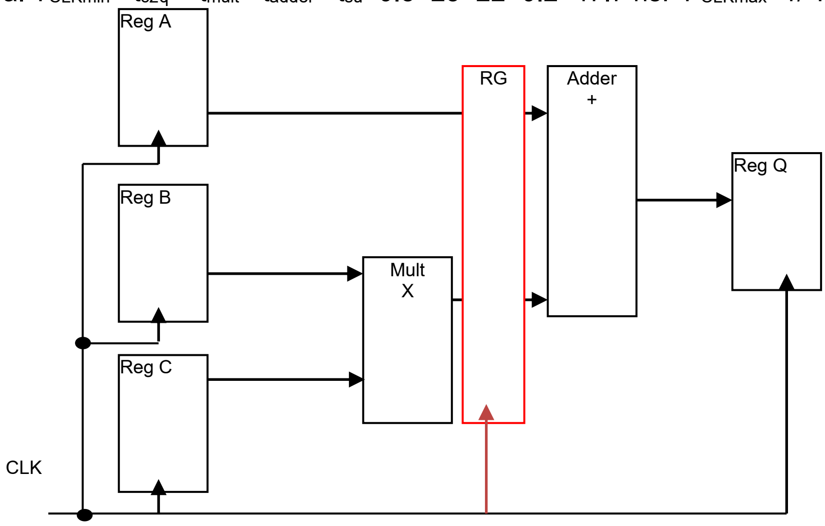
1b159.
a. $t_{Asu}= t_{buf}+ t_{nor2} + t_{su}- t_{buf}$ = 120+160+20-120=180ps.
b. $t_{CLK2B} = t_{buf} +t_{c2q}+ t_{and2}$=120+200+150=470 ps.
c. $T_{CLKmin}= t_{su}+ t_{c2q}+ t_{nor2}$ =20+200+160=380 ps; F_{CLKmax}=1/ T_{CLKmin}=2.63 GHz
1b160.



M1, M2, M3: 3Wp=6Wn; M4, M5: 2Wp=4Wn
M6, M9, M10: 2Wn; M7, M8: Wn.

1b161.

a. $T_{CLKmin}= t_{c2q} + t_{mult}+ t_{adder}+ t_{su}=0.5+25+22+0.2=47.7$ ns: $F_{CLKmax}=1/ T_{CLKmin}=21$ MHz



b. $T_{CLKmin}= t_{c2q} + t_{mult}+ t_{su}=0.5+25+0.2=25.7$ns: $F_{CLKmax}=1/ T_{CLKmin}=39$ MHz

1b162.

$N=\ln(C_{load}/ C_{in1})=4.6$

$C_{out1}=c_{in}1/1.5=1.33$fF

If it is taken N=4

$A=(C_{Load}/C_{in1})^{1/N}=(200/2)^{1/4}=3.16$

$(t_{PHL}+t_{PLH})_{total}=0.7N(R_{n1}+R_{p1})(C_{out1}+ AC_{in1})=0.7*4(R_{n1}+R_{p1})(1.33+3.16*2)=21.43(R_{n1}+R_{p1})$

If it is taken N=5

$A=(C_{Load}/C_{in1})^{1/N}=(200/2)^{1/5}=2.51$

$(t_{PHL}+t_{PLH})_{total}=0.7N(R_{n1}+R_{p1})(C_{out1}+ AC_{in1})=0.7*5(R_{n1}+R_{p1})(1.33+2.51*2)=22.24(R_{n1}+R_{p1})$

The optimal number N=4.

$W_{1n}=1, W_{1p}=2, W_{2n}=3.16, W_{2p}=6.32, W_{3n}=10, W_{3p}=20, W_{4n}=31.6, W_{4p}=63.2$

1b163.

$t_{d1}=3aC R$; $t_{d2}=(R/a)4bC$; $t_{d3}=(R/b)18C$

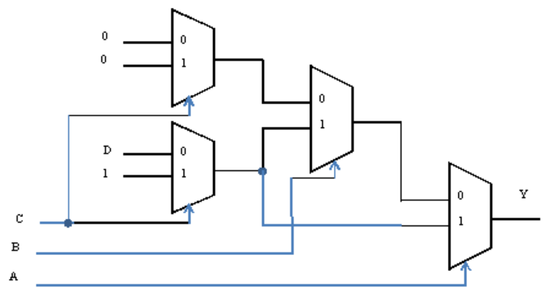
$t_d=t_{d1}+t_{d2}+t_{d3}=RC(3a+4b/a+18/b)$

$dt_d/da=RC(3-4b/a^2)=0 \quad => b=3a^2/4$

$dt_d/db=RC(4/a-18/b^2)=0 \quad => a=4b^2/18=4*9a^4/16*18 => a^3=16*18/4*9=8 => a=2$

1b164.

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	D
0	1	1	1
1	0	0	D
1	0	1	1
1	1	0	D
1	1	1	1



1b165.

Define q0*,q1*,q2* next state functions of flip-flops , using the characteristic equation of T flip-flop.

$t_0= \bar{q}_2$; $q_0=q_0\oplus t_0$

$t_1= \overline{\overline{q_0\cdot q_1}\cdot \bar{q}_2}=q_0\cdot q_1 + q_2$; $q_2=q_2\oplus t_2$

$t_2=q_0$; $q_1=q_1\oplus t_1$

Define the sequence of transitions of a circuit.

$q_2\ q_1\ q_0$
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
0 0 0

The analyzed circuit is a modulo 5 up-counter.

1b166.
The reset signal CLR is supplied to the LUT address input A3. Counter outputs Q0, Q1, Q2 through programmable switches, coming to the address inputs A0, A1, A2.
LUT configuration:

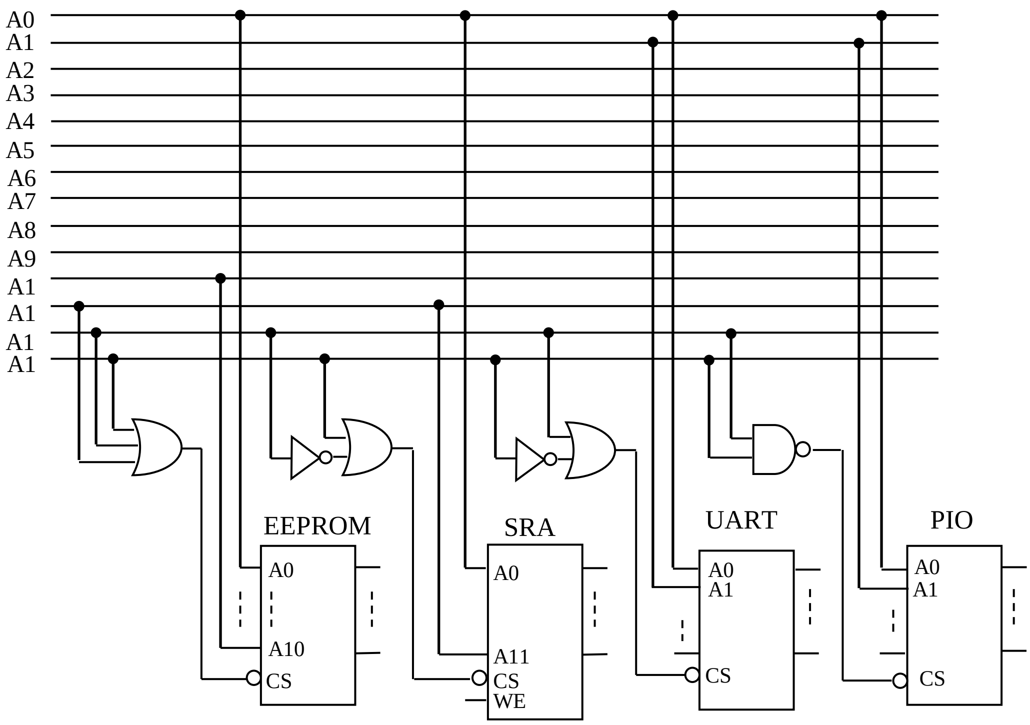
CLR Q2 Q1 Q0				Q3 Q2 Q1 Q0			
I3	I2	I1	I0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

1b167.

A13A12A11 A10 A9 . . . A3A2A1A0	
0 0 0 0 0 . . . 0 0 0 0 . . . . 0 0 0 1 1 . . . 1 1 1 1	EEPROM – 2KB
0 0 1 0 . . . . 0 0 0 0 . . . 0 0 1 1 . . . . 1 1 1 1	Unused Address Space 2 KB
0 1 0 0 . . . 0 0 0 0 0 1 0 0 . . . 0 0 0 1 . . . 0 1 1 1 . . . 1 1 1 1	SRAM – 4 KB
1 0 0 . . . 0 0 0 0 1 0 0 . . . 0 0 0 1 1 0 0 . . . 0 0 1 0 1 0 0 . . . 0 0 1 1	UART – 4B

1 0 0 . . . 0 1 0 0 . . . . . . 1 1 1 . . . 1 0 1 1	Unused Address Space
1 1 1 . . . 1 1 0 0 1 1 1 . . . 1 1 0 0 1 1 1 . . . 1 1 0 0 1 1 1 . . . 1 1 1 1	PIO – 4 B

circuit of address decoding is represented in the figure below.



1b168.

This circuit implements the following functions:

	A3 A2 A1 A0	y3 y2 y1 y0
0	0 0 0 0	1 0 1 0
1	0 0 0 1	1 0 0 0
2	0 0 1 0	1 0 1 0
3	0 0 1 1	0 1 0 1
4	0 1 0 0	0 0 0 0
5	0 1 0 1	0 0 0 0
6	0 1 1 0	0 0 0 0
7	0 1 1 1	0 0 0 0
8	1 0 0 0	1 0 0 0
9	1 0 0 1	0 0 0 0
1 0	1 0 1 0	0 0 0 0
1 1	1 0 1 1	0 0 0 0
1 2	1 1 0 0	0 1 0 1
1 3	1 1 0 1	1 0 0 0
1 4	1 1 1 0	0 1 0 0
1 5	1 1 1 1	1 0 1 0

$y0= m3 + m12;$

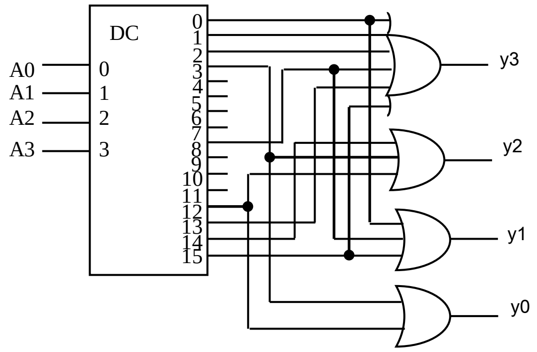
$y1= m0 + m2 + m15;$

$y2= m3 + m12+m14;$

$y3=m0+m1+m2+m8+m13+m15;$

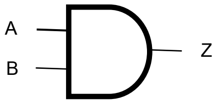
The ROM circuit is shown in the figure below.

m0, m1,m2 ... m15 are minterms of functions. They correspond to decoder outputs 0, 1, 2 ... 15.

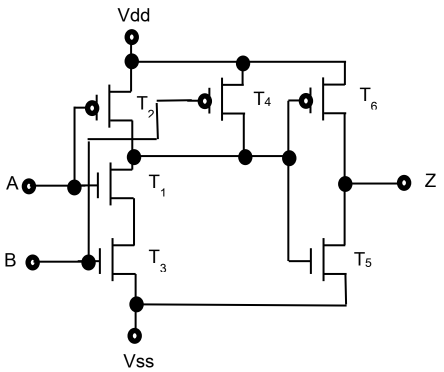


1b169.

1. From the truth table it follows that AND function is presented whose symbol in gate level has the following view:



2. The basic circuit that implements the given logic in transistor level, using three nMOS and three pMOS transistors, will be as follows:



3. the table will look like this after filling in T_1, T_2,..., T_6 columns with «on» or «off» words respectively:

A	B	Z	T_1	T_2	T_3	T_4	T_5	T_6
1	1	1	off	on	off	on	on	off
1	0	1	off	on	on	off	on	off
0	1	1	on	off	off	on	on	off
0	0	0	on	off	on	off	off	on

1b170.

```
reg out1,out2;
always @ (a or b or c or d or e)
  begink
    out1 = !(!(a | b) & !(c ^ d ^ e));
    out2 = !(!(a | b) | !(c ^ d ^ e));
  end
```

2. ANALOG INTEGRATED CIRCUITS

a) Test questions

2a1. D
2a2. D
2a3. E
2a4. E
2a5. B
2a6. E
2a7. B
2a8. E
2a9. B
2a10. E
2a11. E
2a12. D
2a13. C
2a14. C
2a15. C
2a16. A
2a17. C
2a18. C
2a19. E
2a20. A
2a21. C
2a22. D
2a23. D
2a24. D
2a25. E
2a26. D
2a27. E
2a28. E
2a29. D
2a30. B
2a31. A
2a32. B
2a33. E
2a34. C
2a35. B
2a36. C
2a37. C
2a38. E
2a39. B
2a40. C
2a41. B
2a42. E
2a43. B
2a44. D
2a45. C
2a46. D
2a47. E
2a48. A
2a49. E
2a50. E
2a51. D
2a52. E
2a53. C
2a54. A
2a55. D
2a56. A
2a57. D
2a58. C
2a59. B
2a60. B
2a61. A
2a62. D
2a63. A
2a64. D
2a65. A
2a66. D
2a67. C
2a68. D
2a69. A
2a70. B
2a71. A
2a72. B
2a73. C
2a74. C
2a75. B
2a76. B
2a77. E
2a78. C
2a79. E
2a80. B
2a81. A
2a82. C
2a83. B
2a84. C
2a85. E
2a86. C
2a87. B
2a88. B
2a89. C
2a90. A
2a91. A
2a92. D
2a93. A
2a94. B
2a95. C
2a96. A
2a97. A
2a98. A
2a99. D
2a100. B
2a101. C
2a102. C
2a103. B
2a104. B
2a105. C
2a106. D
2a107. D
2a108. C
2a109. A
2a110. B
2a111. C
2a112. C
2a113. A
2a114. B
2a115. A
2a116. D
2a117. B
2a118. E
2a119. D
2a120. B
2a121. C
2a122. B
2a123. C
2a124. B
2a125. A
2a126. C
2a127. E
2a128. E
2a129. D
2a130. B
2a131. E
2a132. E
2a133. D
2a134. D
2a135. B
2a136. C
2a137. C
2a138. B
2a139. B
2a140. B
2a141. A
2a142. B
2a143. C
2a144. C
2a145. C
2a146. D
2a147. C
2a148. C
2a149. D
2a150. D
2a151. A
2a152. D
2a153. C
2a154. C
2a155. D
2a156. C
2a157. E
2a158. E
2a159. D
2a160. A
2a161. C

b) Problems

2b1.

$$I_{D2} = I_{ref}\left(\frac{W_2}{L_2}\right)\Big/\left(\frac{W_1}{L_1}\right) = I_{ref}$$

$$\left|I_{D3}\right| = \left|I_{D2}\right|,\ I_{D3} = I_{ref}$$

$$I_{D4} = I_{D3}\left(\frac{W_4}{L_4}\Big/\frac{W_3}{L_3}\right)$$

$$I_{D4} = I_{ref}$$

2b2.

$$\left(V_{in} - V_{TH1}\right)^2 \cdot W_1 \cdot \mu_n \cdot \frac{C_{ox}}{L_1} \cdot 2 = \left(V_{DD} - V_{TH1} - V_{out}\right)^2 \cdot W_2 \cdot \mu_n \cdot \frac{C_{ox}}{L_2} \cdot 2$$

$$\sqrt{\frac{W_1}{L_1}} \cdot \left(V_{in} - V_{TH1}\right) = \sqrt{\frac{W_2}{L_2}} \cdot \left(V_{DD} - V_{TH1} - V_{out}\right)$$

$$\sqrt{\frac{W_1}{L_1}} = \sqrt{\frac{W_2}{L_2}} \cdot \frac{dV_{out}}{dV_{in}}$$

$$K = \frac{dV_{out}}{dV_{in}} = -\sqrt{\frac{W_1 - L_2}{W_2 - L_1}}$$

2b3.

$$\left(V_{in} - V_{TH}\right)^2 \cdot W_1 \cdot \mu_1 \cdot \frac{C_{ox}}{L_1} \cdot 2 = \left(VDD - V_{TH} - V_{out}\right)^2 \cdot W_2 \cdot \mu_n \cdot \frac{C_{ox}}{L_2} \cdot 2$$

Saturation condition $V_{out} = V_{in} - V_{TH}$

$$\left(V_{in} - V_{TH}\right)^2 \cdot W_1 \cdot \mu_n \cdot \frac{C_{ox}}{L_1} \cdot 2 = \left(V_{DD} - V_{TH} - \left(V_{in} - V_{TH}\right)\right)^2 \cdot W_2 \cdot \mu_n \cdot \frac{C_{ox}}{L_2} \cdot 2$$

$$7 \cdot \left(V_{in} - V_{TH}\right) = 3 \cdot \left(V_{DD} - V_{TH}\right)$$

$$10 \cdot V_{in} = 13.9$$

$$V_{in} = 1.39\,\text{V}$$

2b4.

$$I = \frac{V_{g2} + 2.5V}{R} = \frac{\beta}{2} \cdot \left(V_{g2} - V_{g1} - V_{TH2}\right)^2 = \frac{\beta}{2} \cdot \left(V_{g1} - 2.5 - V_{TH1}\right)^2$$

$$V_{g2} - V_{g1} - V_{TH2} = V_{g1} - 2.5 - V_{TH1}$$

$$V_{g1} = \frac{V_{g2} - 2.5}{2}$$

$$I = \frac{2 \cdot V_{g1}}{R} = \frac{\beta}{2} \cdot \left(V_{g1} - 2.5 - V_{TH1}\right)^2$$

2b5.

$I_{D2}=I_{ref}\,((W_2/L_2)/(W_1/L_1))$

$|I_{D3}|=|I_{D2}|$

$I_{D4}=I_{D3}\,((W_4/L_4)/(W_3/L_3))$

$I_{D4}=I_{ref}\,((W_2/L_2)/(W_1/L_1))((W_4/L_4)/(W_3/L_3))$

$I_{D4}=I_{ref}\,((W_2L_1)/(W_1L_2))((W_4L_3)/(W_3L_4))$

$$I_{D4} = I_{ref}\,\frac{W_2 W_4 L_1 L_3}{W_1 W_3 L_2 L_4}$$

2b6.

$$R = \frac{V_{DD} - V_{ref}}{I}$$

$$I = \frac{\beta}{2}(V_{GS} - V_{THN})^2 = \frac{\beta}{2}(V_{ref} - V_{THN})^2$$

$$\beta = K_n \frac{W}{L} = \mu_n \frac{\varepsilon_{Si} \cdot \varepsilon_0}{t_{ox}} \cdot \frac{W}{L} = 120 \text{ uA/V}^2$$

$$I = 0.6 \cdot 10^{-4}(V_{ref} - 0.8)^2$$

$$V_{ref} = V_{DD} - IR$$

$$V_{ref} = 2 - 10^4 \cdot 10^{-4} \cdot 0.6(V_{ref} - 0.8)^2$$

$$V_{ref} = 2 - 0.6(V^2{}_{ref} - 1.6V_{ref} + 0.64)$$

$$V_{ref} = 2 - 0.6V^2{}_{ref} + 0.96V_{ref} - 0.384$$

$$-0.6V^2{}_{ref} - 0.04V_{ref} + 1.616 = 0$$

$$0.6V^2{}_{ref} + 0.04V_{ref} - 1.616 = 0$$

$$V_{ref\,1,2} = \frac{-0.04 \pm \sqrt{0.0016 + 3.8784}}{1.2}$$

$$V_{ref\,1,2} = \frac{-0.04 \pm 1.97}{1.2}$$

$$V_{ref} = \frac{-0.04 + 1.97}{1.2} = 1.675\,\boldsymbol{V}$$

2b7.

a) When V_{DD} increases by 10%.

$$I_{out} = \frac{\beta}{2}(V_A - V_{TH})^2$$

$$V_A = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$\Delta I_{out} = \frac{\beta}{2}[(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH})^2 - (\frac{R_2}{R_1 + R_2}1.1V_{DD} - V_{TH})^2]$$

$$\beta = K_n \frac{W}{L} = 120 \cdot 10^{-6} \cdot \frac{50}{0.5} = 12\,\mu A/V^2$$

$$\Delta I_{out} = 6 \cdot 10^{-3}[(0.78 - 0.5)^2 - (0.858 - 0.5)^2] = 6 \cdot 10^{-3}(0.0784 - 0.128) \approx -0.3$$

$\Delta I_{out} = -0.3$ mA (increases by 0.3 mA)

b) When V_{DD} reduces by 10%.

$$\Delta I_{out} = \frac{\beta}{2}[(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH})^2 - (\frac{R_2}{R_1 + R_2}0.9V_{DD} - V_{TH})^2]$$

$$\Delta I_{out} = 6 \cdot 10^{-3}(0.0784 - 0.0408) \approx 0.23$$

$\Delta I_{out} = 0.23$ mA (reduces by 0.23 mA)

2b8.

$$K = -\frac{R_2 \,//\, X_C}{R_1}$$

$$K = -\frac{R_2 \cdot \frac{1}{j\omega C}}{R_1(R_2 + \frac{1}{j\omega C})}$$

$$K = -\frac{R_2}{R_1(j\omega R_2 C + 1)} = -\frac{R_2}{R_1} \cdot \frac{1 - j\omega R_2 C}{1 + \omega^2 R_2{}^2 C^2}$$

$$|K| = \frac{R_2}{R_1} \cdot \frac{1}{\sqrt{1 + \omega^2 R_2{}^2 C^2}}$$

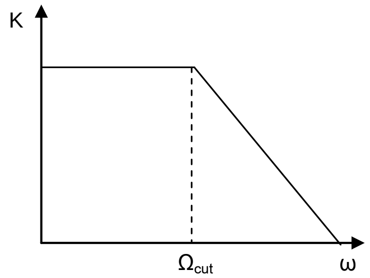
$$\omega = 0 \Rightarrow \quad K = -\frac{R_2}{R_1}, \quad \frac{\frac{R_2}{R_1} \cdot \frac{1}{\sqrt{1 + \omega^2 R_2{}^2 C^2}}}{\frac{R_2}{R_1}} = \sqrt{2}$$

$$\frac{1}{\sqrt{1 + \omega^2 R_2{}^2 C^2}} = \frac{1}{\sqrt{2}}$$

$$1 + \omega^2 R_2{}^2 C^2 = 2$$

$$\omega^2 R_2{}^2 C^2 = 1 \qquad \omega_{cut} = \frac{1}{R_2 C}$$

$$\omega \gg \frac{1}{R_2 C} \Rightarrow K \to 0$$



2b9.

$$I_D = I_{OUT} = (V_{GS} - V_{TH})\frac{g_m}{2}$$

$$V_{GS} = V_G = \frac{R_2}{R_1 + R_2} \cdot VDD$$

Putting together the following will be obtained:

$$I_{OUT} = (\frac{R_2}{R_1 + R_2} \cdot VDD - V_{TH}) \cdot \frac{g_m}{2}$$

2b10.

$$V_{OUT} = VDD - R_D(I_D + \frac{V_{OUT} - V_{in}}{R_F})$$

$$V_{OUT} = \frac{VDD - R_D I_D - \frac{R_D}{R_F} V_{in}}{1 + \frac{R_D}{R_F}}$$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$

$$V_{GS} = V_b - V_{in}$$

$$V_{OUT} = \frac{VDD - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_B - V_{in} - V_{TH})^2 - \frac{R_D}{R_F} V_{in}}{1 + \frac{R_D}{R_F}}$$

2b11.

$$V_- = -\frac{V_{out}}{K_A}$$

$$I_4 = I_1 + I_2 + I_3$$

$$\frac{V_- - V_{out}}{R_4} = \frac{V_{in1} - V_-}{R_1} + \frac{V_{in2} - V_-}{R_2} + \frac{V_{in3} - V_-}{R_3}$$

$$\frac{-\frac{V_{out}}{K_A} + V_{out}}{R_4} = \frac{V_{in1} + \frac{V_{out}}{K_A}}{R_1} + \frac{V_{in2} + \frac{V_{out}}{K_A}}{R_2} + \frac{V_{in3} + \frac{V_{out}}{K_A}}{R_3}$$

$$-V_{out}(1+\frac{1}{K_A}) \cdot R_1 R_2 R_3 = V_{in1} \cdot R_4 R_2 R_3 + V_{out}\frac{1}{K_A} \cdot R_4 R_2 R_3 + V_{in2} R_4 R_1 R_3 +$$

$$+V_{out} \cdot \frac{1}{K_A} \cdot R_4 R_1 R_3 + V_{in3} \cdot R_4 R_1 R_2 + V_{out}\frac{1}{K_A} R_4 R_1 R_2$$

$$V_{out}(\frac{1}{K_A} R_4 (R_2 R_3 + R_1 R_3 + R_1 R_2) + (1+\frac{1}{K_A}) \cdot R_1 R_2 R_3) = -R_4 (V_{in1} R_2 R_3 + V_{in2} R_1 R_3 + V_{in3} R_1 R_2)$$

$$V_{out} = -\frac{R_4 (V_{in1} R_2 R_3 + V_{in2} R_1 R_3 + V_{in3} R_1 R_2)}{\frac{1}{K_A} R_4 (R_2 R_3 + R_1 R_3 + R_1 R_2) + (1+\frac{1}{K_A}) \cdot R_1 R_2 R_3}$$

2b12.

$$I_{m1} = I_{ref}$$

$$I_{m2} = 5 \cdot I_{m1} = 5 \cdot I_{ref}$$

$$I_{m3} = I_{m2} = 5 I_{ref}$$

$$I_{m4} = 5 I_{m3} = 25 I_{ref}$$

$$V_{out} = R_1 \cdot I_{m4} = 25 I_{ref} R_1$$

2b13.

$$|I_{D1}| = |I_{ref}|, \qquad I_{D2} = I_{D1} \left(\frac{W_2}{L_2}\right) \Big/ \left(\frac{W_1}{L_1}\right) = I_{ref}$$

$$|I_{D3}| = |I_{D2}|, I_{D3} = I_{ref}$$

$$I_{D4} = I_{D3} \left(\frac{W_4}{L_4}\right) \Big/ \left(\frac{W_3}{L_3}\right) = 0.5 I_{ref}$$

2b14.

$$I_{out} = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_A - V_{TH})^2, \qquad V_A = \frac{V_{DD}}{R_1 + R_2} R_2$$

$$\Delta I_{out} = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}\left[\left(\frac{V_{DD}}{R_1 + R_2} R_2 - V_{TH}\right)^2 - \left(\frac{1.1 V_{DD}}{R_1 + R_2} R_2 - V_{TH}\right)^2\right]$$

$$\Delta I_{out} = -\frac{1}{2}\mu_n c_{ox}\frac{W}{L}\left[0.21\left(\frac{V_{DD}}{R_1 + R_2} R_2\right)^2 - 0.2\frac{V_{DD}}{R_1 + R_2} R_2 V_{TH}\right]$$

2b15.

$$R = \frac{V_{DD} - V_{ref}}{I}$$

$$I = I_1 + I_2 = \frac{V_{ref}}{R_1 + R_2} + \frac{\beta}{2}\left(\frac{V_{ref}}{R_1 + R_2} R_2 - V_{TH}\right)^2$$

$$R = \frac{V_{DD} - V_{ref}}{\frac{V_{ref}}{R_1 + R_2} + \frac{\beta}{2}\left(\frac{V_{ref}}{R_1 + R_2} R_2 - V_{TH}\right)^2}$$

2b16.
Relative to variable component

$$I_D = g_m V_{gs}$$

$$V_{out} = I_{D3} * R_1$$

$$\frac{I_{D3}}{g_{m3}} = \frac{I_{D2}}{g_{m2}}, \qquad I_{D2} = I_{D1} = g_{m1} V_{in}$$

$$V_{out} = \frac{g_{m1} g_{m3} R_1}{g_{m2}} V_{in}$$

$$k = \frac{dV_{out}}{dV_{in}} = \frac{g_{m1} g_{m3} R_1}{g_{m2}}$$

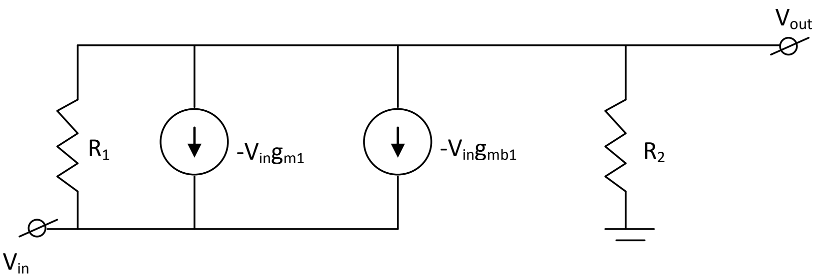
2b17.

$$\left.\begin{aligned} V_{out} &= I_2 R_1 \\ \frac{I_2}{I_1} &= \frac{g_{m3}}{g_{m2}} \\ I_1 &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{THn})^2 \end{aligned}\right\} \Rightarrow V_{out} = R_1 \frac{g_{m3}}{g_{m2}} \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{in} - V_{THn})^2$$

$$A_V = \frac{\partial V_{out}}{\partial V_{in}} = R_1 \frac{g_{m3}}{g_{m2}} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{in} - V_{TH}) = \frac{R_1 g_{m3} g_{m1}}{g_{m2}}$$

Answer: $A_V = \dfrac{R_1 g_{m3} g_{m1}}{g_{m2}}$

2b18.
The small signal model of the circuit is the following.



The following equation can be written for that:

$$-\frac{V_{out}}{R_2} + \frac{V_{in} - V_{out}}{R_1} + g_{m1} V_{in} + g_{mb1} V_{in} = 0$$

$$-V_{out} \frac{1}{R_2 \,//\, R_1} = -V_{in} \left(\frac{1}{R_1} + g_{m1} + g_{mb1}\right)$$

$$A_V = \frac{V_{out}}{V_{in}} = R_2 \,//\, R_1 \left(\frac{1}{R_1} + g_{m1} + g_{mb1}\right)$$

Answer: $R_2 \,//\, R_1 \left(\dfrac{1}{R_1} + g_{m1} + g_{mb1}\right)$

2b19.

The voltage of V1 can be obtained from

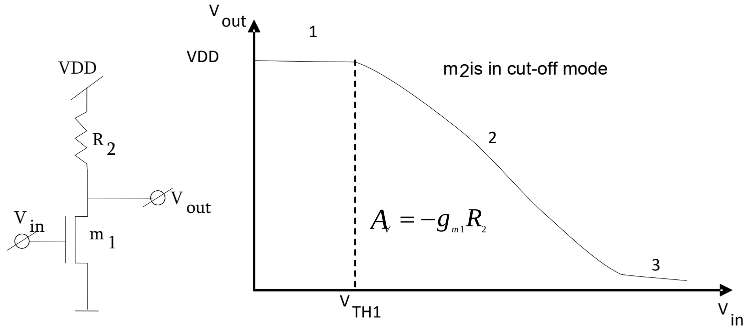
$$V_1 = VDD - \frac{VDD - V_{out}}{1 + \dfrac{R_2}{R_1}}$$

Depending on the ratio of R_2 and R_1 values, 5 cases can be obtained which are:

1)

$$R_1 \langle\langle R_2 \Rightarrow \left(\frac{R_2}{R_1} + 1\right) \to \infty \Rightarrow V_1 \approx VDD - \frac{VDD - V_{out}}{\infty} \approx VDD$$

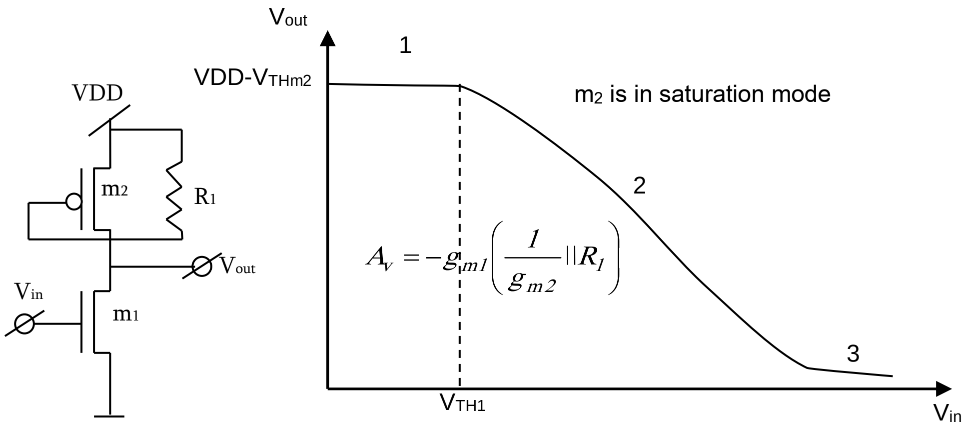
In this case m_2 will be in cut-off mode irrespective of V_{in} value, and the circuit will have the following view:



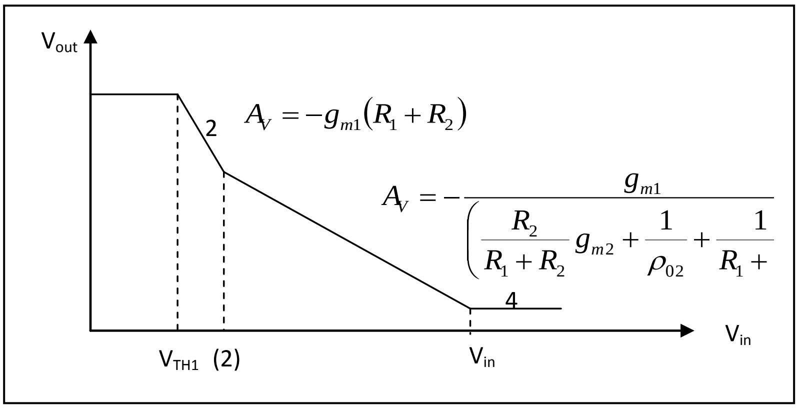
1. m_1 is in cut-off mode
2. m_1 is in saturation mode
3. m_1 is in triode mode

2) $R_1 \rangle\rangle R_2 \Rightarrow \dfrac{R_2}{R_1} \to 0 \Rightarrow V_1 = VDD - VDD + V_{out} = V_{out}$

In this case m_2 can be observed as a diode connection and it will be in saturation mode irrespective of V_{in} value, the circuit will have the following view:



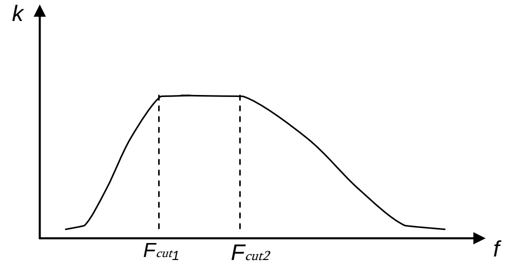
The values of R_1 and R_2 are proportional, in this case, depending on V_{out} -V_{in}, the following curve will be obtained:



1. m_1 and m_2 are in cut-off mode
2. m_1 is in saturation mode, m_2 - in cut-off mode
3. m_1 and m_2 are in saturation mode, (2) point of Vin axis is the value when $|V_1 - VDD| > |VTH_2|$
4. m_1 is in triode mode, m_2 is in saturation

2b20.

1) $K_{cut} = \left(1+\frac{R_3}{R_1}\right) = 11$



$$f_{cut1} = \frac{1}{2\pi C_1 R_2} = \frac{1}{6{,}28\cdot 10^{-5}\cdot 2\cdot 10^3 ohm} = \frac{1000}{12.56} \approx 8Hz$$

$$f_{cut2} = \frac{1}{2\pi C_2 R_3} = \frac{1}{6.28\cdot 10^{-6}\cdot 10\cdot 10^3 ohm} = \frac{1000}{62.8} \approx 16Hz$$

2) C_1,R_2 is a high pass filter.
   C_2R_3 is a low pass filter.
   $\Delta f = f_{kt2} - f_{kt1} = 16Hz - 8Hz = 8Hz$
   $f_{kentr} = \frac{f_{kt1} + f_{kt2}}{2} = 12Hz$

2b21.

After the sampling with the period of Δt=1/f_s=0.001 seconds, a discrete signal can be obtained

$u(n\Delta t) = \cos(2\pi f_0 n\Delta t) = \cos\frac{\pi f_0 n}{500} = x(n) = \cos\frac{\pi n}{4}$, $n\in$Z.

Equation $\cos\frac{\pi f_0 n}{500} = \cos\frac{\pi n}{4}$ in view of the evenness and periodicity of the cosine function is performed for all n, if $\frac{\pi f_0}{500} n = \left(\pm\frac{\pi}{4} + 2\pi j\right) n$, or $f_0 = \pm 125 + 1000 j$ (Hz), where number j is any integer.

Hence the two minimum values of the frequency:

$f_0 = 125$ Hz (no superposition of frequency as f_0 = 125<f_s / 2=500 Hz, conditions of Nyquist theorem are performed), $f_0 = -125 + 1000 = 875$ Hz (conditions of Nyquist theorem are not performed).

Answer: 125 Hz, 875 Hz.

2b22.

See the solution of 2b21.

Answer 700 Hz, 900 Hz.

2b23.

As the sources of all transistors are connected to supply voltages, there is no body effect here.

The circuit can be divided into 2 parts: the 1st part represents unicascade amplifier with diode load the input of which is V_{input} and the output V_1 and the amplification coefficient will be:

$$A_1 = -g_{m1}\left(\frac{1}{g_{m2}} \,||\, r_{01}\right)$$

The 2nd part is a unicascade amplifier with resistive load the input of which is V_1, the output V_{output} and the amplification coefficient will be:

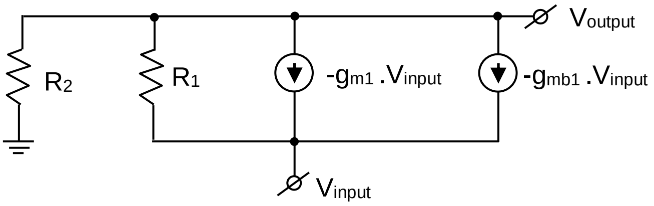
$$A_2 = -g_{m3}(r_{03}||R_1)$$

The total amplification will be $A_1 \cdot A_2 \Rightarrow$

$$A = g_{m1}\cdot g_{m3}\cdot\left(\frac{1}{g_{m2}} \,||\, r_{01}\right)\cdot(r_{03} \,||\, R_1)$$

2b24.

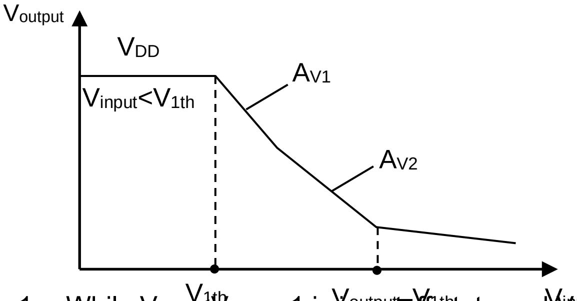
Design the small signal model of the circuit:



$$(V_{output}-V_{input})/R_1-(g_{m1}+g_{mb1})V_{input}=-V_{output}/R_2$$

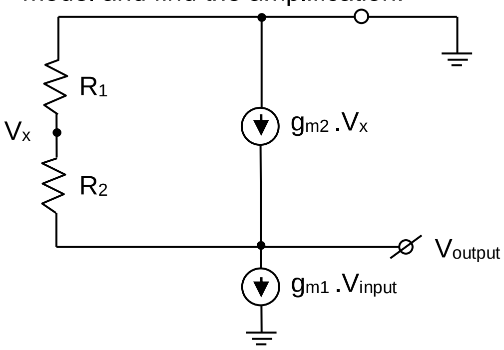
$$A_v=V_{output}/V_{input}=(1+R_1(g_{m1}+g_{mb1}))R_2/(R_2+R_1)$$

2b25.



1. While $V_{input}<V_{1th}$, m1 is in cutoff state and $V_{output}=V_{DD}$.
2. When $V_{input}>V_{1th}$ and while $V_{output}\geq V_{input}-V_{1th}$, m1 is in saturation state and further increase of V_{input} will lead to the increased reduction of V_{output}. During further increase of V_{input}, first m2 will be in cutoff state (while $|V_{DD}-V_x|<|V_{2th}|$), then the gain will be:
$$A_{v1}=-g_{m1}(R_1+R_2).$$

When m2 goes into saturation state, $|V_{DD}-V_{output}|\geq|V_{DD}-V_x|-|V_{2th}|$ the gain will change. Design the small signal model and find the amplification:

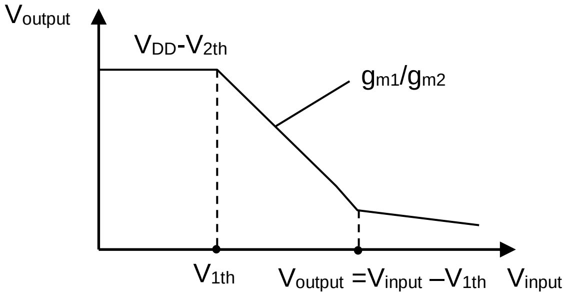


$$g_{m1}\cdot V_{input}=-\frac{V_{output}}{R_1+R_2}-g_{m2}\cdot R_1\cdot\frac{V_{output}}{R_1+R_2}$$

$$A_{v2}=\frac{V_{output}}{V_{input}}=-\frac{g_{m1}(R_1+R_2)}{1+g_{m2}\cdot R_1}$$

3. When $V_{input}=V_{output}-V_{1th}$ m1 transistor will go into triode state and V_{output} will tend to 0.

2b26.



1. While $V_{inpuy}<V_{1th}$, m1 is in cutoff state and $V_{output}\approx V_{DD}-V_{2th}$, as m2 is a diode connected transistor.
2. When $V_{input}>V_{1th}$ and $V_{output}\geq V_{input}-V_{1th}$ m1 is in saturation state and the circuit represents a unicascade amplifier. Design a small signal model and find A_v.

2b27.

$$\begin{bmatrix} G_1+j\omega C_1 & -G_1-j\omega C_1 & 0 & 0 \\ -G_1-j\omega C_1 & G_1+j\omega C_1 & 0 & 0 \\ 0 & 0 & G_2+j\omega C_2 & 1 \\ k & -k & 0 & 1 \end{bmatrix}\cdot\begin{bmatrix} u_{n1} \\ u_{n2} \\ u_{n3} \\ i_1 \end{bmatrix}=\begin{bmatrix} I_0 \\ -I_0 \\ 0 \\ 0 \end{bmatrix}$$

2b28.

a)

V_{tnew} = 0.4 – 0.1 = 0.3V

$I_{ds} = C_{ox}W(1.2-0.4)v_{sat} = C_{ox}\cdot W\cdot v_{sat}\cdot 0.8$; and

$I_{ds} = C_{ox}W(1.2-0.3)v_{sat} = C_{ox}\cdot W\cdot v_{sat}\cdot 0.9$

the saturation current will increase by x1.125

b)

$$\frac{I_{sub1}}{I_{sub2}} = I_s e^{\frac{-qV_{t1}}{nkT}}\left(1-e^{\frac{-qV_{dd}}{kT}}\right)\Big/ I_s e^{\frac{-qV_{t2}}{nkT}}\left(1-e^{\frac{-qV_{dd}}{kT}}\right) = e^{\frac{q}{nkT}(V_{t2}-V_{t1})} = e^{\frac{q}{nkT}(-0.1)} = 0.063$$

Isub2/Isub1 = 15.8

c)

Changing Vt and T

$$\frac{I_{sub1}}{I_{sub2}} = I_s e^{\frac{-qV_{t1}}{nkT1}}\left(1-e^{\frac{-qV_{dd}}{kT1}}\right)\Big/ I_s e^{\frac{-qV_{t2}}{nkT2}}\left(1-e^{\frac{-qV_{dd}}{kT2}}\right) = 0.0089$$

Isub2/Isub1 = 112.35

Changing T only

$$\frac{I_{sub1}}{I_{sub2}} = I_s e^{\frac{-qV_{t1}}{nkT1}}\left(1-e^{\frac{-qV_{dd}}{kT1}}\right)\Big/ I_s e^{\frac{-qV_{t1}}{nkT2}}\left(1-e^{\frac{-qV_{dd}}{kT2}}\right) = 0.0733$$

Isub2/Isub1 = 13.64

The sub-threshold leakage will increase as the temperature increase,

d) Assume that the threshold voltage has to be reduced by increasing the body voltage (using body effect), what would be the value of V_{sb} to reach the targeted V_t.

$V_t = 0.4 + \gamma(\sqrt{2|\phi_F| + V_{sb}} - \sqrt{2|\phi_F|})$; then

$0.3 - 0.4 = 0.2(\sqrt{0.88 + V_{sb}} - \sqrt{0.88})$ => $V_{sb} = -0.688V$

2b29.

Approximate V_{t0} and t_{ox} then:

$$I_{ds} = C_{ox}W\frac{(V_{gs}-V_t)^2}{(V_{gs}-V_t)+E_cL}.\nu_{sat}$$

Assume E_cL = 0, then

$$I_{ds} = C_{ox}W(V_{gs}-V_t).\nu_{sat}$$

Substitute for I_{ds1} = 78.70μA and V_{gs1} = 1.2 V and I_{ds2} = 56.21μA and V_{gs2} = 1.0V then:

$$\frac{I_{ds1}}{I_{ds2}} = \frac{(V_{gs1}-V_{t0})}{(V_{gs2}-V_{t0})} = \frac{(1.2-V_{t0})}{(1.0-V_{t0})} = 1.4 \Rightarrow V_{t0} = 0.5V$$

substitute in one of the two equations, then t_{ox} = 10 nm.

2b30.

First find V_1 potential:

$$V_1 = \frac{VDD\cdot R_1 + V_x\cdot R_2}{R_1+R_2}$$

V_{DS1}: V_{DS1}=VDD-V_x

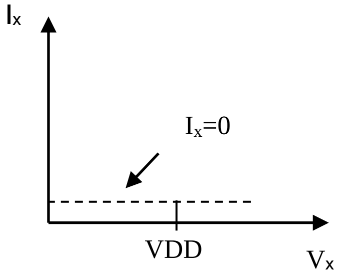
V_{gs1}: V_{gs1}= $\frac{R_1}{R_1+R_2}$ (VDD-V_x)

Note that M_1 cannot be in triode state for any values of V_x from 0 to VDD, as V_{DS1}> V_{gs1} – V_{TH}: Put V_{DS1} and V_{gs1} values in saturation inequality condition:

$$VDD - V_x > \frac{R_1}{R_1+R_2}(VDD-V_x) - V_{TH1}$$

As all the inequality members are positive, it is correct for any V_x.

Now change V_x from 0 to VDD. When V_x=0, M_1 can be either in saturation or cutoff state. Hence the problem gets two solutions:



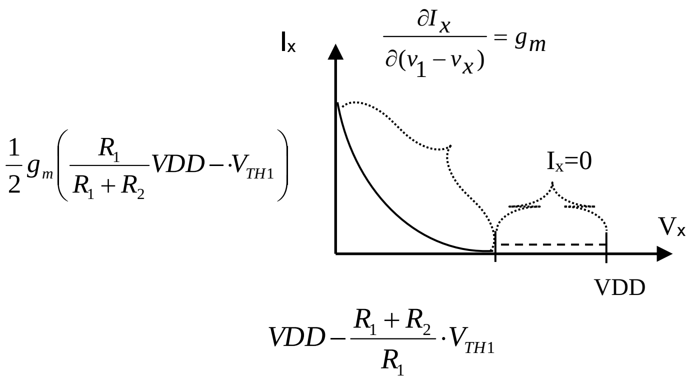
i. When $V_x=0$ and $V_{gs1}< V_{TH}$ - $\dfrac{R_1}{R_1+R_2}$ VDD< V_{TH}, M_1 is in cutoff state and $I_x=0$.

When $V_x \neq 0$, $V_{gs1}=\dfrac{R_1}{R_1+R_2}(VDD-V_x)$. In this case for positive V_x, M_1 will be in cutoff state since $\dfrac{R_1}{R_1+R_2}(VDD-V_x) < \dfrac{R_1}{R_1+R_2}$ VDD< V_{TH1}.

Therefore $I_x=0$, for any V_x values from 0 to VDD.

ii. When $V_x=0$ and $V_{gs1}> V_{TH1}$, i.e. $\dfrac{R_1}{R_1+R_2}$ VDD>V_{TH1}, then M_1 is in saturation mode (triode mode is already excluded) and

$$I_x=\frac{1}{2}g_m(V_{gs1}-V_{TH1})=\frac{1}{2}g_m\left(\frac{R_1}{R_1+R_2}VDD-V_{TH1}\right).$$



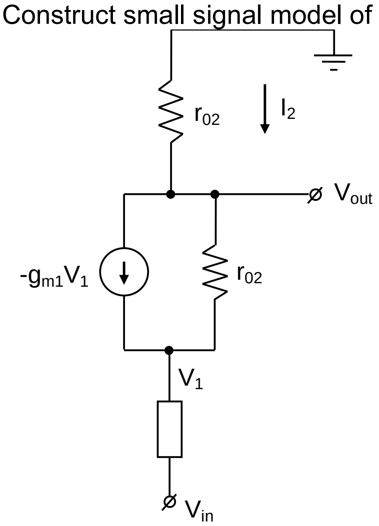
In parallel to V_x increase, I_x will start decreasing by $\dfrac{\partial I_x}{\partial(v_1-v_x)}=g_m$ law, and for some V_x , M_1 will pass to cutoff mode. Find the V_x, in case of higher values of which M_1 will be in cutoff state and $I_x=0$.

$$\frac{R_1}{R_1+R_2}(VDD\cdot V_x)=V_{TH} \Rightarrow$$

$$V_x=VDD-\frac{R_1+R_2}{R_1}V_{TH1}$$

2b31.

Construct small signal model of a circuit:



$V_{out} = -r_{02} I_2 \qquad (1)$

$I_2 = \frac{V_1 - V_{in}}{R_2} \qquad (2)$

$I_2 = \frac{V_{out} - V_1}{r_{01}} - g_{m1} V_1 \qquad (3)$

From (2) and (3) formulas, find I_2

$$I_2 = \frac{\frac{R_s V_{out} + r_{01} V_{in}}{r_{01} + R_s + g_{m1} R_s r_{01}} - V_{in}}{R_s} \qquad (4)$$

Put (4) equation in (1), and divide the right and left parts of the new equation by V_{in}

$$A_v = -\frac{\frac{R_s A_v + r_{01}}{r_{01} + R_s + g_{m1} R_s r_{01}} - 1}{R_s} r_{02}$$

From the obtained equation, A_v can be found.

$$A_v = \frac{r_{02}(1 + g_{m1} r_{01})}{r_{02} + r_{01} + R_3 + g_{m1} R_3 r_{01}}$$

2b32.

If U_{input}>0 and amplifier is inverse, U_{output}<0 and $U^- - U^+ = U_{output} / K'u > 0$

$I_1 = (U_{input} - U^-)/R_1$, $I_1 = (U_{input} - U_{output} / K'u) / R_1$,

$I_2 = I_1 - U^- / R'_{input} = (U_{input} - U_{out} / K'u) / R_1 - (U_{out} / K'u) / R'_{input}$

$U_{output} = U^- - I_2 * R_2 = U_{output} / K'u - ((U_{input} - U_{output} / K'u) / R_1 - (U_{output}/ K'u) / R'_{input}) * R_2 =$

$= U_{output} * (1/ K'u + (1/ K'u) * (R_2/R_1) +(1/ K'u) * (R_2/R'_{input})) - U_{in} * (R_2/R_1)$

Checking – when $K'u \rightarrow \infty$ and $R'_{input} \rightarrow \infty$, then $KU = U_{output}/U_{in} = - R_2/R_1$.

2b33.

If U_{input} >0 and amplifier is non-inverse, then U_{output}>0 , then $U^- - U^+ = U_{output} / K'u < 0$ and $U^- = U_{input} - U_{output} / K'u$

$I_1 = U^- / R_1 = I_1 = (U_{input} - U_{output} / K'u)/R_1$

$I_2 = I_1 + U^- / R'_{input} = (U_{input} - U_{output} / K'u)/R_1 + (U_{input} - U_{output} / K'u) / R'_{input}$

$U_{output} = U^- + I_2 * R_2 = U_{input} - U_{output} / K'u + ((U_{input} - U_{output} / K'u) / R_1) + (U_{input} - U_{output} / K'u) / R'_{input}) * R_2 =$

$=U_{input} + U_{input} * R_2/R_1 + U_{input} * R_2/R'_{input} + U_{output}t + U_{output} (1/ K'u) * (R_2/R_1) + U_{output} * (1/ K'u) * (R_2/R'_{input}))$

$=U_{input} (1 + R_2/R_1 + R_2/R'_{input}) - U_{output} (1/K'u + (1/ K'u) * (R_2/R_1) + (1/ K'u) * (R_2/R'_{input}))$

$U_{output} (1 + 1/ K'u + (1/ K'u) * (R_2/R_1) + (1/ K'u) * (R_2/R'_{input})) = U_{input} (1 + R_2/R_1 + R_2/R'_{input})$

$KU = U_{output}/U_{input} = (1 + R_2/R_1 + R_2/R'_{input}) / (1 + 1/ K'u + (1/ K'u) * (R_2/R_1) + (1/ K'u) * (R_2/R'_{input}))$

Checking – when $K'u \rightarrow \infty$ and $R'_{input} \rightarrow \infty$, then $KU = U_{output}/U_{input} = 1 + R_2/R_1$

2b34.

A1 operates as a linear inverse integrator, in the output of which triangle pulses with T period can be obtained. It equals to pulse periods at U_B and U_C outputs.

A2 and A3 are comparators. A2 has hysteresis characteristic due to positive feedback with R2, R3 resistors.

Calculation

1. As U_{BMAX}=5s and U_{BMIN}=-5s and R2=R3, then +2.5s and -2.5s values are obtained in the output of R2,R3 voltage divider, in the interval of which linear changing voltage of A1 integrator changes.

$$\Delta U_A = 2.5s - (-2.5s) = 5s$$

2. During integration, C is charged and discharged.

$$\Delta U_A = \frac{I_C \cdot \Delta t}{C}, \text{ where } I_C = U_{outA3MAX}/R1$$

3. Pulse difference:

$$T = 2 \cdot \Delta t = \frac{2\Delta U_A \cdot C \cdot R1}{U_{outA3MAX}} = \frac{2 \cdot 5s \cdot 0{,}1 \cdot 10^{-6} \cdot 20 \cdot 10^3 Ohm}{5s} = 4 \cdot 10^{-3} sec$$

2b35.

Repeating error occurs due to V open transistor's channel resistance ($R_{chan} \neq 0$), which together with R3 forms voltage divider. IfR_{chan}=0, then $U^+_{mA2} = U_m \cdot \frac{chan}{R2 + R_{vhan}}$ և

$$U_{out} = U^+_{mA2}\left(1 + \frac{R2}{R1}\right) - U_m \cdot \frac{R2}{R1} = U_m \frac{R_{chan}}{R2 + R_{chan}}\left(1 + \frac{R2}{R1}\right) - Um \cdot \frac{R2}{R1}$$

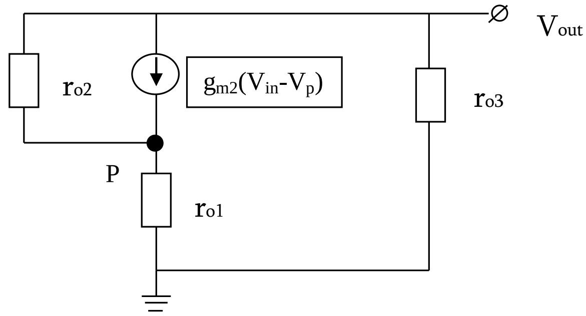
$$K = \frac{U_{out}}{U_m} = \frac{R_{chan}}{R2 + R_{chan}}\left(1 + \frac{R2}{R1}\right) - \frac{R2}{R1}$$

If R1=R2, then $K=\frac{\mathrm{R}chan}{\mathrm{R2+R}_{chan}}\cdot 2-1=\frac{0.14\cdot 2}{20.14}-1=\frac{2}{201}-1$

As for ideal repeater K=-1, then the error equals (accuracy is limited) $\frac{2}{201}$.

2b36.

Construct small signal model of the circuit:



The following equations of currents can be written for small signal model:

$$g_{m2}(V_{in}-V_p)+(V_{out}-V_p)/r_{o2}=V_p/r_{o1} \quad (1)$$

$$-\frac{V_{out}}{r_{o3}}=\frac{V_p}{r_{o1}} \quad (2)$$

From equation (1), find V_p:

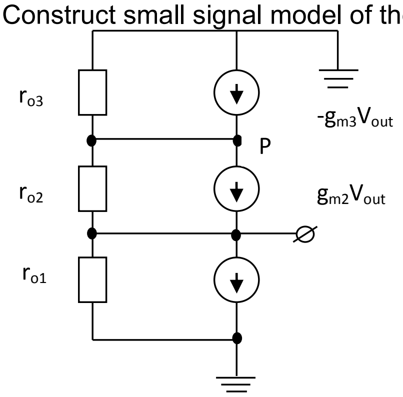
$$V_p=\frac{g_{m2}\cdot r_{o2}\cdot r_{o1}\cdot V_{in}+r_{o1}\cdot V_{out}}{g_{m2}\cdot r_{o1}\cdot r_{o2}+r_{o1}+r_{o2}}$$

Put Vp in equation (2) and find $A_v=\frac{V_{out}}{V_{in}}$ small signal gain coefficient:

$$\boldsymbol{A_v}=\frac{\mathbf{g_{m2}\cdot r_{o2}\cdot r_{o1}\cdot r_{o3}}}{\mathbf{r_{o1}^2\cdot g_{m2}\cdot r_{o2}+r_{o1}^2+r_{o2}\cdot r_{o1}+r_{o1}\cdot r_{o2}}}$$

2b37.

Construct small signal model of the circuit:



The following equations of currents can be written for small signal model:

$$-\frac{V_p}{r_{o3}}-g_{m3}\cdot V_{out}=\frac{V_p-V_{out}}{r_{o2}}-g_{m2}\cdot V_{out} \quad (1)$$

$$\frac{V_{out}}{r_{o1}}+g_{m1}\cdot V_{in}=-\frac{V_p}{r_{o3}}-g_{m3}\cdot V_{out} \quad (2)$$

From equation (1), find V_p:

$$V_p=\frac{V_{out}\cdot r_{o3}\left(1-r_{o2}\left(g_{m2}+g_{m3}\right)\right)}{r_{o2}+r_{o3}}$$

Put Vp in equation (2) and find $A_v=\frac{V_{out}}{V_{in}}$ small signal gain coefficient:

$$A_v=-\frac{g_{m1}}{\frac{1}{r_{o1}}+\frac{1-r_{o2}\left(g_{m2}+g_{m3}\right)}{r_{o2}+r_{o3}}+g_{m3}}$$

2b38.

A_1 is an adder $U_1=-(U_{IN}*R2/R1+U_{OUT}*R2/R5)$

A_1 is a repeater $U_2=-U_1=U_{IN}+U_{OUT}*R2/R5$

$(U_2-U_{OUT})/R6=U_{OUT}/R5+I_L$

$U_{IN}/R6+U_{OUT}*R2/(R5*R6)-U_{OUT}/R6-U_{OUT}/R5=I_L$

$I_L=U_{IN}/R6+U_{OUT}*(R2/(R5*R6)-1/R6-1/R5)$;

$I_L = U_{IN} / R6$ if $(R2 - R5 - R6) / (R6 * R5) = 0 \Rightarrow R2 = R5 + R6$

2b39.

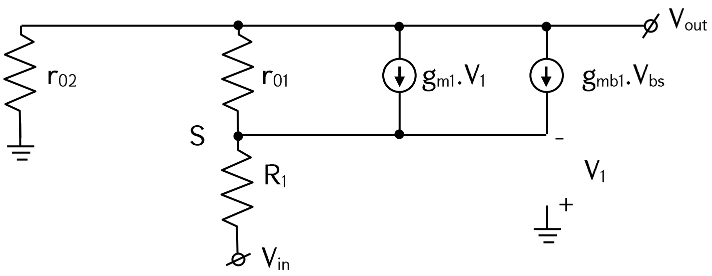
$U_A = U_B$; $U_{R4} = U_{R3}$; $I_4 * R4 = I_3 * R3$

$I_4 * R4 = (I_2 + I_L) * R3$; $(U_A - U_{IN}) * R4 / R1 = (U_B / R2 + I_L) * R3$; $(U_B - U_{IN}) * R4 / R1 = (U_B / R2 + I_L) * R3$

From initial condition: $R3 = R2 * R4 / R1$, then $U_B - U_{IN} = (U_B / R2 + I_L) * R2$ and $I_L = - U_{IN} / R2$

2b40.

Build the small signal model of the circuit.



$$-\frac{V_{out}}{r_{02}} = \frac{V_s - V_{in}}{R_1} \quad (1)$$

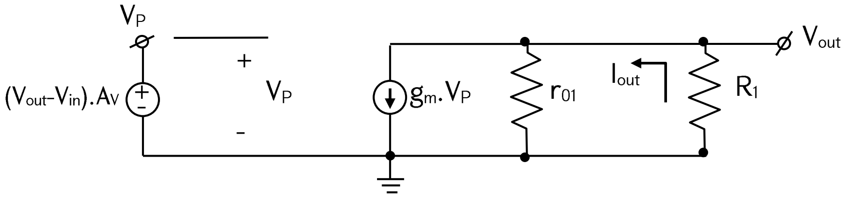
$$-\frac{V_{out}}{r_{02}} = \frac{V_{out} - V_s}{r_{01}} - g_{m1} \cdot V_S - g_{mb1} \cdot V_S \quad (2)$$

From (1) find V_S, put in (2), hence $A_V = \frac{dV_{out}}{dV_{in}}$ gain can be found.

$$A_V = \frac{r_{02}(1 + r_{01}(g_{m1} + g_{mb1}))}{r_{01} + r_{02} + R_1(1 + r_{01}(g_{m1} + g_{mb1}))}$$

2b41.

Build the small signal model of the circuit.



Instead of OpAmp, put voltage source, the value of which is $(V_{out}-V_{in}).A_V$

$$g_m \cdot V_P = -\frac{V_{out}}{r_{01} || R_1} \quad (1)$$

$$V_{out} = -I_{out} \cdot R_1 \quad (2)$$

$$V_P = (V_{out} - V_{in}) \cdot A_V \quad (3)$$

From these three equations, $G = \frac{dI_{out}}{dV_{in}}$ can be found.

$$\frac{I_{out}}{V_{in}} = -\frac{g_m A_V}{R_1\left(\frac{1}{r_{01} || R_1} + g_m A_V\right)}$$

$$G = -\frac{g_m A_V}{R_1\left(\frac{1}{r_{01} || R_1} + g_m A_V\right)}$$

2b42.
Since the threshold voltage of M_1 depends on V_{out}, perform a simple iteration. Note that:

$$(V_{in} - V_{TH} - V_{out})^2 = \frac{2I_D}{\mu_n C_{ox} (\frac{W}{L})_1}$$

First assume $V_{TH} \approx 0.6V$, obtaining $V_{out} = 0.153V$. Now calculate a new V_{TH} as

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}) = 0.635\,\mathrm{V} \ .$$

This indicates that V_{out} is approximately 35 mV less than that calculated above $V_{out} = 0.119V$.

2b43.
The small-signal drain current of M_1, $g_{m1}V_{in}$, is divided between R_p and the impedance seen looking into the source of M_2, $1/(g_{m2} + g_{mb2})$. Thus, the current flowing through M_2 is:

$$I_{D2} = g_{m1}V_{in} \frac{(g_{m2}+g_{mb2})R_P}{1+(g_{m2}+g_{mb2})R_P}$$

The voltage gain is therefore given by:

$$A_V = -\frac{g_{m1}(g_{m2}+g_{mb2})R_P R_D}{1+(g_{m2}+g_{mb2})R_P}$$

2b44.
Assume (somewhat arbitrarily) that M_3 and M_4 remain in deep triode region if $|V_{DS3,4}| \le 0.2 \,\mathrm{x}\, 2|V_{GS3,4} - V_{THP}|$. If each stage in the ring experiences complete switching, then the maximum drain current of M_3 and M_4 is equal to I_{SS}. To satisfy the above condition, it is necessary to have $I_{SS}R_{on3,4} \le 0.4(V_{DD} - V_{cont} - |V_{THP}|)$, and hence:

$$\frac{I_{SS}}{\mu_p C_{ox}(\frac{W}{L})_{3,4}(V_{DD} - V_{cont} - |V_{THP}|)} \le 0.4(V_{DD} - V_{cont} - |V_{THP}|)$$

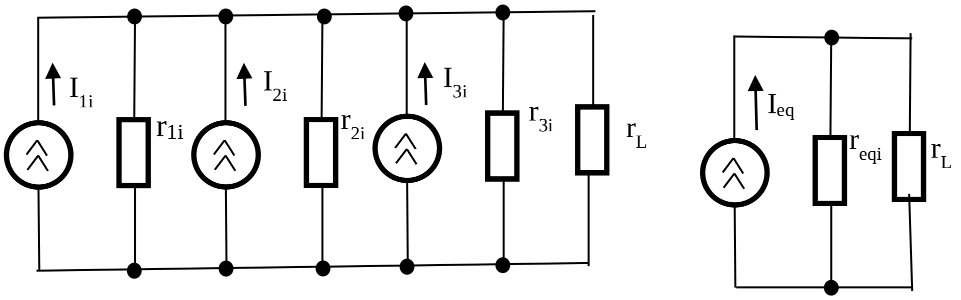
It follows that:

$$V_{cont} \le V_{DD} - |V_{THP}| - \sqrt{\frac{I_{SS}}{0.4\mu_p C_{ox}(\frac{W}{L})_{3,4}}}$$

If V_{cont} exceeds this level by a large margin, M_3 and M_4 eventually enter saturation. Each stage then requires common-mode feedback to produce the output swings around a well-defined CM level.

2b45.
$U_A = (U_{IN} / R_1) * R_2$; $U_A = (U_{OUT} * R_3 / (R_3 + R_4)$
$K_U = U_{OUT} / U_{IN} = (R_2/R_1) * (R_3 + R_4)/R_3) = 10 * 11 = 110$
2b46.
A_1 – adder $U_1 = - (U_{IN} * R_2/R_1 + U_{OUT} * R_2/R_5)$
A_2 – repeater $U_2 = -U_1 = U_{IN} + U_{OUT} * R_2/R_5$
$(U_2 - U_{OUT}) / R_6 = U_{OUT} / R_5 + I_L$
$U_{IN} / R_6 + U_{OUT} * R_2 / (R_5 * R_6) - U_{OUT} / R_6 - U_{OUT}/R_5 = I_L$
$I_L = U_{IN} / R_6 + U_{OUT} * (R_2 / (R_5 * R_6) - 1 / R_6 - 1/R_5)$
$I_L = U_{IN} / R_6$ if $(R_2 - R_5 - R_6) / (R_6 * R_5) = 0$ $\Rightarrow$ $R_5 = R_2 - R_6$

2b47.
Voltage sources are replaced by current sources.



$I_{1i}=E_1/r_1=4/20=0,2A$;
$I_{2i}=E_2/r_2=8/5=1,6A$;
$I_{3i}=E_3/r_3=2,4/12=0,2A$;
$1/r_{eqi}=1/r_{1i} + 1/r_{2i} + 1/r_{3i} = 1/20 +1/5 + 1/12 =1/3$; $r_{eqi}=3Ohm$;
$I_{eq}=I_{1i}+ I_{2i}+ I_{3i}=0,2+1,6+0,2=2A$;
$E_{eq}=I_{eq}r_{eqi}=2*3=6V$;
$r_{eq}=r_{eqi}=3Ohm$
$I= E_{eq}/(r_{eq}+r_L)=6/(3+7)=0,6A$;
$I_1=(E_1-Ir_L)/r_1=(4-0,6*7)/20 =-0,01A$;
$I_2=(E_2-Ir_L)/r_2=(8-0,6*7)/5 =0,76A$;
$I_3=(E_3-Ir_L)/r_3=(2,4-0,6*7)/12 =-0,15A$;

2b48.

$$I_D = \cdot (V_{GS} - V_T)^2$$
$$I_D = \frac{V_{DD}-V_D}{R_D} = \frac{V_S}{R_S};$$
$$V_{GS} = V_G - I_D \cdot R_S$$
$$V_{SB} = I_D \cdot R_S$$
$$V_T = V_{T0} + B\left[\sqrt{I_D \cdot R_S + 2\emptyset_f} - \sqrt{2\emptyset_f}\right]$$
$$I_D = A \cdot (V_G - I_D \cdot R_S - V_{T0} - B\sqrt{I_D \cdot R_S + 2\emptyset_f} + B\sqrt{2\emptyset_f}\ )^2$$
$$I_D = A \cdot (V_G - I_D \cdot R_S - V_T\ )^2$$
$$\frac{I_D}{A} = (V_G - V_T)^2 - 2(V_G - V_T)I_D \cdot R_S + (I_D \cdot R_S)^2$$
$$R_S{}^2 \cdot (I_D)^2 - \left(\frac{1}{A} + 2 \cdot (V_G - V_T) \cdot R_S\right) \cdot I_D + (V_G - V_T)^2 = 0$$
$$1 \cdot 10^3 I_D = (0.6)^2 - 2 \cdot (0.6V)I_D \cdot 1 \cdot 10^3\Omega + 1 \cdot 10^6 (I_D)^2$$
$$1 \cdot 10^6 (I_D)^2 - 2.2 \cdot 10^3 I_D + 0.36 = 0$$
$$I_D = \frac{2.2 \cdot 10^3 \pm \sqrt{4.84 \cdot 10^6 - 4 \cdot 0.36 \cdot 10^6}}{2 \cdot 10^6} = \frac{2.2 \cdot 10^3 \pm \sqrt{3.4} \cdot 10^3}{2 \cdot 10^6} = \frac{2.2 \pm 1.84}{2} 10^{-3} = \frac{4.04}{2} \cdot 10^{-3} \approx 2\ mA$$
$$V_D = V_{DD} - I_D \cdot R_D = 5 - 2 \cdot 10^{-3} \cdot 1.5 \cdot 10^3 = 2\ V$$

3. RF CIRCUITS

a) Test questions

3a1. A
3a2. A
3a3. B

4. SEMICONDUCTOR PHYSICS AND ELECTRONIC DEVICES

a) Test questions

4a1. D
4a2. A
4a3. B
4a4. C
4a5. B
4a6. B
4a7. C
4a8. C
4a9. A
4a10. B
4a11. A
4a12. C
4a13. B
4a14. D
4a15. E
4a16. A
4a17. C
4a18. C
4a19. C
4a20. B
4a21. E
4a22. C
4a23. C
4a24. C
4a25. E
4a26. C
4a27. B
4a28. C
4a29. C
4a30. A
4a31. D
4a32. E
4a33. C
4a34. C
4a35. B
4a36. C
4a37. C
4a38. C
4a39. B
4a40. D
4a41. D
4a42. D
4a43. B
4a44. B
4a45. B
4a46. B
4a47. C
4a48. A
4a49. D
4a50. B
4a51. A
4a52. B
4a53. C
4a54. C
4a55. B
4a56. B
4a57. B
4a58. C
4a59. B
4a60. D
4a61. D
4a62. C
4a63. C
4a64. C
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4a66. C
4a67. C
4a68. E
4a69. C
4a70. C
4a71. D
4a72. B
4a73. E
4a74. E
4a75. D
4a76. E
4a77. C
4a78. A
4a79. E
4a80. D
4a81. C
4a82. C
4a83. B
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4a85. D
4a86. A
4a87. C
4a88. D
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4a91. C
4a92. D
4a93. B
4a94. E
4a95. D
4a96. C
4a97. B
4a98. D
4a99. B
4a100. B
4a101. E
4a102. E
4a103. C
4a104. D
4a105. A
4a106. B
4a107. E
4a108. B
4a109. A
4a110. D
4a111. E
4a112. A
4a113. B
4a114. D
4a115. A
4a116. D
4a117. B
4a118. A
4a119. B
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4a122. A
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4a136. C
4a137. E
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4a144. E
4a145. B
4a146. B
4a147. E
4a148. C
4a149. D
4a150. B
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4a153. B
4a154. C
4a155. D
4a156. A
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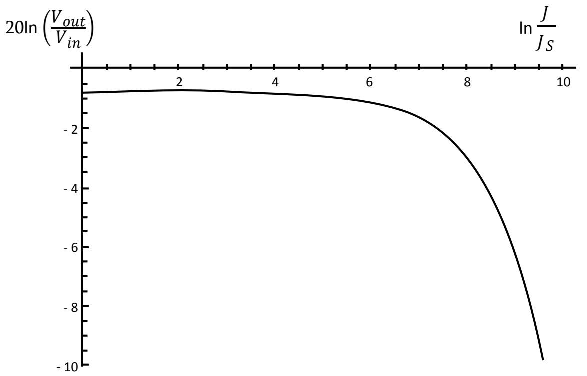
4a176. E
4a177. C
4a178. B
4a179. C
4a180. B
4a181. D
4a182. B
4a183. C
4a184. E
4a185. B
4a186. E
4a187. E
4a188. E
4a189. E

b) Problems
4b1.

Diode's current-voltage characteristic: $J = J_s(e^{\frac{eV}{kT}} - 1)$ can be introduced by the following way: $\frac{dJ}{dV} = J_s \frac{e}{kT} exp\left(\frac{eV}{kT}\right) = \frac{e}{kT}(J_s + J)$, from which for diode's differential resistance this will be obtained: $r = \frac{dV}{dJ} = \frac{kT}{e(J_s + J)}$.

In the shown circuit, for signal decay there is: $\frac{V_{out}}{V_{in}} = \frac{r}{r+R} = \frac{\frac{kT}{e(J+J_s)}}{\frac{kT}{e(J+J_s)} + R}$

The final view of decay expressed by decibels: $20\,ln\frac{V_{out}}{V_{in}} = 20\;ln\frac{\frac{kT}{e(J+J_s)}}{\frac{kT}{e(J+J_s)} + R}$:



The obtained dependence for the given parameters is shown in the figure.

4b2.

It is enough to be limited by the approximation of full depletion layer, according to which formation of a $p-n$ junction results in a depletion region at the p-n interface where the density of volume charge region is given by $\rho = -ekx$ expression. To find potential distribution, it is necessary to solve Poison equation in volume charge's $(-w,0)$ and $(0,w)$ regions: $\frac{d^2\varphi}{dx^2} = \frac{\rho}{\varepsilon\varepsilon_0} = -\frac{ekx}{\varepsilon\varepsilon_0}$:

The general solution of this equation will be: $\varphi(x) = -\frac{ekx^3}{6\varepsilon\varepsilon_0} + C_1x + C_2$,

where the appeared unknown constants should be found from angle conditions requiring that $\varphi(0) = 0$ (start of potential calculation) and $\frac{d\varphi}{dx}(\pm w) = 0$. In the result the following will be formed: $\varphi(x) = -\frac{ekx^3}{6\varepsilon\varepsilon_0} + \frac{ekw^2}{2\varepsilon\varepsilon_0}x.$

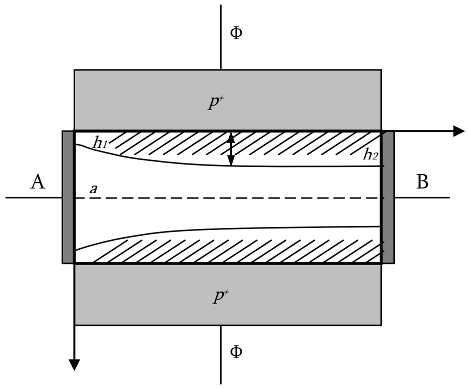
Considering that $\varphi(w) - \varphi(-w) = \psi - V$ the following will be got: $w = \sqrt[3]{\frac{\varepsilon\varepsilon_0(\psi - V)}{ek}}$:

The value of volume charge: $Q = A\int_0^w ekxdx = A\frac{ekw^2}{2} = A\frac{ek}{2}\left(\frac{\varepsilon\varepsilon_0(\psi-V)}{ek}\right)^{2/3}$, from which for junction capacitance the following will be formed: $C = \left|\frac{dQ}{dV}\right| = A\left(\frac{\varepsilon\varepsilon_0 ek}{12(\psi - V)}\right)^{1/3}$

Putting the data, the following will be written: $C \approx 46.5$ pf.

4b3.

The structure of the transistor is shown in the figure. It is convenient to insert the following function, describing the integral density of the charge:



$$Q(y) = \int_0^y \rho(y)dy \ , \ 0 \le y \le h(x) \ ,$$

where by the approximation of full depletion layer $\rho(y) = eN_D(y)$, and $h(x)$ is the width of depletion layer in $x = const$ plane. Reverse to V voltage, applied on $p^+ - n$ junction, it is necessary to use Poison equation in order to find the dependence of $h(x)$-and $\rho(y)$. Integrating it by y and considering that in $y = h(x)$ point the component of field intensity should be zero, the following will come out:

$$-\varepsilon_y = \frac{\partial\varphi}{\partial y} = \frac{1}{\varepsilon\varepsilon_0}\left[Q(h) - Q(y)\right]$$

This equation can be once more integrated according to y -0 to $h(x)$ considering that the change of potential should be equal to V .

$$V = \frac{1}{\varepsilon\varepsilon_0}\left[Q(h)\int_0^h dy - \int_0^h Q(y)dy\right] = \frac{1}{\varepsilon\varepsilon_0}\left[hQ(h) - \int_0^h Q(y)dy\right] = \frac{1}{\varepsilon\varepsilon_0}\int_0^h y\rho(y)dy$$

From here the following will be obtained:

$$\frac{dV}{dh} = \frac{h\rho(h)}{\varepsilon\varepsilon_0}$$

Now it is possible to go into transistor's calculation of current-voltage characteristic and transconductance. In every cross section of the channel $x = const$ current value is constant and equals:

$$I_D = -eZ\mu_n \frac{dV}{dx}\int_{2a-h}^{h} N_D(y)dy = eZ\mu_n \frac{dV}{dx} 2\int_h^a N_D(y)dy \ ,$$

where $\varepsilon_x = -\frac{dV}{dx}$ is the component of field intensity, and channel width equals $2(a-h)$. From the last equation, the following is formed:

$$I_D dx = 2eZ\mu_n dV\int_h^a N_D(y)dy = 2eZ\mu_n \frac{dV}{dh} dh\int_h^a N_D(y)dy \ ,$$

In this equation it has been considered that according to x (along the channel) change of potential takes place and if there is integration in the left part according to x from x=0 (start of the channel) to x=L (end of the channel),then on the right part it equals the change of potential from 0 to drain's V_D voltage. Pass from potential integration, according to h integration is also convenient. In the result,

$$I_D = \frac{2Z\mu_n}{\varepsilon\varepsilon_0 L}\int_{h_1}^{h_2}\left[Q(a) - Q(h)\right]h\rho(h)dh \ ,$$

Here h_1 and h_2 represent the edges of volume charge layer in x=0 and x=L cross sections (accordingly near the source and drain). According to definition, the transconductance will be:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\partial I_D}{\partial h_1}\frac{\partial h_1}{\partial V_G} + \frac{\partial I_D}{\partial h_2}\frac{\partial h_2}{\partial V_G}$$

where V_G is gate's (p^+- domain) voltage. The following is obtained:

$$g_m = \frac{2Z\mu_n}{L}\left[Q(h_2) - Q(h_1)\right].$$

4b4.
R_h=3.33*10^{-4} m^3/Cl,
ρ=8.93*10^{-3} Ohm*m,
β=0.5 Ml,
φ=?
$\varphi=\mu*\beta$, where μ is particle's mobility

$$\mu=\frac{R_h}{\rho}=\frac{3.33*10^{-4}}{8.93*10^{-3}}$$ m^2/(V*v)=3.73*10^{-2} m^2(V*v)

φ=3.73*10^{-2}*0.5=1.86*10^{-2} rad.

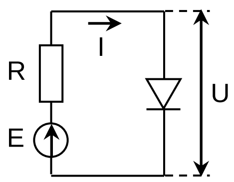
4b5.
K_f=100 uA/lm,
Φ=0.15 lm
R=400 kOhm,
I=10 mA,
U=220 V,
Ku=?, Kp=?
Photovoltaic cell current:
$I_f=K_f*\Phi=15$ uA
Amplifier's input power:
$\rho_m=I^2R=(15*10^{-6})^2*4*10^5=9*10^{-5}$ Vt
Power of relay:
$\rho_n=U*I=220*10*10^{-3}=2.2$ Vt

$$K_p=\frac{\rho_n}{\rho_\delta}=\frac{2.2}{9*10^{-5}}=2.44*10^4$$

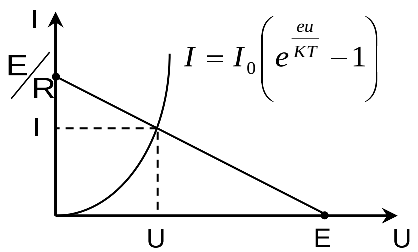
$$K_u=\frac{U_n}{U_R}=\frac{U_p}{I_f*R}=\frac{220}{10*10^{-6}*400*10^3}=36.7$$

4b6.
I_0=8 uA,
E=10 V
R=1 kOhm,
T=300 K,
I=?, U=?
1.

$$I=I_0\left(e^{\frac{u}{\varphi_T}}-1\right)=I_0\left(e^{\frac{E-IR}{(KT)/e}}-1\right)$$



2.



4b7.
I_{hmax}=2 mA,
U_{gcut}=5 V
U_{g1}=-5 V
U_{g2}=0 V
U_{g3}=-2.5 V
I_h=?, S=?

1. $$I_h=I_{hmax}\left(1-\frac{|U_g|}{U_{gcut}}\right)^2 \qquad I_{h1}=2\left(1-\frac{|-5|}{5}\right)^2=0$$

$$I_{h2} = 2\left(1-\frac{|0|}{5}\right)^2 = 2 \qquad I_{h3} = 2\left(1-\frac{|-2.5|}{5}\right)^2 = 0.5$$

2. $$S = \frac{2\cdot I_{hmax}}{U_{gcut}}\left(1-\frac{|U_g|}{U_{gcut}}\right)^2 \qquad S_1 = \frac{2\cdot 2}{5}\left(1-\frac{|-5|}{5}\right)^2 = 0$$

$$S_2 = \frac{2\cdot 2}{5}\left(1-\frac{|0|}{5}\right)^2 = 0.8 \qquad S_3 = \frac{2\cdot 2}{5}\left(1-\frac{|-2.5|}{5}\right)^2 = 0.2$$

4b8.

a. By the above mentioned values calculate the densities of majority carriers in *p-* and *n-* domains:

$$n_n = N_d = \frac{\sigma_n}{q\mu_n} = \frac{10}{1.6*10^{-19}*1300} = 4.8*10^{16}\ \text{cm}^{-3},\ P_p = N_a = \frac{\sigma_p}{q\mu_p} = \frac{5}{1.6*10^{-19}*500} = 6.2*10^{16}\ \text{cm}^{-3}$$

When the external voltage is missing, the contact φ_k difference of potentials can be calculated by the following:

$$\varphi_k = \frac{kT}{q}\ln\frac{n_n p_p}{n_i^2} = \frac{1.38*10^{-23}300}{1.6*10^{-19}}\ln\frac{4.8*10^{16}*6.2*10^{16}}{(1.4*10^{10})^2} = 0.78\ \text{V},$$

b. d_p and d_n widths of both common d and p & n domains will be defined in the following way:

$$d = \sqrt{\frac{2\varepsilon\varepsilon_0\varphi_k(N_d+N_a)}{qN_dN_a}} = \sqrt{\frac{2*12*8.86*10^{-14}*0.78*(4.8*10^{16}+6.2*10^{16})}{1.6*10^{-19}*4.8*10^{16}*6.2*10^{16}}} = 0.196\ \text{um}$$

$$\frac{d_n}{d_p} = \frac{N_a}{N_d} = \frac{p_p}{n_n}, \qquad d_p = d - d_n,$$

$$d_n = \frac{d*N_a}{N_d(1+N_a/N_d)} = \frac{0.0000196*6.2*10^{16}}{4.8*10^{16}*\left(1+\frac{6.2*10^{16}}{4.8*10^{16}}\right)} = 0.11\ \text{um}$$

$$d_p = d - d_n = 0.196 - 0.11 = 0.086\ \text{um}$$

c. The maximum E_m strength of an electrical field is defined by the following:

$$E_m = \frac{2*\varphi_k}{d} = \frac{2*0.78}{0.0000196} = 7.9*10^4\ \text{V/cm}$$

4b9.

a. j_S density of photodiode's saturation current by ideal p-n junction can be defined as follows:

First, from Einstein equation define diffusion coefficients of electrons and holes

$$D_n = \frac{kT}{q}\mu_n = 0.026*1300 = 33.8\ \text{cm}^2/\text{v},\ D_p = \frac{kT}{q}\mu_p = 0.026*500 = 13\ \text{cm}^2/\text{v},\ \text{where } kT/q = 0.026\text{V},$$

then the densities of minority carriers.

$$p_n = \frac{(n_i)^2}{N_d} = \frac{(1.4*10^{10})^2}{10^{15}} = 1.96*10^5\ \text{cm}^{-3},\ n_p = \frac{(n_i)^2}{N_a} = \frac{(1.4*10^{10})^2}{5*10^{15}} = 3.9*10^4\ \text{cm}^{-3}$$

And finally the current density:

$$j_S = q\left(\frac{D_pP_n}{L_p}+\frac{D_nn_p}{L_n}\right) = 1.6*10^{-19}\left(\frac{13*1.96*10^5}{0.006}+\frac{33.8*3.9*10^4}{0.01}\right) = 8.8*10^{-11}\ \text{A/cm}^2$$

b. In order to define open circuit voltage, first define the photo current by the above mentioned values:

$$I_f = q\alpha W\beta S\Phi = 1.6*10^{-19}*10^3*0.01*0.7*10^{-4}*10^{18} = 1.1*10^{-4}\ \text{A}$$

then open circuit voltage $V_{xx} = \frac{kT}{q}\ln\left(\frac{I_F}{I_S}+1\right) \approx \frac{kT}{q}\ln\left(\frac{I_F}{I_S}\right) = 0.026*\ln\left(\frac{1.1*10^{-4}}{8.8*10^{-11}}\right) = 0.3\ \text{V}$

4b10.

a. Define h_1/h_2 ratio of h_1 and h_2 widths of the channel near the source and drain. Near source reverse biasing voltage applied on p-n junction $V_{p-n} = V_G + V_1 = 1 + 0.5 = 1.5$ V, and near the drain $V_{p-n} = V_G + V_2 = 1 + 1 = 2$ V. Near source width of charge layer $d = \left(2\varepsilon\varepsilon_0\mu_n\rho\, V_{P-n}\right)^{1/2} =$ $= \left(2*12*8.85*10^{-14}*1300*0.5*1.5\right)^{1/2} = 0.45*10^{-4}$ cm, and near the drain

$$d_2 = \left(2\varepsilon\varepsilon_0\mu_n\rho V_{P-n}\right)^{1/2} = \left(2*12*8.85*10^{-14}*1300*0.5*2\right)^{1/2} = 0.52*10^{-4} \text{ cm}.$$

h_1 and h_2 widths of source and drain of the channel will be defined:

$$h_1 = \alpha - 2d_1 = 2*10^{-4} - 2*0.45*10^{-4} = 1.1*10^{-4} \text{ cm},$$

$$h_2 = \alpha - 2d_2 = 2*10^{-4} - 2*0.52*10^{-4} = 0.96*10^{-4} \text{ cm},$$

Thus h_1/h_2 ratio of h_1 and h_2 widths will be

$$h_1/h_2 = 1.1/0.96 = 1.15$$

b. cutoff voltage

$$V_{G0} = \frac{\alpha^2}{8\varepsilon\varepsilon_0\mu_n\rho} = \frac{4*10^{-8}}{8*12*8.85*10^{-14}*1300*0.5} = 7.24 \text{ V}$$

4b11.

a. Define C capacitance of the gate in depletion mode

$$S = \ell \cdot b = 10^{-2}*10^{-2} = 10^{-4} \text{ cm}^2 \qquad C = \frac{\varepsilon\varepsilon_0 S}{d} = \frac{12*8.85*10^{-14}*10^{-4}}{0.5*10^{-4}} = 2.12*10^{-12} \text{ F}$$

b. In order to define the cutoff voltage, first find the density of majority carriers in the channel $n = N_C\, exp\left[-\frac{E_C - E_F}{kT}\right] = 10^{19} * exp\left[-\frac{0.2}{0.025}\right] = 3.2*10^{15}$ cm^{-3}, then the cutoff voltage

$$V_{G0} = \frac{qn\alpha bl}{C} = \frac{1.6*10^{-19}*3.2*10^{15}*2*10^{-4}*10^{-2}*10^{-2}}{2.12*10^{-12}} = 4.8 \text{ V}$$

4b12.

Capacitance of the abrupt p-n- junction is given by

$$C = \sqrt{\frac{\varepsilon\varepsilon_0 N_A N_D e}{2(N_a + N_0)(V_r + \;_k)}}S,$$

where N_A and N_D are the donor and acceptor densities and S is cross section area of diode.
When V_r=2 V, C_1=200 pF

$$C_1 = S\sqrt{\frac{\varepsilon\varepsilon_0 N_A N_D e}{2(N_a + N_0)(V_{r1} + \;_k)}},$$

When reverse bias is V_r, then C_2 = 50 pF.

$$C_2 = S\sqrt{\frac{\varepsilon\varepsilon_0 N_A N_D e}{2(N_a + N_0)(V_{r2} + \;_k)}},$$

Therefore

$$\frac{C_1}{C_2} = \sqrt{\frac{V_{r2} + \;_k}{V_{r1} + \;_k}},$$

Hence

$$V_{r2} = \left(\frac{C_1}{C_2}\right)^2 (V_{r1} + \;_k) - \;_k = 44.1 \text{ V}.$$

4b13.

$$\sigma = e\mu_n N_D$$

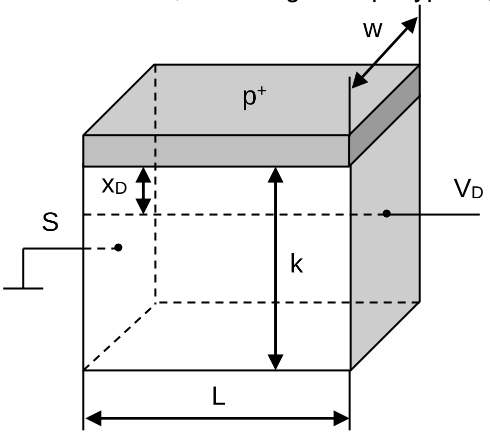
$$N_D = \frac{\sigma}{e\mu_n} = 10^{21}\mu^{-3}$$

The “pinch-off” voltage of the channel for the abrupt p-n junction is $U_{po} = \frac{\varepsilon N_D a^2}{2\varepsilon\varepsilon_0}$,

where $a = \frac{w}{2} = 4$ μ m, hence $U_{po} = 12$.

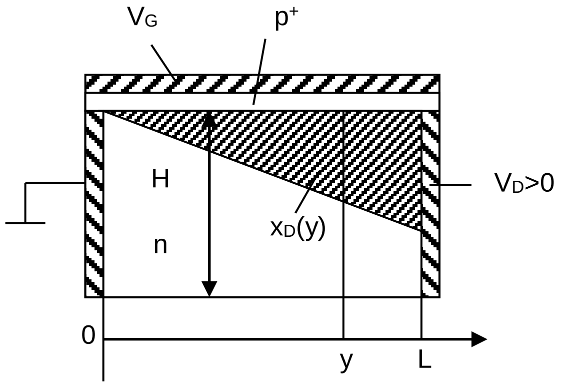
4b14.

For simplification, an asymmetric field effect transistor will be considered, the channel of which is an n-type semiconductor, and the gate is p^+-type region which forms the p^+-n junction with the channel.



k<<L<<w

a)



b)

The n-channel of the transistor has length L (a distance from source to drain), width “w” and depth “H” (a distance between the insulating substrate and metallurgical boundary of the gate).
When the source is grounded and V_D=0, the channel effective width (the width of its quasI-neutral part) is uniform in any cross section y=const and equals (H-x_D), where

$$x_D = \sqrt{\frac{2\varepsilon\varepsilon_0(V_{bi} - V_G)}{eN_D}}.$$

Here V_{bi} is the contact potential difference , V_G-gate voltage, N_D is the channel doping level, ε- dielectric , ε_0-electrical constant and e is an elementary charge.
Assume that p^+-region of the gate is strongly doped and therefore almost all space charge region can be considered as fully expanded in the n- channel region.
L>>H and the Schottky graduate channel approximation is valid. Also for the uniform doped channel the approximation of complete depletion layer is applicable. When V_D>0, the drain current in the y section is

$$I_D = eN_D w[H - x_D(y)]v(y),$$

where v(y)- is the electron drift velocity, which is defined by ε_y-component of electrical field in the section y:

$$v(y) = \frac{\mu_n\varepsilon_y}{1 + \frac{\varepsilon_y}{\varepsilon_c}},$$

and

$$x_D = \sqrt{\frac{2\varepsilon\varepsilon_0(V(y) + V_{bi} - V_G)}{eN_D}}$$

is depletion layer width in the same section.
As L>>H, then $\varepsilon_y = \frac{dV(y)}{dy}$, and

$$I_D = eN_D w\left[H - \sqrt{\frac{2\varepsilon\varepsilon_0(V(y) + V_{bi} - V_G)}{eV_D}}\right]\frac{\mu_n}{1 + \frac{1}{\varepsilon_c}\frac{dv}{dy}}\frac{dv}{dy}$$

or

$$I_D = \left\{ eN_D w \left[H - \sqrt{\frac{2\varepsilon\varepsilon_0 (V(y) + V_{bi} - V_G)}{eV_D}} \right] \mu_n - \frac{I_D}{\varepsilon_c} \right\} \frac{dv}{dy}$$

Integrating this equation y=0 (V(0)=0) up to y=L (V(L)=V_D), considering that I_D=Const, the following can be obtained:

$$I_D \cdot L = \int_0^{V_D} \left\{ eN_D w \left[H - \sqrt{\frac{2\varepsilon\varepsilon_0 (V(y) + V_{bi} - V_G)}{eV_D}} \right] \mu_n - \frac{I_D}{\varepsilon_c} \right\} dv =$$

,

$$= eN_D wH\mu_n V_D - eN_D w\mu_n \int_0^{V_D} \sqrt{\frac{2\varepsilon\varepsilon_0 (V(y) + V_{bi} - V_G)}{eV_D}} dv - \frac{I_D}{\varepsilon_c} V_D$$

Or

$$I_D \left(1 + \frac{V_D}{\varepsilon_c L} \right) = \frac{eN_D wH\mu_n V_D}{L} - \frac{eN_D w\mu_n}{L} \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_D}} \int_0^{V_D} \sqrt{V + V_{bi} - V_G}\, dv \ .$$

After some transformation the final expression for the drain current follows:

$$\frac{I_D}{I_p} = \frac{3\dfrac{V_D}{V_{bi} - V_T} - 2\left[\left(\dfrac{V_D + V_{bi} - V_G}{V_{bi} - V_T} \right)^{\frac{3}{2}} - \left(\dfrac{V_{bi} - V_G}{V_{bi} - V_T} \right)^{\frac{3}{2}} \right]}{1 + \dfrac{V_D}{\varepsilon_c L}},$$

where

$$I_p = \frac{3N_D wH\mu_n}{3L} (V_{bi} - V_T)$$

$$V_T = V_{bi} - \frac{eN_D H^2}{2\varepsilon\varepsilon_0} .$$

4b15.

For a “limited source” condition with the total amount of impurities Q , the solution of the Fick equation is given by the Gaussian function.

$$N(x,t) = \frac{Q}{\sqrt{\pi Dt}} \exp[-\left(\frac{x}{2\sqrt{Dt}} \right)^2]$$

$p-n$ junction is formed at that place, where boron concentration equals to the concentration of impurities in the bulk silicon substrate, that is: $\frac{Q}{\sqrt{\pi Dt}} \exp[-\left(\frac{x_j}{2\sqrt{Dt}} \right)^2] = N_D$

Solving this equation with respect to x_j , the following is obtained $x_j = 2\sqrt{Dt} \sqrt{\ln\left[\frac{Q}{N_D \sqrt{\pi Dt}} \right]}$

Substituting the numerical values of Q , D , N_D and t , into this expression yields $x_j = 2{,}7$ μ m.

4b16.

First find equilibrium heights of emitter and collector junctions:

$$\varphi_{0E} = \frac{kT}{e} ln \frac{N_{AE} \cdot N_{DB}}{n_i^2} = 0.856 \text{ eV},$$

$$\varphi_{0K} = \frac{kT}{e} ln \frac{N_{DB} \cdot N_{AK}}{n_i^2} = 0.635 \text{ eV}.$$

The width of emitter junction depletion region in the base of the transistor is

$$W_{nE} = \sqrt{\frac{2\varepsilon\varepsilon_0(e\varphi_{0E} - U_{EB})}{e^2 N_{DB}^2\left(\frac{1}{N_{AE}} + \frac{1}{N_{DB}}\right)}} = 0.215\ \mu\text{ m},$$

and correspondingly the width of collector junction depletion region in the base is

$$W_{nK} = \sqrt{\frac{2\varepsilon\varepsilon_0(e\varphi_{0K} - U_{BK})}{e^2 N_{DB}^2\left(\frac{1}{N_{AK}} + \frac{1}{N_{DB}}\right)}} = 0.258\ \mu\text{ m}.$$

Therefore the width of the neutral base will be the following:

$$W_B = W - W_{nE} - W_{nK} = 0.527\ \ \mu\text{ m}.$$

The concentration of minority carries (holes) at the emitter-base junction will equal the following:

$$p_n(0) = \frac{n_i^2}{N_{DB}} exp\left(\frac{eU_{EB}}{kT}\right) = 5.18\cdot 10^{12}\ cm^{-3}.$$

Finally, the total charge of minority carries accumulated in the base is

$$Q = \frac{eS\, p_n(0)W_B}{2} = 6.4\cdot 10^{-13}\ \ K.$$

4b17.
Bipolar diffusion coefficient is determined as

$$D = \frac{n+p}{\frac{n}{D_p} + \frac{p}{D_n}}.$$

For intrinsic semiconductor

$$D = \frac{2D_n D_p}{D_n + D_p}.$$

Using Einstein relations one obtains

$$D = \frac{k_B T}{e}\frac{2\mu_n\mu_p}{\mu_n + \mu_p} \approx 20{,}7\ \text{cm}^2\text{/s}.$$

4b18.
First a density of donors in the semiconductor can be defined:

$$N_D = \frac{1}{e\mu_n\rho} = 1.6\cdot 10^{15}\ \ cm^{-3}.$$

The built-in potential barrier for the electrons is equal to

$$_m = \Phi_{Au} - \Phi_{Ge},$$

Here the semiconductor work function can be represented as

$$\Phi_{Ge} = \chi_{Ge} + E_c - E_F = \chi_{Ge} + kT\, In\frac{N_c}{N_D} = \chi_{Ge} + kT\, In\frac{N_c}{n_i} + kT\, In\frac{n_i}{N_D} = \chi_{Ge} + \frac{E_g}{2} - {}_0$$

where it is meant, that

$$\frac{E_g}{2} = kT\, In\frac{N_c}{n_i},$$

and

$$_0 = kT\, In\frac{N_D}{n_i} = 0.11\ \text{eV}$$

Therefore, $\Phi_{Ge} = 4.22$ eV, and $\varphi_m = 0.78$ eV.

4b19.

a) $\gamma = \dfrac{I_{ep}}{I_{ep} + I_{en}} = \dfrac{3}{3 + 0.01} \approx 0.9967,$

b) $\alpha_T = \frac{I_{cp}}{I_{cp}} = \frac{2.99}{3} = 0.9967$,

c) $\alpha_0 = \gamma\alpha_T = 0.9934$

$I_e = I_{ep} + I_{en} = 3.01$ m²

$I_c = I_{cp} + I_{cn} = 2.99 + 0.001 = 2.991$ mA

$I_{cp0} = I_c - \alpha_0 I_e = 2.991 - 0.9934 \cdot 3.01 = 0.000866 = 0.87$ uA.

4b20.

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_S qN_a(2\psi_B)}}{C_{ox}}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{d} = \frac{3.9\cdot 8.85\cdot 10^{-14}F}{5\cdot 10^{-7}\,cm\cdot cm} = 6.9\cdot 10^{-7}\,F/cm^2$$

$$V_{FB} = \psi_S - \frac{Q_{ox}}{C_{ox}} \approx -0.98 - \frac{1.6\cdot 10^{-19}\cdot 5\cdot 10^{11}}{6.9\cdot 10^{-7}} \approx -1.1\text{ V}$$

$$V_T = -1.1 + 0.84 - \frac{\sqrt{2\cdot 11.9\cdot 8.85\cdot 10^{-14}\cdot 1.6\cdot 10^{-19}\cdot 10^{17}\cdot 0.84}}{6.9\cdot{}^*10^{-7}} \approx 0.02\text{ V}$$

The substrate accumulation charge (Boron) will lead to flat-band bias by $\frac{qN_{\mathrm{bor}}}{C_{ox}}$, and therefore

$$0.6 = -0.02 + \frac{\mathrm{qN_{bor}}}{\mathrm{C_{ox}}}$$

$$\mathrm{N_{bor}} = \frac{0.62\cdot 6.9\cdot 10^{-7}}{1.6\cdot 10^{-19}} \approx 2.67\cdot 10^{12}\text{ cm}^{-2}$$

4b21.

$$\sigma_1 = \sigma_o e^{-\frac{\Delta E}{2kT_1}} \qquad \Delta\sigma = \sigma_1 - \sigma_2 = \sigma_0\left(e^{-\frac{\Delta E}{2kT_2}} - e^{-\frac{\Delta E}{2kT_1}}\right)$$

$$\sigma_2 = \sigma_o e^{-\frac{\Delta E}{2kT_2}} \qquad \frac{\Delta\sigma}{\sigma_1} = \frac{e^{-\frac{\Delta E}{2kT_2}} - e^{-\frac{\Delta E}{2kT_1}}}{e^{-\frac{\Delta E}{2kT_1}}} = e^{-\frac{\Delta E}{2k}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)} - 1 \approx 1.18 - 1 \approx 0.18$$

Answer: will increase by 18%.

4b22.

$$\sigma = en\mu_n + ep\mu_p \qquad p = \frac{n_i^2}{n}$$

$$\sigma = en\mu_n + e\frac{n_i^2}{n}\mu_p$$

Find the minimum value from $\frac{d\sigma}{dn} = 0$ condition:

$$\frac{d\sigma}{dn} = \cancel{e}\mu_n - \cancel{e}\frac{n_i^2}{n^2}\mu_p = 0$$

$$\mu_n = \frac{n_i^2}{n^2}\mu_p \Rightarrow n = n_i\sqrt{\frac{\mu_p}{\mu_n}}$$

$$p = \frac{n_i^2}{n} = \frac{n_i^{\cancel{2}}}{\cancel{n_i}\sqrt{\frac{\mu_p}{\mu_n}}} = n_i\sqrt{\frac{\mu_n}{\mu_p}}$$

4b23.

$$\mu = \frac{e\tau}{m};\ \ L_d = \sqrt{D\tau};\ \ D = \frac{kT}{e}\mu$$

$$L_d = \sqrt{\frac{kT}{e}\mu\tau} = \sqrt{\frac{kT\tau^2}{m}} = \tau\sqrt{\frac{kT}{m}}$$

$$L_D - \frac{L_D}{10} = \sqrt{\frac{kT}{e}\mu\left(1+\frac{1}{20}\right)\cdot\tau\left(1+\frac{x}{100}\right)} = \sqrt{\frac{kT\tau^2}{m}\left(1+\frac{1}{20}\right)\cdot\left(1+\frac{x}{100}\right)}$$

$$L_D\left(1+\frac{1}{10}\right) = \tau\sqrt{\frac{kT}{m}\left(1+\frac{1}{20}\right)\cdot\left(1+\frac{x}{100}\right)} = \sqrt{\frac{21}{20}\cdot\frac{100+x}{100}}$$

Answer: will increase by 15%.

4b24.

a. Using Bohr model, the ionization energy of donors in any semiconductor is expressed by:

$$E_d = \left(\frac{\varepsilon_o}{\varepsilon_s}\right)^2\cdot\left(\frac{m^*}{m_o}\right)\cdot E_H$$

$$E_d = \frac{1}{(17)^2}\cdot 0.014\cdot 13.6 \approx 6.58\cdot 10^{-4}\ \text{eV}$$

b. The radius of the first orbit (n=1) is connected to the corresponding radius of hydrogen atom

$$r = \left(\frac{\varepsilon\cdot m_o}{m^*}\right) r_H$$

$$r_{I_nS_b} = \left(\frac{17}{0.014}\right)\cdot 0.53 = 643.6\,\overset{o}{A}$$

c. Density of conducting electrons

$$n \approx \frac{N_d}{1+g\exp\left(-\frac{E_d}{kT}\right)} \approx \frac{N_d}{1+2\exp\left(-\frac{E_d}{kT}\right)}$$

$$kT = 0.00034$$

$$n = \frac{1\cdot 10^{14}}{1+2\exp(-2)} = 0.78x10^{14}$$

4b25.

Field tension in space for metal $E = \frac{V_k}{d} = 10^7$ V/cm.

Surface density of charge

$Q_s = E_K\cdot\varepsilon_o,\ Q_s = 10^7\cdot 8.85\cdot 10^{-14} = 8.85\cdot 10^7$ K/cm²

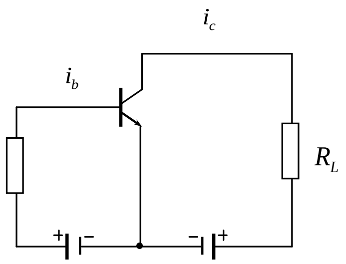
Number of electrons $n = \frac{Q_s}{q} = \frac{8.85\cdot 10^{-7}}{1.6\cdot 10^{-19}K}\cdot\frac{K}{cm^2} \approx 5.5\cdot 10^{12} cm^{-2}$

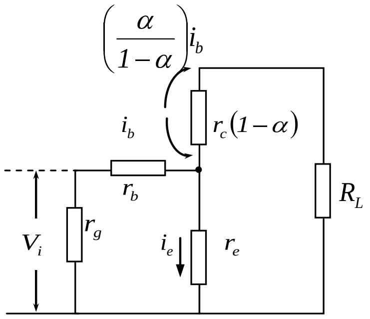
in order to provide the difference of the same potentials (for metal–n type semiconductor contact) it will be necessary to deplete $W = \frac{n}{n_{ss}} = \frac{5\cdot 10^{12}}{10^{15}} = 5\cdot 10^{-3}$ cm width layer from semiconductor.

4b26.

According to AC, the input voltage

$$V_i = i_e r_e + i_b r_b$$
$$\alpha = i_c / i_e \,,$$
$$i_b = (1-\alpha) i_e$$





Input power

$$P_i = V_i \cdot i_b = \left[i_e r_e + (1-\alpha)\cdot i_e r_b\right](1-\alpha) i_e$$

Output power

$$P_{out} = i_c^2 R_L = i_e^2 \alpha R_L$$

Amplification coefficient according to power

$$G_p = \frac{\alpha^2 R_L}{\left[r_c + (1-\alpha) r_b\right](1-\alpha)}$$

$\alpha = 0.98,\ r_e = 20$ Ohm, $r_b = 500$ Ohm, $R_L \approx 30$ kOhm

$$G_p = \frac{0.98^2 \cdot 3 \cdot 10^4}{(20 + 0.02 \cdot 500)(0.02)} = 5 \cdot 10^4$$

4b27.
As it is known

$$n \sim T^{3/2} \exp(-E_g / 2k_B T)$$

Therefore

$$\frac{n_1}{n_2} = \left(\frac{T_1}{T_2}\right)^{3/2} \exp\left[-\frac{E_g(0)}{2k_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$, where $E_g = E_g(0) - \alpha T$.

Therefore

$$E_g(0) = 2k_B \frac{T_1 T_2}{T_1 - T_2} \ln\left(n_1 T_2^{3/2} / n_2 T_1^{3/2}\right) = 0.26 \text{ eV.}$$

4b28.

In the given case continuity equation has the following form: $D_p \frac{d^2\Delta p}{dx^2} - E\mu_p \frac{d\Delta p}{dx} - \frac{\Delta p}{\tau_p} = 0$, $x \neq 0$, or

$$\frac{d^2\Delta p}{dx^2} - \frac{eE}{k_B T}\frac{d\Delta p}{dx} - \frac{\Delta p}{L_p^2} = 0:$$

It is obvious that $\Delta p \to 0$, when $x \to \pm\infty$. Therefore

$$\Delta p = \begin{cases} \Delta p(x=0)\exp(k_1 x), & x < 0 \\ \Delta p(x=0)\exp(k_2 x), & x > 0 \end{cases}$$

where $k_{1,2} = eE/2k_B T \pm \left(e^2 E^2 / 4k_B^2 T^2 + L_p^{-2}\right)^{1/2}$. It is obvious that $k_1 > 0$ and $k_2 < 0$.

4b29.

From the determination of the injection coefficient it follows that $j_p(0) = \xi\left[j_p(0) + j_n(0)\right]$. Therefore $j_n(0) = j_p(0)(1-\xi)/\xi$. Hole current density at $x = 0$ equals $j_p(0) = -eD_p \frac{d\Delta p}{dx}\big|_{x=0}$. Taking into account that in the considered case $\Delta p = \Delta p(x=0)\exp(-x/L_p)$, one obtains $j_p(0) = eD_p\Delta p(0)/L_p$, therefore $j_n(0) = eD_p\Delta p(0)(1-\xi)/\xi L_p = 1.68$ mA.cm^{-2}.

4b30.

Sample resistivity $\rho = RS/l = 0.03$ Ohm. On the other hand, $\rho = 1/(en\mu_n + ep\mu_p) = 1/(e\frac{n_i^2}{p}\mu_n + ep\mu_p)$. Hence

$$p = \frac{1+\sqrt{1-4e^2\rho^2\mu_n\mu_p n_i^2}}{2e\rho\mu_n} = 4\times10^{21}\ \text{m}^{-3}.$$

4b31.

a. The density of radiation, coming to surface is F, and in d depth, after absorption, is Fe$^{-\alpha d}$. Therefore, the number of quantum, absorbed in d depth, is F(1-e$^{-\alpha d}$), and the photocurrent, occurred in the result of absorption, is I_{Ph}=qSF(1-e$^{-\alpha d}$).

b. Find the photocurrent, occurred in the result of absorption of λ_1 wave radiation.

$$I_{Ph1} = qSF\,(1-e^{-\alpha 1d}) \approx 10^{-9}\text{A}$$

c. Find the photocurrent, occurred in the result of absorption of λ_2 wave radiation.

$$I_{Ph1} = qSF\,(1-e^{-\alpha 1d})\,) \approx 0.15*10^{-9}\text{A}$$

d. Find the ratio of photocurrents.

$$\frac{I_{Ph1}}{I_{Ph2}} \approx 6.7$$

4b32.

In general, the performance of photodiode is characterized by three processes 1. τ_{RC} time constant, 2. τ_d diffusion time of non-equilibrium charges through the base and 3. τ time of non-equilibrium charges through bulk charge domain.

Time constant of photodiode is defined by base resistance and charge capacitance of p-n junction. $\tau_{RC} = RC$:

Base resistance and charge capacitance of p-n junction are defined by the following expressions:

$$R = \frac{w}{Sqn\mu_n} \approx 0{,}3\ \text{Ohm}, \quad C = \frac{S\varepsilon\varepsilon_0}{d} \approx 10^{-10}\text{F}.$$

Therefore, $\tau_{RC} = RC \approx 3\cdot10^{-11}$s.

Diffusion time of non-equilibrium charges through the base can be defined by the following expression: τ_d=w^2/2D=2,9$\cdot$10^{-7}s.

The drift time of non-equilibrium charges through bulk charge domain can be defined by the following expression:

$$\tau = \frac{d}{V_{\max}} = 2\cdot10^{-11}\text{s}.$$

Therefore, photodiode performance, which is defined by the largest time constant, in the given case diffusion time of non-equilibrium charges through the base, will equal 2,9$\cdot$10^{-7}s.

4b33.

In order to define the power density equivalent to the noise of photodiode, its basic noise must be taken into account, which has fluctuation nature and is defined by average square value of current fluctuation by the following expression:

$$\bar{I}_{dr}^2 = 2qI\Delta f,$$

as well as photosensitivity, according to power, by the following expression:

$$S_i(\lambda) = \frac{I_{L\Phi}}{P}:$$

Consider that minimum signal, detected against the background of noise is defined by the value of signal noise ratio, equal to one.

$$\frac{I}{\sqrt{\bar{I}_{dr}^2}} \equiv \frac{S_i(\lambda)P}{\sqrt{\bar{I}_{dr}^2}} = 1;$$

Threshold sensitivity can be defined, i.e. the minimum power of radiation which will be detected against the background of the noise.

$$P = \frac{\sqrt{\bar{I}_{dr}^2}}{S_i(\lambda)}$$

$\bar{I}^2$ is proportional to Δf range of bandwidth, hence, the power density, equivalent to noise in the unit layer of frequency will be.

$$P = \frac{1}{S_i(\lambda)}\sqrt{\frac{\bar{I}_{dr}^2}{S\Delta f}} = 8\cdot 10^{-12}\ \text{Vt}\cdot\text{Hz}^{-1/2}\cdot\text{cm}^{-1}$$

4b34.

Near the source, d width of p-n junction will be defined by the following expression:

$$d_1 = \left(\frac{2\varepsilon\varepsilon_0}{q}\cdot\frac{}{N_d}\right)^{1/2} = 0{,}36\cdot 10^{-4}\text{cm}.$$

and near the drain:

$$d_2 = \left(\frac{2\varepsilon\varepsilon_0}{q}\cdot\frac{\varphi + V}{N_d}\right)^{1/2} = 1{,}79\cdot 10^{-4}\ \text{cm}.$$

therefore narrowing size of channel near the source will equal d_1-d_2=1,43·10^{-5}cm.

4b35.

The saturation voltage of the transistor $V_{DS\ sat.} = V_{GS} - V_t$= 3-1= 2V.

$V_{DS} > V_{DS\ sat}$ therefore the transistor operates in saturation mode. In this mode the drain current of the transistor will equal I_D = 0,5 μ_n Cox (W/L) (V_{GS}- V_t)^2. Calculate Cox = ($\varepsilon_0\ \varepsilon_{si\ o2}$)/ t_{ox} =(3,9x8,85x10^{-14})/10x10^{-7}= 3,45x10^{-7} F/cm^2.

I_D = 0,5x300x3,45x10^{-7}(3-1)^{2}x (10/1)=2,07 uA.

Transconductance g_m=d I_D/d V_{GS}

g_m= μ_n Cox (W/L) (V_{GS}- V_t) =300x3,45x10^{-7}x10x2= 2 uA

Answer: 2,07 uA and 2 uA.

4b36.

$$\varphi_s^{(1)} = 0$$

$$\varphi_s^{(2)} = \varphi_o$$

$$\varphi_s^{(3)} = 2\varphi_o$$

$$Q_{sc}, C_{sc} = ?$$

1. If $\varphi_s = 0$, Q_{sc} charge is missing, and C_{sc} equals C_{FB} of flat regions.

   $Q_{sc} = 0;$

   $$C_{si} = C_{FB} = \sqrt{\frac{\varepsilon_s\varepsilon_o\cdot q\cdot N_{ш}}{kT/q}}$$

   Calculate the necessary characteristics.

   $$N_a = \frac{1}{q\cdot\mu_p\cdot\rho} = \frac{1}{1.6\cdot 10^{-19}\cdot 600\cdot 10} = 1\cdot 10^{15}\text{cm}^{-3}$$

   $$_O = \frac{kT}{q} ln\frac{N_d}{n_i} = 0.0259\cdot ln\frac{1\cdot 10^{15}}{1.6\cdot 10^{10}} = 0.29\ \text{V}.$$

   $$C_{FB} = \sqrt{\frac{11.8\cdot 8.85\cdot 10^{-14}\cdot 1.6\cdot 10^{-19}\cdot 1\cdot 10^{15}}{0.0259}} = 8\cdot 10^{-8}\ \text{F}/\text{cm}^2.$$

2. If $\varphi_s = \varphi_o$ the semiconductor will be intrinsic which is the boundary value from depletion region to transition into low inversion:

$$Q_{sc} = Q_B = \sqrt{2 \cdot \phi_s \varepsilon_o \cdot q \cdot N_{\text{a}} \left(\varphi_o - {kT}/{q} \right)} =$$

$$= \sqrt{2 \cdot 11.8 \cdot 8.85 \cdot 10^{-14} \cdot 1.6 \cdot 10^{-19} \cdot 1 \cdot 10^{15} \cdot 0.26} = 9.3 \cdot 10^{-9}\ \text{S}/\text{cm}^2$$

$$C_{sc} = C_B = \sqrt{\frac{\varepsilon_s \varepsilon_o \cdot q \cdot N_{\text{a}}}{2 \cdot \left(\varphi_o - {kT}/{q} \right)}} =$$

$$= \sqrt{\frac{11.8 \cdot 8.85 \cdot 10^{-14} \cdot 1.6 \cdot 10^{-19} \cdot 1 \cdot 10^{15}}{2 \cdot (0.29 - 0.03)}} = 5.7 \cdot 10^{-8}\ \text{F}/\text{cm}^2$$

3. If $\varphi_s = 2\varphi_o$, which corresponds to transition from low inversion into high inversion, then

$$Q_{sc} = 2 \cdot \varepsilon_s \varepsilon_o \cdot q \cdot N_{\text{a}} \cdot 2\varphi_o =$$

$$= \sqrt{2 \cdot 11.8 \cdot 8.85 \cdot 10^{-14} \cdot 1.6 \cdot 10^{-19} \cdot 1 \cdot 10^{15} \cdot 0.58} = 1.4 \cdot 10^{-8}\ \text{S}/\text{cm}^2$$

$$C_{sc} = \sqrt{\varepsilon_s \varepsilon_o \cdot q \cdot {N_{\text{a}}}/{2\varphi_o}} =$$

$$= \sqrt{\frac{11.8 \cdot 8.85 \cdot 10^{-14} \cdot 1.6 \cdot 10^{-19} \cdot 1 \cdot 10^{15}}{0.58}} = 1.7 \cdot 10^{-8}\ \text{F}/\text{cm}^2$$

4b37.

pSi

$N_{\text{a}} = 10^{18}\,\text{cm}^{-3}$,

$T = 300\text{S}$

$N_{\text{ss}} = 2 \cdot 10^{12}\,\text{cm}^{-2} \cdot \text{eV}^{-1}$

$\varphi_s^{(1)} = 0$

$\varphi_s^{(2)} = \varphi_o$

$\varphi_s^{(3)} = 2\varphi_o$

$Q_{ss} = ?\ \ Q_{sc} = ?$

The charge of surface states:

$Q_{ss} = -qN_{ss}(\varphi_s - \varphi_o)$, and Q_{sc} charge is conditioned by ionized acceptors:

$Q_{sc} = -\sqrt{2q\xi_s\xi_o N_{\text{a}}\varphi_s}$

$$\varphi_o = \frac{kT}{q}\ln\frac{N_{\text{a}}}{n_i} = 0.0259 \cdot \ln\frac{10^{18}}{1.6 \cdot 10^{10}} = 0.46\ \text{V}$$

$$Q_{ss}^{(1)} = qN_{ss}\varphi_o = 1.6 \cdot 10^{-19} \cdot 10^{12} \cdot 0.46 = 1.5 \cdot 10^{-7}\ \text{S}/\text{cm}^2$$

$$Q_{ss}^{(2)} = 0$$

$$Q_{ss}^{(3)} = -qN_{ss}\varphi_o = -1.6 \cdot 10^{-19} \cdot 2 \cdot 10^{12} \cdot 0.46 = -1.5 \cdot 10^{-7}\ \text{S}/\text{cm}^2$$

$$Q_{sc}^{(2)} = 0$$

$$Q_{sc}^{(2)} = -\sqrt{2q\xi_s\xi_o N_{\text{ш}}\varphi_s} = -2 \cdot 1.6 \cdot 10^{-19} \cdot 8.85 \cdot 10^{-14} \cdot 11.8 \cdot 10^{18} \cdot 0.46 = -3.9 \cdot 10^{-7}\ \text{S}/\text{cm}^2$$

$$Q_{sc}^{(3)} = -\sqrt{2q\xi_s\xi_o N_{\text{ш}} 2\varphi_o} = \sqrt{-2 \cdot 1.6 \cdot 10^{-19} \cdot 8.85 \cdot 10^{-14} \cdot 11.8 \cdot 10^{18} \cdot 0.92} = -5.5 \cdot 10^{-7}\ \text{S}/\text{cm}^2$$

4b38.

$$n = \frac{N_1}{2e^{\frac{E_1 - F}{kT}} + 1}$$, when $F = E_1 \Rightarrow n = \frac{N_d}{3}$.

4b39.

$$\Delta n(t) = \Delta n(0) \cdot e^{-t/\tau_n}; \quad \left|\Delta n(0) = 2.5 \cdot 10^{-20} m^{-3}\right.$$

$$\left.\frac{d(\Delta n(t))}{dt}\right|_{t=o} = -\frac{\Delta n(0)}{\tau_n} = 2.8 \cdot 10^{24}$$

$$a)\tau_n = \left|\frac{\Delta n(0)}{2.8 \cdot 10^{24}}\right| = 89 um/\sec$$

$$b)\Delta n(2um) = 2.5 \cdot 10^{-20} \cdot e^{-\frac{2 \cdot 10^{-3}}{89 \cdot 10^{-6}}} \approx 4.4 \cdot 10^{10} m^{-3}$$

4b40.

$$R = 0$$

$$R = \frac{1}{e} \cdot \frac{p\mu_p^2 - n\mu_n^2}{(p\mu_p + n\mu_n)^2} = 0 \Rightarrow n\mu_n^2 = p\mu_p^2 \Rightarrow \frac{n}{p} = \frac{\mu_p^2}{\mu_n^2}$$

$$\frac{\sigma_p}{\sigma} = \frac{ep\mu_p}{en\mu_n + ep\mu_p} = \frac{1}{\frac{n\mu_n}{p\mu_p} + 1} = \frac{1}{\frac{\mu_p^2 \mu_n}{\mu_n^2 \mu_p}} = \frac{1}{\frac{\mu_p}{\mu_n} + 1} \approx 0.7; \quad \frac{\sigma_p}{\sigma} \approx 70\%$$

4b41.

$$\mu = \frac{e\tau}{m}; \; L = \sqrt{D\tau}; \; D = \frac{kT}{e}\mu; \; L = \sqrt{\frac{kT}{e}\mu\tau} \Rightarrow L\sqrt{\frac{kT}{m}\tau^2} = \tau\sqrt{\frac{kT}{m}}$$

$$L + \frac{L}{10} = \sqrt{\frac{kT}{e}\left(\mu + \frac{\mu}{20}\right) \cdot \left(\tau + \frac{\tau \cdot x}{100}\right)}$$

$$L\left(1 + \frac{1}{10}\right) = \sqrt{\frac{kT}{e}\mu\tau\left(1 + \frac{1}{20}\right) \cdot 1\left(\tau + \frac{x}{100}\right)}$$

$$1 + \frac{1}{10} = \sqrt{\frac{21}{20} \cdot \frac{100 + x}{100}} \Rightarrow x = 15\%$$

4b42. If there are scattering centers of N_d concentration with the S cross section, the average path will be

$$l = \frac{1}{N_\eta S}, \quad l = \frac{1}{N_\eta \pi r^2} \approx 0.64 \text{ um}$$

$$\tau = \frac{l}{\bar{v}}; \quad \frac{m^* \bar{v}^2}{z} = \frac{3}{2}kT; \quad \bar{v} = \left(\frac{3kT}{m^*}\right)^{1/2}$$

$$\tau = l\left(\frac{m^*}{3kT}\right)^{1/2} \approx 0.69 \cdot 10^{-11} \sec$$

$$\mu = \frac{e\tau}{m^*} \approx 0.77 \, \mathrm{m}^2/\mathrm{V} \cdot \sec$$

4b43.

Using the orbital moving equation of the electron bounded on the donor state $\frac{mv^2}{r} = \frac{e}{4\pi\varepsilon\varepsilon_0}$, the relation between the electron wavelength and momentum $\lambda = \frac{2\pi\hbar}{mv}$, as well as quantization condition $n\lambda = 2\pi r$ for the radius of electron orbit $r=\frac{4\pi\hbar^2\varepsilon\varepsilon_0}{me^2}n^2$ is obtained, where n is the main quantum number. From the obvious condition of impurity band originates $N_d^{-1/3}=2r(n=1)$, for the minimal concentration of donor impurity $N_d=\left(me^2/8\pi\hbar^2\varepsilon\varepsilon_0\right)^3=7.5\times10^{14}\ \mathrm{cm}^{-3}$ is obtained.

4b44.

Condition of band-to-band impact ionization is $mv^2/2\geq E_g$. Electron velocity determined as $v=\mu E+v_T$, where v_T is the thermal electron velocity. Therefore $E=\frac{1}{\mu}\left(\sqrt{2E_g/m}-\sqrt{3k_BT/m}\right)$: For silicon $E_g>>k_BT3/2$, therefore $E=\frac{\sqrt{2E_g/m}}{\mu}\cong7.4\times10^4$ V/cm.

4b45.

As well known $n_i=\left(N_cN_v\right)^{1/2}e^{-E_g/2k_BT}$, where $N_{c,v}=2\left(m_{n,p}k_BT/2\pi\hbar^2\right)^{3/2}$, $E_g(T)=E_g(0)-\alpha T$, α is the coefficient of temperature expansion of semiconductor forbidden gap. Therefore from the equations follows that

$$n_i^2(T_1)=N_c(T_1)N_v(T_1)e^{-\frac{E_g(0)-\alpha T_1}{k_BT_1}}\quad\text{and}\quad n_i^2(T_2)=N_c(T_2)N_v(T_2)e^{-\frac{E_g(0)-\alpha T_2}{k_BT_2}}$$

$$\alpha=\frac{k_BT_1}{T_1-T_2}\ln\frac{n_i^2(T_1)}{N_c(T_1)N_v(T_1)}-\frac{k_BT_2}{T_1-T_2}\ln\frac{n_i^2(T_2)}{N_c(T_2)N_v(T_2)}=5\times10^{-3}\ \text{eV/K}.$$

4b46.

The condition of the electron reflection from the atomic planes is determined by Wolf-Breg formula $2d\sin\theta=n\lambda$. The distance between atomic planes is defined as $d=a/(h^2+k^2+l^2)^{1/2}=a/(1^2+0^2+0^2)^{1/2}=a$. Using the relation between electron energy and wave-length $\varepsilon=p^2/2m=h^2/2m\lambda^2$ one obtains $\varepsilon=h^2n^2/2m(2d\sin\theta)^2$. Therefore, in the case $n=1$ for the electron energy one obtains $\varepsilon\cong4.8$ eV.

4b47.

1. First find the densities of minority carriers:

$$p_n=\frac{(n_i)^2}{N_d}=\frac{\left(1.4*10^{10}\right)^2}{10^{15}}=1.96*10^5\ \text{cm}^{-3},\quad n_p=\frac{(n_i)^2}{N_a}=\frac{\left(1.4*10^{10}\right)^2}{5*10^{15}}=3.9*10^4\ \text{cm}^{-3},$$

2. Then, from Einstein relation, the coefficients of electron and hole diffusion:

$$D_n=\frac{kT}{q}\mu_n=0.026*1300=33.8\ \text{cm}^2/\text{s},\quad D_p=\frac{kT}{q}\mu_p=0.026*500=13\ \text{cm}^2/\text{s},$$

3. The density of saturation current will be:

$$j_S=q\left(\frac{D_pP_n}{L_p}+\frac{D_nn_p}{L_n}\right)=1.6*10^{-19}\left(\frac{13*1.96*10^5}{0.006}+\frac{33.8*3.9*10^4}{0.01}\right)=8.8*10^{-11}\ \text{A}/\text{cm}^2$$

4. And the photocurrent

$$I_F=SqF_0,$$

therefore

$$\frac{I_F}{I_s}=\frac{SqF_0}{Sj_s}=\frac{qF_0}{j_s}=\frac{1.6*10^{-19}*10^{18}}{8.8*10^{-11}}\approx2*10^{10}\ \text{A}.$$

5. Thus, for idle state voltage, there is:

$$V_{xx}=\left(\frac{kT}{q}\right)\ln\left(\frac{I_F}{I_s}+1\right)=0.026*\ln\left(2*10^{10}\right)=0.62\ \text{V}.$$

4b48.

1. First find the densities of majority carriers in n and p domains:

$$n_n = N_C \exp\left[-\frac{E_C - E_F}{kT}\right] = 2.8*10^{19}*\exp\left[-\frac{0.2}{0.026}\right] = 1.28*10^{16}\ \text{cm}^{-3},$$

$$p_p = N_V \exp\left[-\frac{E_F - E_V}{kT}\right] = 1.02*10^{19}*\exp\left[-\frac{0.1}{0.026}\right] = 2.17*10^{17}\ \text{cm}^{-3}:$$

2. Then n – p junction's contact potential difference:

$$\varphi_k = \frac{kT}{q}\ln\frac{p_p * n_n}{n_i^2} = 0.026*\ln\frac{1.28*10^{16}*2.17*10^{17}}{2.56*10^{20}} \approx 0.78\ \text{eV}.$$

4b49.

As in the proposed structure the junctions are connected to each other sequentially, are symmetric, therefore they have the same width, the general charge capacitance of the structure will be:

$$C = \frac{C_1 C_2}{C_1 + C_2},$$

where $C_1 = C_2 = \frac{\varepsilon\varepsilon_0 S}{d/2}$. Using $C_{1,2}$ expression, $C = \frac{\varepsilon\varepsilon_0 S}{d} \approx 10^{-12}$ F is obtained.

4b50.

p-n junction barier capacitance is given by $C = \left[\frac{\varepsilon\varepsilon_0 q N_a N_d}{2(N_a + N_d)}\right]^{1/2} * (V + \varphi)^{-1/2} = K * (V + \varphi)^{-1/2}$,

Hence the change of capacitance in the result of lowering V voltage twice will be given by $\frac{C_1}{C_2} = \frac{(2 + 0.6)^{-1/2}}{(1 + 0.6)^{-1/2}} = 0.784$, or $C_2 = C_1 * 0{,}784 = 78{,}4$ *pF*

Answer: 78.4 *pF*.

4b51.

For calculation of Miller indices it is necessary:

a. To find intercepts of the given plane with the three basis axes x, y, z of cubic crystal;

b. To take the reciprocals of these numbers;

c. To reduce them to the smallest three integers having the same ratio.

For the given plane, there is:

a. Intercepts are equal to: $S_x = 2$; $S_y = 1/2$; $S_z = 1$.

b. Reciprocals values are equal to: 1/2; 2; 1

c. Smallest three integers are equal to: 1; 4; 2.

So, Miller indices of the given plane are as follows (142).

4b52.

Determine the resistivity.

$$\rho = RS/l = 150 \cdot 1 \cdot 10^{-3} \cdot 2 \cdot 10^{-3} / (10 \cdot 10^{-3}) = 0{,}03\ \ \Omega\text{.m}.$$

Resistivity of the n-type silicon sample is given by

$$\rho = \left[q(n\mu_n + p\mu_p)\right]^{-1}:$$

Substituting the corresponding values of the quantities from the problem condition the following is obtained

$$0{,}03 = \left[1{,}6 \cdot 10^{-19}(0{,}12 \cdot n + p \cdot 0{,}05)\right]^{-1},$$

or

$$0{,}12/n + 0{,}05p = 2{,}08 \cdot 10^{20}:$$

As $np = n_i^2$, then

$$p = \frac{n_i^2}{n} = \frac{(1{,}5 \cdot 10^{16})^2}{n}:$$

The following is obtained:

$$0{,}12n + 0{,}05(1{,}5 \cdot 10^{16})^2 / n = 2{,}08 \cdot 10^{20},$$

or

$$0{,}12n^2 + 0{,}05(1{,}5 \cdot 10^{16})^2 - 2{,}08 \cdot 10^{20} n = 0:$$

Hence for majority carriers:

$$n = \frac{2{,}08\cdot 10^{20} + \sqrt{\left(2{,}08\cdot 10^{20}\right)^2 - 4\cdot 0{,}12\cdot 0{,}05\cdot \left(1{,}5\cdot 10^{16}\right)^2}}{2\cdot 0{,}12} = 1{,}73\cdot 10^{21}\,\text{m}^{-3}:$$

As all the mixed atoms are ionized, N_d=n=1,73· 10^{21}m^{-3}.

4b53.

For the resistivity of semiconductor:

$$\sigma = q(n\mu_n + p\mu_p) \text{ and } np = n_i^2$$

Thus

$$\frac{\sigma}{q} = n\mu_n + \frac{n_i^2\mu_p}{n}.$$

This expression has the minimum, when

$$\frac{d(\sigma/q)}{dn} = 0,$$

or when $\mu_n - n_i^2\mu_p/n^2 = 0$ or $n = n_i\sqrt{\mu_p/\mu_n}$.

Since $\frac{d^2(\sigma/q)}{dn^2}$ the value of this expression is positive, then in this point $n = n_i\sqrt{\mu_n/\mu_p}$ resistivity has the minimum value.

4b54.

For the p-type silicon $\sigma_p = q\rho_p\mu_p$. From this expression for the hole densities in the p-region, the following is obtained:

$$p_p = \sigma_p/(q\mu_p) = 10^4/(0{,}19\cdot 1{,}6\cdot 10^{-19}) = 3{,}29\cdot 10^{23}\ \text{m}^{-3}:$$

Similarly for the n-type silicon:

$$n_n = \sigma_n/(q\mu_n) = 100/(0{,}39\cdot 1{,}6\cdot 10^{-19}) = 1{,}6\cdot 10^{21}\,\text{m}^{-3}$$

For the hole densities in the n-region:

$$p_n = n_i^2/n_n = (2{,}5\cdot 10^{19})^2/(1{,}60\cdot 10^{21}) = 3{,}91\cdot 10^{17}\,\text{m}^{-3}$$

Therefore the built-in potential is equal to:

$$\varphi_k = \frac{kT}{q}\ln\left(\frac{p_p}{p_n}\right) = \frac{1{,}38\cdot 10^{-20}\cdot 300}{1{,}6\cdot 10^{-19}}\ln\left(\frac{3{,}29\cdot 10^{23}}{3{,}91\cdot 10^{17}}\right) = 0{,}35\ \text{V}.$$

4b55.

Let us find the diode DC current for the DC voltage (V=0,1V) by the following formula

$$I = I_0\exp(\frac{qV}{kT} - 1) = 25\cdot 10^{-6}(\exp(1{,}6\cdot 10^{-19}\cdot 0{,}1/1{,}38\cdot 10^{-23}\cdot 300) - 1) = 1{,}17\ \text{mA}:$$

In this case DC resistance of diode is equal to

$$R_0 = V/I = 0{,}1/(1{,}17\cdot 10^{-3}) = 85\ \Omega.$$

4b56.

For wet oxidation at 950^{0}C $d_0^2 + Ad_0 = Bt$

Rearranging the equation $d_0 = \frac{Bt}{d_0} - A$

Thus, a plot of *do* versus *t/do* will give B as the slope and A as the intercept.

do (μm)	0.041	0.100	0.128	0.153	0.177
t/do (h/μm)	2.683	3.000	3.125	3.268	3.390

From the plot, the intercept of the line yields A = 0.50 μm.
The slope of the line yields B = 0.2 μm^{2}h.

4b57.
For a “limited source” condition with the total amount of impurities Q , the solution of Fick equation is given by the Gaussian function.

$$N(x,t)=\frac{Q}{\sqrt{\pi Dt}}\exp[-\left(\frac{x}{2\sqrt{Dt}}\right)^2]$$

$p-n$ junction is formed at the place, where boron concentration equals the concentration of impurities in the bulk silicon substrate, that is:

$$\frac{Q}{\sqrt{\pi Dt}}\exp[-\left(\frac{x_j}{2\sqrt{Dt}}\right)^2]=N_D$$

Solving this equation with respect to x_j ,

$$x_j=2\sqrt{Dt}\sqrt{\ln\left[\frac{Q}{N_D\sqrt{\pi Dt}}\right]}$$

Substituting the numerical values of Q , D , N_D and t , into this expression yields

$$x_j=2{,}7\ \mu\text{ m.}$$

4b58.
The capacitance of quantum dot with a radius r:

$$C=4\pi\varepsilon\varepsilon_0 r\ ,$$

where ε is the dielectric constant of the material, surrounding the quantum dot (for GaAs, ε=13.2) ε0=8.85g10-12F/m. If there is one electron on the dot, due to the presence of the second electron, the electrostatic energy of the dot will increase by ΔE=e2/c. This means that the change in point’s potential

$$\Delta V=\frac{\Delta E}{e}=\frac{e}{C}=\frac{e}{4\pi\varepsilon\varepsilon_0 r}=11mv$$

Hence it follows that the change of gate voltage about 10mV will give rise to the step on the current-voltage characteristics, i.e. coulomb step of coulomb staircase is about of 10 mVr.

4b59.
In the mode of photocurrent, the diode is under bias voltage and when lightingthe current I=-(I0+IΦ) flows through it where IΦ is photocurrent, which in the case of internal quantum yield equal to one is

$$I_\Phi=e\frac{p}{h\nu}=e\ \frac{p\lambda}{hc}=6\cdot10^{-3}\text{ A.}$$

Here e is the value of electron charge, c is the light speed, v is the light frequency.

$$\text{Thus, } I=-(I_0+I_\Phi)=-(I_0+\frac{ep}{h\nu})\approx -6\text{ mA}\quad (I_0\ll I_\Phi)\ .$$

In photoemf mode $I=I_0(e\frac{eV_{xx}}{kT})-I_\Phi=0,$ therefore

$$V_{xx}=\frac{kT}{e}\ln(1+\frac{I_\Phi}{I_0})\approx\frac{kT}{e}\ln\frac{I_\Phi}{I_0}\ ,$$

where k is the Boltzmann constant. Putting the numerical values, the following is obtained:

$$V_{xx}=0.35\text{ V.}$$

4b60.
Estimate the value of field strength by considering the equilibrium conditions, when in each cross section of the base, current density of majority carriers is equal to zero.

$$j_n=j_{nD}+j_{nE}=eD_n\frac{dn}{dx}+e\mu_n E\cdot n(x)=0\ .$$

Here $D_n=\frac{kT}{e}\mu_n$ is the electron diffusion coefficient, μ_n is mobility, κT is the quantum of thermal energy, e is the elementary charge, E is the electric field strength.
Using the local electro neutrality condition $n_0(x)=N_0(x)$ from (1) it can be written as:

$$E(x)=-\frac{D_n}{\mu_n n(x)}\frac{dn(x)}{dx}=-\frac{kT}{e}\frac{1}{N_D(x)}\frac{dN_D(x)}{dx}=\frac{kT}{e}\frac{1}{L_0}=\text{const}(y)\ .$$

Such an electrical field also affects the movement minority carriers / holes/, injected to the base. The drift time of their movement through the base is

$$t_{dr} = \frac{W}{\mu_p E} = \frac{WL_0}{D_p} .$$

And the diffusion transition time of holes is : $t_{dif} = \frac{W^2}{2D_p}$.

Dividing these values to each other the following is obtained:

$$\frac{t_{dr}}{t_{dif}} = \frac{WL_0}{D_p} \bigg/ \frac{W^2}{2D_p} = \frac{2L_0}{W} .$$

4b61.

In case of constant gate charge $Q_G = Const$, the charge Q_{sc} in space charge region will also remain constant $Q_G = G_{sc}$. The total charge in surface potential well of MIS structure consists of free charges, created in the well due to thermal generation and ionized donor charge in total depletion layer of width $W(t)$ at the moment of time t:

$$Q_{sc} = Q_p + Q_d$$

(semiconductor is considered to be of n - type).

Here

$$Q_d = eN_d W(t) \qquad \text{and}$$

$$Q_p = \int_0^t \frac{en_i}{2\tau_o} W(t)dt = \frac{en_i}{2\tau_o}\int_0^t W(t)dt$$

As

$$Q_d + Q_p = Q_G = Const,$$

$$\frac{dQ_p}{dt} = -\frac{dQ_p}{dt},$$

$$\frac{en_i}{2\tau_o} W(t) = -eN_d \frac{dW}{dt},$$

$$\frac{dW}{dt} = -\frac{n_i}{2\tau_o N_d} W(t),$$

$$W(t) = W(0)\exp\left(-\frac{n_i}{2\tau_o N_d} t\right) .$$

Hence it follows that relaxation time

$$\tau_{relax} = 2\tau_0 \frac{N_d}{n_i} .$$

4b62.

The voltage, applied between the gate and the semiconductor at any arbitrary instance of time is distributed along dielectric (oxide) layer and semiconductor space charge layer.

$$V_G = \psi_s + \frac{Q_{sc}}{C_{ox}} = Const .$$

Or taking a derivative

$$C_{ox}\frac{d\psi_s}{dt} + \frac{dQ_{sc}}{dt} = 0 .$$

Here C_{ox} is the insulator layer capacitance, Q_{sc} is the space charge value at given moment of time, ψ_S is the surface potential of a semiconductor which is connected to the W with the following relation:

$$W(t) = \sqrt{\frac{2\varepsilon\varepsilon_o\psi_s}{eN_d}} .$$

Or

$$\frac{dW}{dt}=\sqrt{\frac{2\varepsilon\varepsilon_o}{eN_d}}\frac{1}{2\sqrt{\psi_s}}\frac{d\psi_s}{dt}=C_B\frac{d\psi_s}{dt}\frac{1}{eN_D},$$

where $C_B=\sqrt{\frac{e\varepsilon\varepsilon_0 N_d}{2\psi_s}}$ is a depletion layer capacitance.

So

$$\frac{d\psi_s}{dt}=\frac{eN_d}{C_B}\frac{dW}{dt}.$$

As $Q_{sc}=Q_p+Q_d$, then

$$\frac{dQ_{sc}}{dt}=\frac{dQ_p}{dt}+\frac{dQ_B}{dt}=\frac{en_i}{2\tau_0}W(t)+eN_D\frac{dW(t)}{dt}.$$

Using the above expressions, the following equation can be derived:

$$eN_d\frac{C_{ox}}{C_B}\frac{dW}{dt}+\frac{en_i}{2\tau_o}W(t)+eN_d\frac{dW}{dt}=0.$$

Or finally

$$\frac{dW}{dt}=-\frac{n_i}{2\tau_o N_D\left(1+\frac{C_{ox}}{C_B}\right)}W(t)=-\frac{W(t)}{\tau_{pen}}.$$

Thus

$$\tau_{relax1}(V_G=const)=2\tau_o\frac{N_d}{n_i}\left(1+\frac{C_{ox}}{C_B}\right)>\tau_{relax}\left(Q_G=Const\right),$$

i.e. the relaxation time of MIS-structure in case of constant gate voltage is more than in case of constant gate charge.

4b63.

The differential resistance of collector junction is:

$$r_k=\left.\frac{dUk}{dI_k}\right|_{I_e=const}=\left.\frac{dU_k}{dW}\frac{dW}{d\alpha}\frac{d\alpha}{dI_k}\right|_{I_e=const},$$

where $\alpha-$ current transfer coefficient of a transistor

$$\alpha=\frac{\partial I_K}{\partial I_E}=\frac{\partial I_{Ee}}{\partial I_E}\frac{\partial I_K}{\partial I_{Ee}}=\gamma\chi,$$

here γ is the efficiency of the emitter $\gamma\approx 1-\frac{N_D}{N_A}\approx 1,$

χ - efficiency of electrons transfer through the base, which for $W<<L_p$,

$$\chi\approx 1-\frac{1}{2}\left(\frac{W}{L_p}\right)^2:$$

In case of high doped asymetrical p^+-n junction $\left(N_A>>N_D\right)$, the space charge layer is mainly located in the base layer and

$$\ell_{p-n}=\sqrt{\frac{2\varepsilon\varepsilon_o(\Delta\varphi_k-U_k)}{eN_D}}.$$

Here $\Delta\varphi_k$ - contact potential difference, U_k - collector voltage, e - elementary charge value. Therefore changing U_k, the ℓ_{p-n} and the width W of the base are changed, as a result of which transfer coefficient α is changed (Early effect). Thus,

$$r_k = \frac{dU_k}{d\ell_{p-n}} \frac{d\ell_{p-n}}{dW} \frac{dW}{d\chi} \frac{d\chi}{d\alpha} \frac{d\alpha}{dI_k}.$$

Considering that

$$\frac{d\ell_{p-n}}{dW} = -1:$$

$$\frac{dU_k}{d\ell_{p-n}} = \frac{1}{\dfrac{d\ell_{p-n}}{dU_k}} = \sqrt{|U_k|}\sqrt{\frac{2eN_D}{\varepsilon\varepsilon_o}} \qquad (-U_k >> \Delta\varphi_k).$$

On the other hand,

$$\frac{dW}{d\chi} = \frac{1}{\dfrac{d\chi}{dW}} = \frac{1}{-\dfrac{W}{L_{p^2}}} = -\frac{L_{p^2}}{W},$$

$$\frac{d\chi}{d\alpha} = \frac{1}{\gamma} \approx 1,$$

$$\frac{d\alpha}{dI_k} = \frac{1}{I_e}, \quad I_k = \alpha I_e$$

Finally,

$$r_k = \sqrt{\frac{2eN_D}{\varepsilon\varepsilon_o}}\sqrt{|U_k|}\cdot(-1)\left(-\frac{L_{p^2}}{W}\right)\cdot\frac{1}{\gamma}\cdot\frac{1}{I_e} = \sqrt{\frac{2eN_D}{\varepsilon\varepsilon_o}}\frac{L^2{}_{p^2}}{W}\frac{\sqrt{|U_k|}}{\gamma I_e}$$

After putting numerical values:

$$r_k \approx 5{,}2 \ MOhm$$

4b64.

As a such maximum temperature one can consider the temperature, when the intrinsic concentration of charge carriers becomes equal to the electron concentration introduced by donors: $n_i = N_d$.

Or

$$(N_c \cdot N_v)^{1/2} \exp\left(-\frac{E_g}{2kT_{cr}}\right) = N_D \quad .$$

Hence

$$T_{cr} = \frac{E_g}{2k} \frac{1}{\ln\sqrt{\dfrac{N_c N_v}{N_D}}}.$$

For Si:

$$N_c = 2.5\cdot 10^{19}\left(\frac{m_{dn}{}^x}{m_o}\right)^{3/2}\left(\frac{T}{300}\right)^{3/2} cm^{-3} = 2{,}8\cdot 10^{19}\left(\frac{T}{300}\right)^{3/2} cm^{-3}$$

$$N_v = 2{,}5\cdot 10\left(\frac{m_{dp}{}^x}{m_o}\right)^{3/2}\left(\frac{T}{300}\right)^{3/2} cm^{-3} = 1{,}02\cdot 10^{19}\left(\frac{T}{300}\right)^{3/2} cm^{-3},$$

Therefore

$$\frac{T_{cr}}{300} = \frac{E_g}{2k\cdot 300}\frac{1}{\ln\dfrac{\sqrt{N_c N_v}}{N_D}} = \frac{22{,}2}{\ln(10^4\sqrt{2{,}8\cdot 1{,}02}) + \dfrac{3}{2}\ln(\dfrac{T_{cr}}{300})} \quad ,$$

Denoting $x = \dfrac{T_{cr}}{300}$, the following transcendent equation will be found:

$$\frac{22{,}2}{x} = 9.73 + 1{,}5\ln x,$$

the solution of which is $x \approx 2.1$, or $T_{cr} = 630\ K$.

4b65.

inter-surface distance is defined by:

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}},$$

where h, k, l are Miller indices.

Therefore:

$$d_{100} = \frac{4{,}11 \cdot 10^{-10}}{\sqrt{1^2 + 0^2 + 0^2}} = 4{,}11 \cdot 10^{-10}\ \text{m}.$$

Similarly:

d_{110}=2,9*10^{-10}; d_{111}=2,37*10^{-10}; d_{132}=1,1*10^{-10} m.

4b66.

For calculation of Miller indices it is necessary:

a. To find intercepts of the given plane with the three basis axes x, y, z of cubic crystal;

b. To take the reciprocals of these numbers;

c. To reduce them to the smallest three integers having the same ratio.

For the given plane, there are the following:

a. Intercepts are equal to: $x_0 = 1$; $y_0 = 2$; $z_0 = 3$;

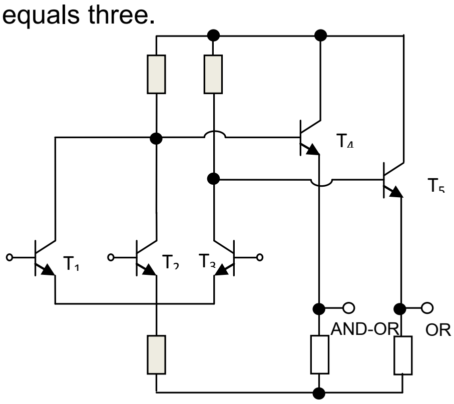
b. Reciprocal values are equal to: 1/2; 1/3; 1;

c. Smallest three integers are equal to: 1; 1/2; 1/3.

So, Miller indices of the given plane are as follows (632).

4b67.

Collector of T_1 and T_2 transistors are conjugated, therefore they can be set in the same isolation region. Analogically in the other isolation region T_4 and T_5 transistors can be set. T_3 transistor has different collector voltage, therefore it should be set on another isolation region. Preparation of resistances, depending on their value, can be fully implemented in any isolation region. So, the minimum number of isolation regions equals three.



4b68.

The crystal resistance in T_1=20^{0}C=293K temperature is defined by the following formula:

$$R_1 = R_\infty \exp\left(\frac{\Delta E_g}{2kT_1}\right).$$

In T_2 = 80^{0}C= 353 K temperature, the crystal resistance will be:

$$R_2 = R_\infty \exp\left(\frac{\Delta E_g}{2kT_2}\right).$$

Therefore

$$\frac{R_1}{R_2} = \frac{R_\infty \exp\left(\frac{\Delta E_g}{2kT_1}\right)}{R_\infty \exp\left(\frac{\Delta E_g}{2kT_2}\right)} = \exp\left(\frac{\Delta E_g}{2kT_1} - \frac{\Delta E_g}{2kT_2}\right)$$

$$R_2 = \frac{R_1}{\exp\left(\frac{\Delta E_g (T_2 - T_1)}{2kT_1T_2}\right)} = 1.38 \cdot 10^3\, Ohm$$

4b69.
In case of spherical metallographic section method, p-n junction depth is measured by the following formula:

$$d = \left(D_1^2 - D_2^2\right)/4D.$$

Putting the corresponding values, the following will be obtained:

$$d = \frac{(3)^2 - (2)^2}{4 \times 60} = 0.02 \text{ mm} = 20 \text{ um}.$$

4b70.
Symbols of plane passing through points A,B and C can be determined by solving the system of three equations of the following type $hx + ky + lz = 1$. The result obtained is $(hkl) = (111)$. The angle between the crystalline planes (111) and (121) can be determined using the scalar product of vectors perpendicular to the planes: $\cos\alpha = 4/\sqrt{18}$.

4b71.
At temperature T=0K Fermi energy F is determined though conduction electron concentration n as $F = \frac{\hbar^2}{2m}(3\pi^2 n)^{2/3}$. In face-centred cubic crystal the concentration of atoms equals $n_{atom} = 4/a^3$. Therefore $n/n_{atom} = (2mF/\hbar^2)^{3/2}\frac{a^3}{12\pi^2} \cong 3.3\cdot$

4b72.
Continuity equation $\frac{d\Delta n}{dt} = -R$ for electrons can be presented in form $\frac{d\Delta n}{dt} = -\alpha_n\left[(n_0 + \Delta n)(p_0 + \Delta p)\right]$, where n_0 and p_0 are the equilibrium and Δn and Δp non-equilibrium concentrations of electrons and holes, correspondingly. As well $n_0 p_0 = n_i^2$, $\Delta n = \Delta p$ then $\frac{d\Delta n}{dt} = -\alpha_n\left[(\Delta n)^2 + n_0\Delta n)\right]$. Solving the diff-equation with $\Delta n(t=0) = \Delta n_{st}$ initial condition one obtained $\Delta n(t) = \frac{n_0\Delta n_{st}}{(n_0 + \Delta n_{st})e^{\alpha_n n_0 t} - \Delta n_{st}}$.

4b73.
From $m\frac{d^2x}{dt^2} = eE_0\sin\omega t$ Newton equation of electron in electromagnetic field $E = E_0\sin\omega t$ it follows that electron displacement from the equilibrium state is determined as $x = -\frac{eE_0}{m\omega^2}\sin\omega t$. Therefore, for the polarization, i.e. unit volume dipole momentum one has $P = enx = -\frac{eE_0\sin\omega t}{m\omega^2}en$. Using relation $P = \chi\varepsilon_0 E = (\varepsilon_r - 1)\varepsilon_0 E$, for dielectric permittivity one obtains $\varepsilon = \varepsilon_0(1 - \frac{en^2}{\varepsilon_0 m\omega^2})$.

4b74.
1. The ray absorption is performed by exponential law $F = F_0 e^{-\alpha x}$, where F is the intensiveness in *x* depth, therefore $x_1 = \frac{1}{\alpha}\ln\frac{F_0}{F_1} = 10^{-6}\ln 10^{11} \cong 0{,}25$ um.

2. $x_2 = \frac{1}{\alpha}\ln\frac{F_0}{F_2} = 10^{-6}\ln F_0 \cong 0{,}375$ um.

3. So, the active layer width $d = x_1 - x_2 \approx 0{,}12$ um.

4b75.
1. From the ray absorption law:

$F_1(x) = F_{01}e^{-\alpha_1 x}$, and $F_2(x) = F_{02}e^{-\alpha_2 x}$, therefore $\dfrac{F_2(x)}{F_1(x)} = \dfrac{F_{02}e^{-\alpha_2 x}}{F_{01}e^{-\alpha_1 x}} = \dfrac{F_{02}}{F_{01}}e^{x(\alpha_1-\alpha_2)}$.

2. In x_1 point $F_1(x_1) = 2F_2(x_1) = \dfrac{F_2(x_1)}{F_{02}}F_{01}e^{-x_1(\alpha_1-\alpha_2)}$.

From (1) $x_1 = \dfrac{1}{\alpha_2}\ln\dfrac{F_{02}}{F_2(x_1)} = 5{,}67\cdot 10^{-7}\ln 10^{11} \approx 0.143\,\text{um}$.

3. From (2) $F_{01} = 2F_{02}e^{x_1(\alpha_1-\alpha_2)}$, and $x_1(\alpha_1-\alpha_2) = 3{,}171$,

therefore $F_{01} = 2F_{02}e^{x_1(\alpha_1-\alpha_2)} = 2\cdot 10^{16}e^{3,6} = 7{,}3\cdot 10^{17}$ qv/*cm*$^2\cdot$ *v.*

4b76.
It is known that the permittivity coefficient of rectangular potential barrier:

$$D = D_0 e^{-\frac{2}{\hbar}\sqrt{2m(E_0-E)}d}.$$

The permittivity coefficient of an electron:

$$D_e = D_0 e^{-\frac{2}{1{,}054.10^{-34}}\sqrt{2\cdot 9{,}1\cdot 10^{-31}\cdot 1.6\cdot 10^{-19}}\,0.2\cdot 10^{-9}} \approx 0.2e^{-2.16} = 0.023$$

Proton permittivity coefficient:

$$D_p = D_0 e^{-\frac{2}{1{,}054.10^{-34}}\sqrt{2\cdot 1{,}67.10^{-27}\cdot 1.6\cdot 10^{-19}}\,0.2\cdot 10^{-9}} \approx 0.2e^{-216} = 4.8\cdot 10^{-19}$$

4b77.
$\Delta\delta_{st}$ stationary photoconductance:

$$\Delta\delta_{st} = q\Delta n_{st}(\mu_n + \mu_p)$$

At switching off the light, the density of nonequilibrium charge carriers decreases by the following law:

$$\Delta n = \Delta n_{st}\, e^{-\frac{(t-t_1)}{\tau}}$$

Hence it follows that

$$\Delta\delta_{st}/2 = q\Delta n_{st}(\mu_n+\mu_p)/2 = \Delta\delta_{st}\, e^{-\frac{(t_2-t_1)}{\tau}}$$

therefore $\dfrac{(t_2-t_1)}{\tau} = \ln 2$, or $t_2 - t_1 = \tau\cdot\ln 2 = 0.69\cdot 10^{-6}$ v.

4b78.

The number of free places in the crystal with N atoms is: $n = Ne^{-\frac{E}{kT}}$;

Free places per atom: $n_1 = \dfrac{n}{N} = e^{-\frac{E}{kT}}$

For $T_1 = 300^\circ$K $n_1 = e^{-\frac{0.75\cdot 1.6\cdot 10^{-19}}{1.38\cdot 10^{-22}\cdot 300}} \approx 25\cdot 10^{-14}$

For T2 = 600ºK $n_1 = e^{-\frac{0.75 \cdot 1.6 \cdot 10^{-19}}{1.38 \cdot 10^{-22} \cdot 600}} \approx 5 \cdot 10^{-7}$

4b79.

$E = F \pm \delta$; F is the Fermi energy: $f = \dfrac{1}{e^{\frac{E-F}{kT}} + 1}$

$f_1 = \dfrac{1}{e^{\frac{F+\delta-F}{kT}} + 1} = \dfrac{1}{e^{\frac{\delta}{kT}} + 1}$; f_1 is the probability of being above by δ;

$f_2 = \dfrac{1}{e^{\frac{-\delta}{kT}} + 1}$ is the probability of being below by δ.

The sum of probabilities of being and not being in any level is always = 1 $f_{being} + f_{not\ being} = 1$

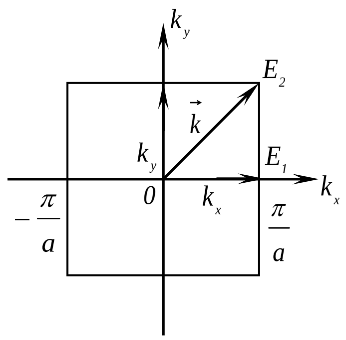
Add f_1 and f_2

$$f_1 + f_2 = \frac{1}{e^{\frac{\delta}{kT}} + 1} + \frac{1}{e^{\frac{-\delta}{kT}} + 1} = \frac{e^{\frac{-\delta}{kT}} + 1 + e^{\frac{\delta}{kT}} + 1}{1 + e^{\frac{-\delta}{kT}} + 1 + e^{\frac{\delta}{kT}}} = 1$$

$f_1 + f_2 = 1$ is obtained because $f_{1being} + f_{1not\ being} = 1$, therefore $f_2 = f_{1not\ being}$

f_2 is the probability of being below by δ; $f_{1not\ being}$ the probability of not being above by δ;

4b80.



$$E_1 = \frac{\hbar^2 k_x^2}{2m}$$
$$E_2 = \frac{\hbar^2 k^2}{2m}$$
$$|k|^2 = k_x^2 + k_y^2 = 2k_x^2$$
$$k_x = k_y$$

$$E_2 = \frac{\hbar^2 k^2}{2m} = \frac{\hbar^2 2k_x^2}{2m} = \frac{\hbar^2 k_x^2}{2m}$$
$$\frac{E_2}{E_1} = \frac{\hbar^2 k_x^2}{m} : \frac{\hbar^2 k_x^2}{2m} = 2$$

4b81.

The velocity of an electron as a group velocity of an electronic wave is defined as:

$\nu = \frac{1}{\hbar} E_o \cdot a \cdot (-\sin k_x a)$. As $\nu_F = \nu_{\max}$, then ν_{max} will be if $|-\sin k_x a| = 1 \Rightarrow \nu_F = \frac{1}{\hbar} E_o \cdot a \approx 2.3 \cdot 10^7$ cm/s.

4b82.

If the semiconductor is of n type and F= E_d, then the issue is about low temperature when it is still possible to ignore band to band transition and accept that electrons appeared in the conduction band at the expense of donor ionization: $n = N_\eta^+$. The probability of the particle being on discrete level is given by Gibs distribution:

$$f = \frac{1}{\frac{1}{g_i} e^{\frac{E_i - F}{kT}} + 1}.$$

E_i is the discrete level, g_i - its degeneration degree. If coupled-hole must be located on donor level, then $g_{i(\eta)} = \frac{1}{2}$. According to problem, $E_i = F$ (in this case $E_i = E_\eta$).

$$f = \frac{1}{\frac{1}{\frac{1}{2}} e^{\frac{E_\eta - F}{kT}} + 1} = \frac{1}{2e^{\frac{E_\eta - F}{kT}} + 1}$$

$$N_\eta^+ = \frac{N_\eta}{2e^{\frac{E_\eta - F}{kT}} + 1} = n$$

if $E_\eta = F$, then $n = \frac{N_\eta}{3}$

4b83.

The semiconductor density under the influence of light will be:

$$n = n_0 + \delta_n = 10^{16} + 10^{15} = 1.1 \cdot 10^{16} cm^{-3}$$

$$p = p_0 + \delta_p = 10^{15} cm^{-3}$$

Respectively, Fermi quasienergies are equal.

$$F_n - E_i = kT \ln \frac{n}{n_i} = 0.0259 \cdot \ln \frac{1.1 \cdot 10^{16}}{2 \cdot 10^{13}} = 163 meV$$

$$F_p - E_i = -kT \ln \frac{p}{n_i} = 0.0259 \cdot \ln \frac{1 \cdot 10^{15}}{2 \cdot 10^{13}} = -101 meV$$

For comparison, Fermi energy in case of the lack of light equals:

$$E_F - E_i = kT \ln \frac{n_0}{n_i} = 0.0259 \cdot \ln \frac{10^{16}}{2 \cdot 10^{13}} = 161 meV$$

which in its value is rather close to Fermi quasienergy for majority carriers;

4b84.

The efficiency of an emitter equals:

$$\gamma E = \frac{1}{1 + \frac{D_{p,E} N_B w'_B}{D_{n,B} N_E w'_E}} = 0.994$$

The transfer coefficient of the base equals:

$$\alpha_T = 1 - \frac{{w'_B}^2}{2 D_{n,B} r_n} = 0.9992$$

The transfer coefficient of the current is computed from the following equation:

$$\beta = \frac{\alpha}{1 - \alpha} = 147.5$$

where α transfer coefficient has been computed as a product of the efficiency of an emitter and the result of transfer coefficient of the base;

$$\alpha = \gamma E \; \alpha_T = 0.994 \cdot 0.9992 = 0.993$$

4b85.

$a_\tau = \frac{eE}{m} \Rightarrow v_D = a_\tau \cdot \tau = \frac{eE\tau}{m}$, $v_D = \mu E \Rightarrow \mu = \frac{v_D}{E} = \frac{e\tau}{m}$, $\sigma = en\mu = \frac{e^2 \tau}{m} \Rightarrow \tau = \frac{\sigma m}{e^2 n}$

$$\sigma = en\mu = \frac{e^2\tau}{m} \Rightarrow \tau = \frac{\sigma m}{e^2 n},\ \frac{3}{2}kT = \frac{mv^2}{2} \Rightarrow v_D = \sqrt{3kT/m}$$

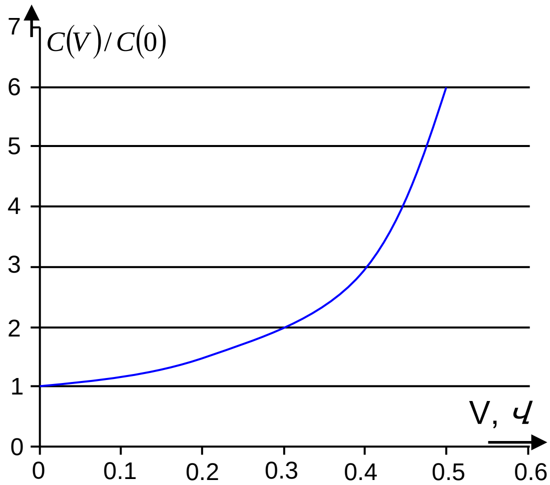
$$\lambda = v_D\tau \Rightarrow \lambda = v_D \cdot \frac{\sigma m}{e^2 n} = \sqrt{3kT/m} \cdot \frac{\sigma m}{e^2 n} =$$

$$\frac{3}{2}kT = \frac{mv^2}{2} \Rightarrow v_D = \sqrt{3kT/m} = \sqrt{3\cdot 1.38\cdot 10^{-28}\cdot 300/9.11\cdot 10^{-28}} = 11.67\, cm/sec$$

$$\lambda = v_D\tau \Rightarrow \lambda = v_D \cdot \frac{\sigma m}{e^2 n} = 11.67\cdot 3.3\cdot 10^{-11} = 38.511\cdot 10^{-11} cm$$

4b86.

It is known that $C(0) = \sqrt{\frac{q\varepsilon\varepsilon_0 N}{2\varphi_b}}$, and $C(V) = \sqrt{\frac{q\varepsilon\varepsilon_0 N}{2(\varphi_b - V)}}$ £ . Therefore, their $C(V)/C(0)$ ratio will be $\frac{C(V)}{C(0)} = \sqrt{\frac{\varphi_b}{(\varphi_b - V)}}$, and the respective curve will have the following form:



4b87.
The width of depletion layer is defined by the following formula:

$w = \left(\frac{2\varepsilon\varepsilon_0(\varphi_b - V)}{qN_a}\right)^{1/2}$, hence $V = \varphi_b - \frac{qw^2 N_a}{2\varepsilon\varepsilon_0}$ £

Putting numerical values, the following will be obtained:

1. $V = \varphi_b - \frac{qw^2 N_a}{2\varepsilon\varepsilon_0} = 0.6 - \frac{1.9*10^{-19}*5*10^{14}*10^{-10}}{2*12*8.86*10^{-14}} = 0.59V$

2. $V = \varphi_b - \frac{qw^2 N_a}{2\varepsilon\varepsilon_0} = 0.6 - \frac{1.9*10^{-19}*5*10^{14}*2*10^{-10}}{2*12*8.86*10^{-14}} = 0.45\ V$

4b88.
In homogeneous environment, F intensity of the ray depends on x depth of absorption by Buger - Lambert law.

$F = F_0 e^{-\alpha x}$, where F_0 – initial intensity, F – intensity in x depth, α - absorption coefficient.

It is obvious that in x = 0.5 mkm depth, where the intensities of two waves equal each other, the following condition takes place:

$F_1 = F_{01}e^{-\alpha_1 x} = F_2 = F_{02}e^{-\alpha_2 x}$, hence

$$\frac{F_{02}e^{-\alpha_2 x}}{F_{01}e^{-\alpha_1 x}} = \frac{F_{02}}{F_{01}} e^{-x(\alpha_2 - \alpha_1)} = 1,$$

hence

$F_{02} = F_{01}e^{x(\alpha_2 - \alpha_1)}$. Putting the value, the following will be obtained:

$F_{02} = F_{01}e^{x(\alpha_2 - \alpha_1)} = 10^{15} e^{5\cdot10^{-5}\cdot 2\cdot10^{5}} = 2.2\cdot10^{19}$ qv./cm^2·s.

4b89.

The length of drift of holes $L_d = E\mu_p \tau_p$.

Use diffusion length and Einstein relations:

$$L_p = (D_p \tau_p)^{1/2} \text{ and } D_p / \mu_p = kT/q:$$

Putting the above equation in the expression of drift length, the following will be obtained:

$$L_d = L_p^2 qE/kT = 0.09 \text{ cm}.$$

4b90.

The forward-bias current can be written as follows:

$J \sim \exp(-E_g / k_B T)\exp(eV / k_B T)$.

Therefore, for a given temperatures the following will be obtained:

$$J_2 / J_2 = \frac{\exp(-E_g / k_B T_2)\exp(eV_2 / k_B T_2)}{\exp(-E_g / k_B T_1)\exp(eV_1 / k_B T_1)}.$$

If current is to remains constant, then $J_1 = J_2$ and:

$\exp([-E_g + eV_2]/k_B T_2) = \exp([-E_g + eV_1]/k_B T_1)$.

Then, V_2 = 0.58 V is obtained. The change in the forward-bias voltage is 0.02 V.

4b91.

Average energy of electron is determined as $\overline{E} = \int Ef(E)d\mathbf{k} / \int f(E)d\mathbf{k}$, where $f(E)$ is the Fermi-Dirac distribution function. From the relation $E = \hbar^2 k^2 / 2m$ between the electron energy and momentum it follows that the average energy of electron is $\overline{E} = \int f(E)E^{3/2}dE / \int f(E)E^{1/2}dE$. Using the behavior of the Fermi-Dirac function at $T = 0$, for the electron average energy $\overline{E}(T=0) = \int\limits_0^F E^{3/2}dE / \int\limits_0^F E^{1/2}dE = \frac{3}{5}F$ is obtained. At temperature T=0 K Fermi energy F is determined through n concentration of conduction electron as $F = \frac{\hbar^2}{2m}(3\pi^2 n)^{2/3}$. Therefore $\overline{E}(T=0) = \frac{3}{10}\frac{\hbar^2}{m}(3\pi^2 n)^{2/3}$.

4b92.

Solution of the continuity equation $\frac{d^2\Delta p}{dx^2} - \frac{eE}{k_B T}\frac{d\Delta p}{dx} - \frac{\Delta p}{L_P} = 0$ is $\Delta p = \Delta p(x=0)\exp(kx)$, where $k = 1/2l(1 - \sqrt{1 + 4l/L_E})$, $l = k_B T / eE$, $L_E = eEL_p^2 / k_B T$. In the given case $l / L_p << 1$. Therefore $k \approx -1/L_E$ and $\Delta p = \Delta p(x=0)\exp(-x/L_E)$.

4b93.

It is known that $I_x = J_x S$, $S = d_y d_z$, $J_x = (en\mu_n + ep\mu_p)E_x = \sigma E_x$, $V_x = E_x d_x$. The Hall's voltage determined as $V_H = R_H J_x B d_z$ where $R_H = \frac{r}{e}\frac{p\mu_p^2 - n\mu_n^2}{(n\mu_n + p\mu_p)^2}$ is the Hall's coefficient, r is the Hall's factor which is order of unit ($r \approx 1$). Therefore for the Hall's voltage there is $V_H = \frac{1}{e}\frac{p\mu_p^2 - n\mu_n^2}{(n\mu_n + p\mu_p)^2}\frac{I_x}{d_z}B$.

From the $V_H < 0$ condition of the problem it follows that semiconductor conductivity is n-type ($n > p$).

Then $V_H = \frac{1}{en}\frac{I_x}{d_z}B$ or $n = \frac{1}{eV_H}\frac{I_x}{d_z}B$. Therefore electron conductivity and mobility can be calculated on the base of relations $\rho = E_x / J_x$ and $\mu_n = 1/en\rho$.

4b94.

Input power on photoreceiver will be:

$$P = \frac{\mathrm{hc}}{\lambda}\mathrm{r_p} = \frac{1.05 * 10^{-34} * 3 * 10^{8}}{1.5 * 10^{-6}}10^{10}W = 1.32 * 10^{-9}W$$

Therefore photocurrent equals: $\mathrm{I_p} = \mathrm{RP} = 0.6\frac{\mathrm{A}}{\mathrm{W}} * 1.32 * 10^{-10}W = 7.95 * 10^{-10}W$

Output current of photocurrent with internal amplification: $I = M\, I_p = 20 * 7.95 * 10^{-10}A = 15.9nA$

Therefore quantum output will equal:

$$\eta = \frac{\mathrm{I_p/e}}{\mathrm{r_p}} = \frac{7.95{*}10^{-10}{*}\frac{1}{1.6{*}10^{-19}}}{10^{10}} \approx 0.5$$

Note that e is the electron charge value.

4b95.

It is known that in non-degenrate semiconductor, the distance of Fermi level from the center of bandgap is given by

$$\varphi_0 = \frac{kT}{e}ln\frac{n_0}{n_i}$$

expression where n_i – intrinsic concentration of carriers, n_0 – concentration of electroncs in conduction band.

On the other hand, the following values are given:

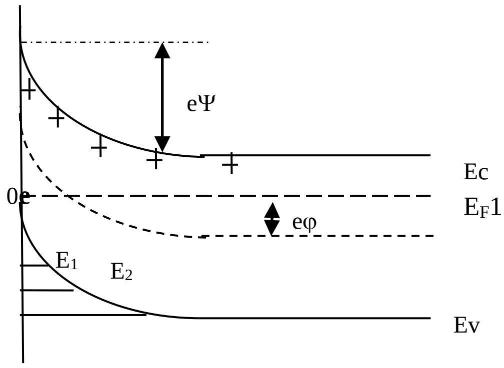
m_h= 0.56 m_0

ε = 11.8

N_c^*=3.6*10^{18}cm^{-3} (T=77K)

n_i = 3*10^{-20} cm^{-3} (T=77K)

N_v^*=1.4*10^{18}cm^{-3} (T=77K)



In the well Q_{free} << Q_B, i.e. volume charge is mainly due to the ionized donors, and as their concentration is constant, the potential well can be assumed triangular.

Find $\mathrm{e}\varphi_0 = \mathrm{E_F} - \mathrm{E_i} = \mathrm{kTln}\frac{\mathrm{N_D}}{\mathrm{n_i}} = 0.45\mathrm{eV}$

Knowing ψ_S , Q_B can be found.

$$Q_B = \sqrt{2e\varepsilon\varepsilon_0 N_D\psi_S} = \sqrt{4e\varepsilon\varepsilon_0 N_D\varphi_0}$$

Therefore, strength of the electric field at the surface:

$$E_S = \frac{Q_B}{\varepsilon\varepsilon_0} = \sqrt{\frac{4eN_D\varphi_0}{\varepsilon\varepsilon_0}} = 5.3 * 10^6 V/cm$$

It is known that the energy of the bottom of the first subzone in a linear is given by the following formula:

$E_0 = \left[\frac{ehE_S}{(2m_h)^{1/2}}\right]^{\frac{2}{3}}\gamma_0$, where $\gamma_0 = 2.238$ the first zero of the Airy function.

Therefore $E_0 = 0.103$ eV.

The distance from the Fermi level E_F to the valence band E_{Vs} at the surface is $E_g - (E_c - E_F)$, i.e.

$$E_F - E_{Vs} = \left(E_g - E_F\right) - 2\varphi_0 = \left(E_g - E_F\right) - 2(E_F - E_i) = (E_g - E_F) - 2kTln\frac{N_D}{n_i} =$$
$$= E_g - kTln\frac{N_c}{N_D} - 2kTln\frac{N_D}{n_i}$$

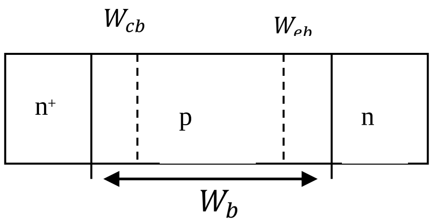
i.e.

$E_F - E_{Vs} = E_g - kTln\frac{N_c}{N_D}\left(\frac{N_D}{n_i}\right)^2 = E_g - kTln\frac{N_c N_D}{{n_i}^2} = 0.13$ eV

Therefore

$$N_D = \frac{kT}{\pi\hbar^2}\mathrm{m}_\mathrm{n}^* \ln\left(1 + \exp\left(-\frac{E_F - E_{Vs} - E_1}{kT}\right)\right) \approx \frac{kT}{\pi\hbar^2}\mathrm{m}_\mathrm{n}^*\exp\left(-\frac{E_F - E_{Vs} - E_1}{kT}\right) = 1.1 * 10^{-3}\frac{1}{cm^2}$$

4b96.



It is known that for silicon $n_i(300) = 1.6 * 10^{10} cm^{-3}$.
Puncture occurs when

$$W_{cb} = W_b - W_{eb}$$

It is possible to find:

$$\varphi_{oe} = KTln\frac{N_D * N_A}{n_i^2} = 0.025ln\frac{10^{19} * 10^{16}}{1.6^2 * 10^{20}} = 0.025ln\frac{10^{15}}{1.6^2} = 0.902eV$$

And

$$\varphi_{oc} = KTln\frac{N_D * N_A}{n_i^2} = 0.025ln\frac{10^{16} * 5 * 10^{16}}{1.6^2 * 10^{20}} = 0.706eV$$

Also find

$$W_{eb} = \sqrt{\frac{2\varepsilon\varepsilon_0\varphi_{oe}}{eN_D^2\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}} = \sqrt{\frac{2\varepsilon\varepsilon_0\varphi_{oe}N_A}{eN_D(N_A + N_D)}} = 0.2mkm$$

At the puncture

$\mathrm{W_{cb}} = \mathrm{W_b} \text{-} \mathrm{W_{eb}} = 0.5\text{-}0.2 = 0.3$ mkm

As $\quad \mathrm{W}_{cb} = \sqrt{\frac{2\varepsilon\varepsilon_0 \mathrm{N}_\mathrm{D}^c(\varphi_{oc}+\mathrm{eU_{пр}})}{\mathrm{eN}_\mathrm{A}^b(\mathrm{N}_\mathrm{D}^c+\mathrm{N}_\mathrm{A}^b)}}$, hence

$$U_p = \frac{N_A^b(N_D^c + N_A^b){W_{cb}}^2}{2\varepsilon\varepsilon_0 N_D^c} - \frac{\varphi_{oc}}{e} = 13.2\ V$$

The transit time through the base without $(U_\mathrm{K} = 0)$, equals

$$\tau = \frac{W^2}{2D_n} = \frac{(W_b - W_{eb} - W_{cb})^2}{2D_n} = 9.2\ ns,$$

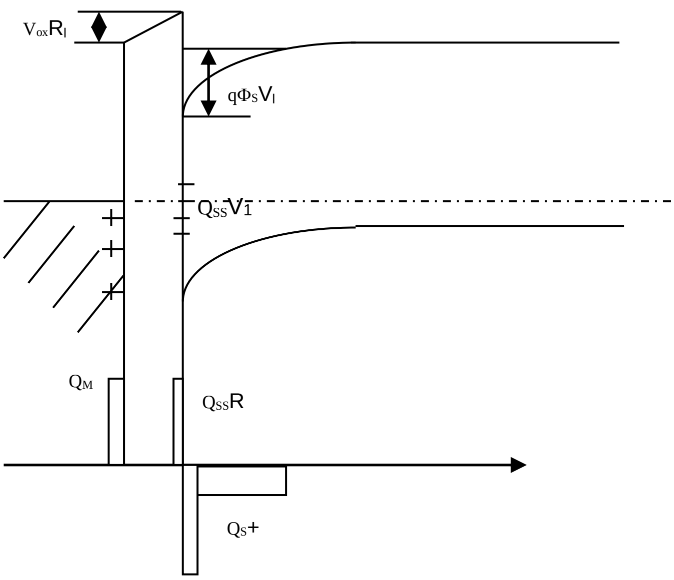
as

$$D_n = 1500 * 0.025\ \frac{cm^2}{c} = 15 * 25\frac{cm^2}{c}$$

Knowimg the transit time we can calculate the maximum operating frequency

$$f = \frac{1}{2\pi\tau} = 17.3\ GHz$$

4b97.



Suppose there is a MOS structure based on p-Si and that the work function of the metal Φ_M is smaller than the work function of semiconductor Φ_s ($\Phi_{MS} = \Phi_s - \Phi_M$). In a semiconductor, a depletion and weak inversion layer is formed, the metal is positively charged, the positive charge is captured by surface states.
Electroneutrality equation is $Q_G + Q_{SS} + Q_S = 0$, where Q_G is the charge on the metal electrode, Q_{SS} is the charge on the surface states, Q_S– the charge in a semiconductor, and $Q_{SS} = Q_e + Q_A$ in p-semiconductor.
It is clear that $Q_G = V_{ox}C_{ox}$, where V_{ox} – voltage drop across the oxide layer.

When $V_G = 0$, the contact potential difference is divided between semiconductor and dielectric:

$$\triangle \phi_{MS} = -\phi_{So} - V_{oxo}$$

External voltage is also divided between semiconductor and oxide:

$V_G = V_{ox} - V_{oxo} + \Phi_S - \Phi_{So} = V_{ox} + \phi_S + \triangle \phi_{MS}$

Or

$$V_G - \triangle \phi_{MS} = \phi_S + \frac{Q_G}{C_{ox}} = \phi_S + \frac{-Q_{SS} - Q_S}{C_{ox}}$$

On the other hand, $V_G - \triangle \phi_{MS} + \frac{Q_{SS}}{C_{ox}} = \phi_S - \frac{Q_S}{C_{ox}}$

In an ideal MOS transistor, $\Phi_S = 0,\ Q_S = 0$, when $V_G = 0$.

In this case $\Phi_S = 0, Q_S = 0$, when $V_G = \triangle \phi_{MS} - \frac{Q_{SS}}{C_{ox}}$

This condition is “flat” zone condition.

4b98.

Define channel depletion layer width in strong inversion mode for $V_{bs}<0$ (1):

$$l(V_{bs}) = l_0 \cdot \sqrt{1 - \frac{V_{bs}}{\varphi_s}} \qquad (1)$$

Define channel depletion layer width in strong inversion mode at $V_{bs}=0$ (2):

$$l_0 = \sqrt{\frac{2 \cdot \varepsilon \cdot \varepsilon_0 \cdot \varphi_s}{e \cdot N_b}} \qquad (2)$$

Define surface potential (3):

$$\varphi_s = 2 \cdot \varphi_b = 2 \cdot \varphi_t \cdot \ln\left(\frac{N_b}{n_i}\right) \qquad (3)$$

Using (3) calculate surface potential:

$$\varphi_s = 2 \cdot 0.0258 \cdot \ln\left(\frac{10^{16}}{1.5 \cdot 10^{10}}\right) \approx 0.7V$$

Using (2) calculate channel depletion layer width at $V_{bs}=0$

$$l_0 = \sqrt{\frac{2 \cdot 1.1 \cdot 10^{-12} \cdot 0.7}{1.6 \cdot 10^{-19} \cdot 10^{16}}} = 3.1 \cdot 10^{-5}\ \text{cm} = 0.31\ \text{um}$$

Using (1) calculate channel depletion layer width at $V_{bs}=-2V$

$$l(-4) = 0.31 \cdot \sqrt{1 - \frac{(-2)}{0.7}} = 0.61\ \text{um}$$

4b99.

W = 4*(a+b)/2 = 2(a+b), L=(b-a)/2

4b100.

$\varphi_0 = \varphi_T \ln(N_A N_D/n_i^2) = 0.026\ V * \ln[(10^{16}\ 10^{20} /(2.1*10^{20})] = 0.94\ V$

$N_D >> N_A$, so

$$x_{dep} = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot \varepsilon_0 \cdot \varphi_0}{e \cdot N_A}} = \sqrt{\frac{2 \cdot 11.7 \cdot 8.85 \cdot 10^{-14}(F/cm) \cdot 0.94(V)}{1.6 \cdot 10^{-19}(C) \cdot 10^{16}(cm^{-3})}} = 0.35\ \text{um}$$

$$C_j(0) = \frac{\varepsilon_{Si} \cdot \varepsilon_0}{x_{dep}} S = \frac{11.7 \cdot 8.85 \cdot 10^{-14}(F/cm)}{0.35 \cdot 10^{-4}(cm)} 1.5 \cdot 1.5 \cdot 10^{-8}(cm^2) = 0.67\ \text{fF}$$

4b101.

One side of the core square

$L_C = \sqrt{49}$ = 7mm.

One side required to place the pads approximately equals

$L_P = (N_P/4)(W_P + S_P)$ = 32*200um = 6.4 mm.

$L_P < L_C$ so the type of this die is core – limited.

4b102.

1. Find induced Q charge of the channel:

$$Q = \Delta n.qabl = 9{,}6 \cdot 10^{-19} \text{ Cl}$$

2. Define gate capacitance:

$$C_1 = Q / V_{g1} \approx 5 \cdot 10^{-19} \text{ F}$$

$$C_2 = Q / V_{g2} \approx 3 \cdot 10^{-19} \text{ F}$$

3. Define cutting voltages for different gate voltages:

$$V_{g01} = qnabl / C_1 \approx 0{,}2\text{V}$$

$$V_{g02} = qnabl / C_2 \approx 0{,}3\text{V}$$

4. Specific electro conductance of the channel is given by the following expression:

$$\sigma = \frac{\mu_n C}{abl} (V_g - V_{g0})$$

Therefore, when the gate voltage changes by 1V, specific electro conductance of the channel will change:

$$\sigma_1 = \frac{\mu_n C_1}{abl} (V_{g1} - V_{g01}) \approx 100 \text{ Ohm}^{-1} \cdot \text{cm}^{-1},$$

$$\sigma_2 = \frac{\mu_n C_2}{abl} (V_{g2} - V_{g02}) \approx 65 \text{ Ohm}^{-1} \cdot \text{cm}^{-1},$$

and

$$\sigma_1 - \sigma_2 = 35 \text{ Ohm}^{-1} \cdot \text{cm}^{-1}.$$

Answer: by 35 $\text{Ohm}^{-1} \cdot \text{cm}^{-1}$.

4b103.

1. Absorption is carried out by $F(x) = F_0 e^{-\alpha x}$ law, where $F(x)$ is beam intensity in x depth, and F_0 - of surface.
   Considering absorption depth to be 1 um, the number of quanta, absorbed from 1 cm^2 surface per second, or the number of generated photo charge carriers will be:

$$F(x) = F_0 \left(1 - e^{-\alpha x}\right) = 0{,}63 \cdot 10^{18} \text{ quantum/cm}^2 \cdot \text{s}$$

2. Photo current density of photo resistance will be defined by the following expression:

$$J = (1 - R)\beta q F_0 \left(1 - e^{-\alpha x}\right) = 0{,}07 \text{ A/ cm}^2$$

Answer: 0,07 A/ cm^2:

4b104.

1. Current density by diode is defined in the following way:

$$J = J_h [\exp(qV / kT) - 1] ,$$

where the saturation current density is:

$$J_h = AT^2 \exp(-q\varphi_b / kT):$$

In case of T=300 K the current density will be:

$$J = AT^2 \exp(-q\varphi_b / kT)[\exp(qV / kT) - 1],$$

As in $[\exp(qV / kT) - 1]$, exponent is much higher than 1, so 1 can be disregarded. So the following will be obtained in the result:

$$J_1 = A300^2 \exp(-q\varphi_b / k300)[\exp(qV / k300)]$$

and

$$J_2 = A350^2 \exp(-q\varphi_b / k350)[\exp(qV / k350)]$$

2. The changing value of current density can be calculated as follows:

$$\frac{J_1}{J_2} = \frac{A300^2 \exp\left(-q\varphi_b / k300\right)\left[\exp\left(qV / k300\right)\right]}{A350^2 \exp\left(-q\varphi_b / k350\right)\left[\exp\left(qV / k350\right)\right]} = 0{,}73\exp\left(-1{,}16\right)\exp\left(1{,}16\right) = 0{,}73:$$

Answer: $\frac{J_1}{J_2} = 0{,}73.$

4b105.

1. First determine the charge capacitance in case of the absence of voltage:

$$C_L = S\left[\frac{\varepsilon\varepsilon_0}{2} q \frac{N_\eta}{\varphi_h}\right]^{1/2} = 11900 \text{ pF}$$

In case of applying 0.2 V reverse voltage, the following is obtained:

$$C_L = S\left[\frac{\varepsilon\varepsilon_0}{2} q \frac{N_\eta}{\varphi_h + 0.2}\right]^{1/2} = 10310 \text{ pF}$$

2. Find the density of the donors, relevant to 1031 pF:

$$N_d = \frac{1}{S^2} \frac{2\varphi_h C_L^2}{\varepsilon\varepsilon_0 q} = 7{,}5 \cdot 10^{14} \text{ cm}^{-3}$$

Answer:

$N_d = 7.5 \cdot 10^{14}$ cm^{-3}:

4b106.

The charge neutrality condition is expressed as $n_0 = p_0 + N_d^+$. If complete ionization is assumed, then $n_0 = p_0 + N_d$. If p_0 is expressed as n_i^2 / n_0, then one obtains $n_0 = n_i^2 / n_0 + N_d$ or $n_0^2 - N_d n_0 - n_i^2 = 0$. Therefore $n_0 = \frac{N_d}{2} + \sqrt{\frac{N_d^2}{4} + n_i^2}$. From this equation the majority carrier electron concentration n_0 and minority carrier hole concentration $p_0 = n_i^2 / n_0$ can be found.

4b107.

Since $N_a > N_d$ the compensated semiconductor is of p-type, thermal-equilibrium carrier concentration is determined by charge neutrality condition: $n_0 + N_a^- = p_0 + N_d^+$. If complete ionization is assumed, then $n_0 + N_a = p_0 + N_d$. If n_0 is expressed as n_i^2 / p_0, then one has $p_0 = \frac{N_a - N_d}{2} + \sqrt{\left(\frac{N_a - N_d}{2}\right)^2 + n_i^2}$.

4b108.

At T=500K the intrinsic carrier concentration n_i is evaluated as $n_i^2 = N_c N_v e^{-E_g / k_B T}$, where $N_c = 2\left(2\pi m_n k_B T / h^2\right)^{3/2}$, $N_v = 2\left(2\pi m_p k_B T / h^2\right)^{3/2}$. For the intrinsic carrier concentration to contribute no more than 10 percent of the total electron concentration, $n_0 = 1{,}1 N_d$ is set. If complete ionization is assumed, then charge neutrality condition is expressed as $n_0 = p_0 + N_d$. If p_0 is expressed as n_i^2 / n_0, then $n_0^2 - N_d n_0 - n_i^2 = 0$ is obtained. Therefore $n_0 = \frac{N_d}{2} + \sqrt{\frac{N_d^2}{4} + n_i^2}$. Solution of equation $1{,}1 \cdot N_d = \frac{N_d}{2} + \sqrt{\left(\frac{N_d}{2}\right)^2 + n_i^2}$ yields N_d.

4b109.

Using the following relations between the direct and reciprocal lattice:

$$\mathbf{b}_1 = 2\pi \frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot \mathbf{a}_2 \times \mathbf{a}_3}, \quad \mathbf{b}_2 = 2\pi \frac{\mathbf{a}_3 \times \mathbf{a}_1}{\mathbf{a}_1 \cdot \mathbf{a}_2 \times \mathbf{a}_3}, \quad \mathbf{b}_3 = 2\pi \frac{\mathbf{a}_1 \times \mathbf{a}_2}{\mathbf{a}_1 \cdot \mathbf{a}_2 \times \mathbf{a}_3}$$

for the reciprocal lattice vectors $\mathbf{b}_1 = 2\pi \frac{\hat{\mathbf{x}}}{5}, \mathbf{b}_2 = 2\pi \frac{\hat{\mathbf{y}}}{2}, \mathbf{b}_3 = 2\pi\hat{\mathbf{z}}$ are obtained. Therefore for the Brillouin first zone volume one has $\Omega_0 = b_1 \cdot b_2 \times b_3 = (2\pi)^3 \frac{1}{5}$ A^{-3}.

4b110.

Resistivity of a semiconductor: $\sigma = en\mu_n + ep\mu_p$ (1)

It is known $n \cdot p = n_i^2$ (n_i intrinsic concentration) $n = \frac{n_i^2}{p}$ put in (1) $\sigma = e\frac{n_i^2}{p}\mu_n + ep\mu_p$ suffix by p and make equal to 0. It will be ext., corresponding to min., as according to 1, there can be no max. value (depending on n and p, σ always increases).

$$\frac{d\sigma}{dp} = -\frac{en_i^2\mu_n}{p^2} + e\mu_p = 0$$

$\frac{n_i^2\mu_n}{p^2} = \mu_p$; $p^2 = n_i^2\frac{\mu_n}{\mu_p}$; $p = n_i\sqrt{\frac{\mu_n}{\mu_p}}$

The same for electrons concentration $p = \frac{n_i^2}{n}$ $\sigma = en\mu_n + \frac{en_i^2\mu_p}{n}$

$\frac{d\sigma}{dn} = e\mu_n - \frac{en_i^2\mu_p}{n^2} = 0$ $\frac{n_i^2\mu_p}{n^2} = \mu_n$ $n^2 = n_i^2\frac{\mu_p}{\mu_n}$ $n = n_i\sqrt{\frac{\mu_p}{\mu_n}}$

Solution: $n = n_i\sqrt{\frac{\mu_p}{\mu_n}}$; $p = n_i\sqrt{\frac{\mu_n}{\mu_p}}$

4b111.

Semiconductor is n type. When Fermi level councides with E_d, temperature levels are low and band to band transitions can be ignored. Free electrons are generated only due to donor ionization.

Therefore $n = N_\eta^+$ (N_η^+ is a number of ionized donors)

Or $n = p_\eta$ ($p_\eta = N_\eta^+$ p_η is a number of attached holes)

Donor level is a discrete level. Thus ion distribution on it is described by $f = \frac{1}{\frac{1}{g}e^{\frac{E_\eta - F}{KT}}}$ distribution function.

(F- energy of Fermi, g-degenerate energy level)

For the case of electron presence on donor level $g = 2$,and $\frac{1}{2}$ for holes. Number of attached holes will be $f \cdot N_\eta$: Thus

$n = f \cdot N_\eta = \frac{N_\eta}{2e^{\frac{E_\eta - F}{KT}}+1}$, when $F = E_\eta$ $n = \frac{N_\eta}{2e^0+1} = \frac{N_\eta}{3}$

Solution:` $n = \frac{N_\eta}{3}$

4b112.

If the quantum output is 1, then in order to emerge 1 electron and hole, 1 photon is absorbed.

Photon energy $\varepsilon = h\nu = \frac{hc}{\lambda}$

The number of emerged electrons will be equal to the number of absorbed photon.

$$n = \frac{E}{\varepsilon} = \frac{E\lambda}{hc} = \frac{10^{-4} \cdot 2 \cdot 10^3 \cdot 10^{-10}}{6{,}62 \cdot 10^{-34} \cdot 3 \cdot 10^{8}} \approx\cdot 0{,}3 \cdot 10^{15}$$

The charge, passing through the circuit, will be:

$Q = en = 1{,}6 \cdot 10^{-19} \cdot 0{,}3 \cdot 10^{15} = 0{,}48 \cdot 10^{-4}$Cl

Answer: $n = 3 \cdot 10^{14}$

$Q = 4{,}8 \cdot 10^{-5}$

4b113.

The velocity of an electron, as a group velocity of a wave, is defined by:

$\vartheta = \frac{1}{\hbar}\frac{dE}{dK}$. Derive the given $E(\vec{K})$

$\vartheta = \frac{E_0 a}{\hbar} \sin K_x a$ (1)

High energy electrons in a conductor are above or below Fermi energy in KT dimension in the range of 2 KT (K-Boltzmann constant, T ^{0}K). Therefore the maximum average energy will be Fermi energy. In that level the maximum velocity of an electron $\vartheta_F$will be obtained from the maximum value of (1), coming from $\sin K_x a = 1$ condition.

$$\vartheta = \vartheta_F = \frac{E_0 a}{\hbar} = \frac{0{,}5 \cdot 1{,}6 \cdot 10^{-19} \cdot 3 \cdot 10^{-10}}{1{,}054 \cdot 10^{-34}} \approx 2{,}3 \cdot 10^5\, {}^{m}/{}_{s}$$

Solution: $\vartheta \approx 2{,}3 \cdot 10^5\, {}^{m}/{}_{s}$

4b114.

$W_1 = W_2 = 40$ watt, number of photons, delivered per second are N_1 and N_2 respectively, and photon energies: E_1 and E_2.

$$W_1 = W_2$$
$$N_1\, E_1 = N_2\, E_2$$
$$N_1\, h\nu_1 = N_2\, h\nu_2$$
$$N_1 \frac{c}{\lambda_1} = N_2 \frac{c}{\lambda_2}$$
$$\frac{N_1}{N_2} = \frac{\lambda_1}{\lambda_2} = \frac{400}{700} = \frac{4}{70} < 1 \Rightarrow N_2 > N_1$$

Solution: second source.

4b115.

Temperature coefficient of ρ resistivity α is determined as $\alpha = \frac{1}{\rho}\frac{d\rho}{dT}$. On the other hand $\rho = \rho_0 e^{E_g/2k_B T}$, where $\rho_0 = \text{const}$. Therefore $\alpha = -\frac{E_g}{2k_B T^2}$. Using relation $E_g = 2\pi\hbar c/\lambda_0$ one obtains $\alpha = -\frac{\pi\hbar c}{\lambda_0 k_B T^2}$.

4b116.

In intrinsic semiconductor $\tau_n = \tau_p \equiv \tau$. Photoconductivity relaxation is described by $\sigma_2 - \sigma_0 = (\sigma_1 - \sigma_0)e^{-\Delta t/\tau}$ law. Using relation $\rho = 1/\sigma$ one obtains $\frac{(\rho_0 - \rho_2)\rho_1}{(\rho_0 - \rho_1)\rho_2} = e^{-\Delta t/\tau}$: Therefore $\tau = \Delta t / \ln \frac{(\rho_0 - \rho_1)\rho_2}{(\rho_0 - \rho_2)\rho_1}$.

4b117.

From problem conditions it follows that

$$\begin{cases} np = n_i^2 \\ n + N_a = p \end{cases}$$

Therefore $p^2 - pN_a - n_i^2 = 0$ and $p = -\frac{N_a}{2} + \sqrt{\frac{N_a^2}{4} + n_i^2}$ or $p = n_i(\sqrt{2} - 1)$. Using relation $\rho = 1/\sigma$, one has $\frac{\rho}{\rho_i} = \frac{n_i\mu_n + p_i\mu_p}{p\mu_p} = \frac{n_i(b+1)}{p} = \frac{(b+1)}{\sqrt{2} - 1}$.

4b118.

The work function A is determined as $A = U_0 - F$, where F is the Fermi energy, U_0 is the potential energy of the free electron. Fermi energy in a metal is determined by electron concentration n as $F = \hbar^2(3\pi^2 n)^{2/3}/2m_0$. Electron concentration is determined as $n = N_A\rho/\mu$, where N_A is the Avogadro number, ρ is the mass density, μ is the molar mass. Therefore for the potential energy of free electron, one has $U_0 = A + \hbar^2(3\pi^2 N_A \rho/\mu)^{2/3}/2m_0$.

4b119.

Photon energy E_f = hc / λ and for visible light it is between E_f = 1,8-3,31 eV. Since the energy of Si and GaAs bandgap is smaller than the energy of visible light phonon, then visible light phonons will be fully absorbed by those semiconductors which means that they are not transparent. Since GaP bandgap energy is in the range of visible light spectrum, it is transparent only for one part of the spectrum and is considered to be translucent. Since GaN bandgap energy is larger than the energy of the entire spectrum of visible light, it does not absorb light phonons and is completely transparent to visible light.

4b120.
p-n junction corrective properties cease to occur when the number of electrons and the number of holes are equal. This happens when N_d(N_a)≈n_i=$\sqrt{N_c N_v}$exp(-E_a/2kT)~$T^{3/2}$exp(-E_a/2kT). From here and the given parameters it can be found that the maximum temperature is T_{Ge}≈400K, T_{Si}≈650K and T_{GaN}≈1700K.

4b121.
Consider emitter junction. It is known that the width of depletion domain of junction can be calculated by the following expression:

$\mathrm{l} = \mathrm{l}_0\sqrt{\frac{\Delta\varphi_0 - V}{\Delta\varphi_0}}$ where $\mathrm{l}_0 = \sqrt{\frac{2\varepsilon_0\varepsilon\Delta\varphi_0}{q}\left(\frac{1}{N_d} + \frac{1}{N_a}\right)}$, and $\Delta\varphi_0 = \frac{kT}{q}\ln\frac{n_{n0}}{n_{p0}}$ or $\Delta\varphi_0 = \frac{kT}{q}\ln\frac{p_{p0}}{p_{n0}}$

As voltage is not applied to emitter junction and $N_d \gg N_a$, in this case emitter junction width can be calculated by the following expression: $\mathrm{l}_0 = \sqrt{\frac{2\varepsilon_0\varepsilon\Delta\varphi_0}{q}\frac{1}{N_a}}$, contact potential difference can be found by the following expression $\Delta\varphi_0 = \frac{kT}{q}\ln\frac{n_{n0}}{n_{p0}}$. n_{p0} can be calculated by the following expression p_{p0}*n_{p0} = n_i^2. Putting corresponding values in the given expressions, l_0= 0,098um will be obtained for depletion domain of emitter junction. Since doping level of emitter domain is much greater than the one of base, the depletion domain is mainly in the base.
Now consider the collector domain. As it is reverse biased, the width of depletion domain will be given by the following expression: $\mathrm{l} = \mathrm{l}_0\sqrt{\frac{\Delta\varphi_0 + V}{\Delta\varphi_0}}$, where $\mathrm{l}_0 = \sqrt{\frac{2\varepsilon_0\varepsilon\Delta\varphi_0}{q}\left(\frac{1}{N_d} + \frac{1}{N_a}\right)}$ and $\Delta\varphi_0 = \frac{kT}{q}\ln\frac{p_{p0}}{p_{n0}}$. Here p_{n0} can be found from p_{n0}*p_{p0}= n_i^2 expression. The width of depletion domain of junction consists of two parts: l_{b0} and l_{c0}, which have the following dependence $\frac{l_{b0}}{l_{c0}} = \frac{N_d}{N_a}$, and in its turn $\mathrm{l}_0 = \mathrm{l}_{b0} + \mathrm{l}_{c0}$. Thus, calculating l_0 value, the value of l_{b0} can be found which equals 0,034um. In this case the total base width can be presented as: $w = \mathrm{l}_{eb0} + \mathrm{l}_{cb0}\sqrt{\frac{\Delta\varphi_0 + V}{\Delta\varphi_0}} = 0{,}5\mathrm{um}$. Making respective calculations for the maximum value of bias voltage of collector junction, ≈13,7 V is obtained.

4b122.
The open circuit voltage of a photodiode can be found by the following expression: $0 = I_0\left(\exp\left(\frac{qV_{oc}}{kT}\right) - 1\right) - I_l$ hence $V_{oc} \approx \frac{kT}{q}\ln\left(\frac{I_l}{I_0}\right)$, where $I_0 = qS\left(\frac{L_p p_n}{\tau_p} + \frac{L_n n_p}{\tau_n}\right)$, and $L_p = \sqrt{D_p\tau_p}$ and $L_n = \sqrt{D_n\tau_n}$. The concentration of minority charge carriers can be defined by: $p_n = \frac{n_i^2}{N_d}$ and $n_p = \frac{n_i^2}{a}$. Putting the parameters in the given expression, I_0=2*10^{-12}A and V_{oc}= 0,61V are obtained. The operating voltage of maximum power can be found from dP/dV=0 expression where the operating power is $P = I_L V - I_0 V\left(\exp\left(\frac{qV}{kT}\right) - 1\right)$.

Hence $V_{max} \approx V_{oc} - \frac{kT}{q}\ln\left(1+\frac{qV_{max}}{kT}\right)$, making the corresponding numerical operations, V_{max}=0,53V is obtained. Putting the value of this voltage in the expression of power above, P_{max}=48mWt is obtained.

4b123.

The voltage, applied to capacitance, is distributed on isolator (V_i) and semiconductor (ψ_s). V= V_i+ ψ_s. Voltage on isolator is equal to $V_i = \frac{Q_s}{C_i}$ where $C_i = \frac{\varepsilon_i}{4\pi d}$, and Q_s is the charge, accumulated on semiconductor, ε_i is the dielectric constant of isolator, and d – isolator thickness. When the voltage drop on semiconductor is small for its conductivity type to be sharply inverse, accumulated charge will be defined by: $|Q_s| = qN_a w_d = qN_a\left(\frac{\varepsilon_s\psi_s}{2\pi q N_a}\right)^{1/2}$, where ε_s - dielectric permittivity of semiconductor, w_d – depletion domain width. Hence $V = \psi_s + \frac{2d}{\varepsilon_i}\sqrt{2\pi q\varepsilon_s N_a\psi_s}$.

In order to make the semiconductor surface intrinsic, it is needed that ψ_s potential is $\psi_s = \psi_{fp} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$.

a. Thus, using $V = \psi_s + \frac{2d}{\varepsilon_i}\sqrt{2\pi q\varepsilon_s N_a\psi_s}$ expression and putting corresponding parameter values, the necessary voltage value will be obtained, equal to 1,24V

b. it is known that sharp inversion of semiconductor surface occurs when $\psi_s = 2\psi_{fp}$. Doing corresponding calculations, necessary voltage will be equal to 2V.

4b124.

Reflection exclusion condition is the equality of two wave resistances $z_{01} = z_{02}$, hence $\frac{120}{\sqrt{\varepsilon}}\frac{h}{w} = \frac{256}{\sqrt{\varepsilon}}\log\frac{2D}{d}$. As $D/_d = 5d$, then 120 $h/_w$ = 276, hence $h/_w = 2{,}3$.

4b125.

Differentiating the expression, $dI_d = I_0 e^{U_d/\varphi_T}\frac{1}{\varphi_T}dU_d$ will be obtained. Hence

$$\frac{dU_d}{dI_d} = R_d = \frac{\varphi_T}{I_0 e^{U_d/\varphi_T}} = \frac{\varphi_T}{I_d}.$$

4b126.

Currents of emitter I_e, collector I_c and base I_b of a transistor are related as follows:

$I_e = I_c + I_b$, where $I_c = \beta I_b$.

Therefore $I_e = (\beta+1)I_b$. As $I_e = \frac{U_e}{200}$, $I_F = \frac{5-(U_e+0{,}75)}{1000}$, where U_e is the emitter voltage, putting these expressions and the value of β in the previous formula, this will be obtained:

$$\frac{U_e}{200} = 25\cdot\frac{5-(U_e+0{,}75)}{1000} = \frac{4{,}25-U_e}{40},$$

hence $U_e = 3{,}54$V. Base voltage U_b=U_e+0,75=3,54+0,75=4,29V.

As $U_c = 5 - I_c\cdot 50 = 5-\beta I_b\cdot 50$, and $I_b = \frac{5-U_b}{1000} = \frac{5-4{,}29}{1000} = \frac{0{,}71}{1000}$=0,71$\cdot 10^{-3}$A, then $U_c = 5 - 24\cdot 0{,}71\cdot 40\cdot 10^{-3} = 4{,}32$V.

4b127.

Resistive film is a hollow cylinder, which if cut by the generating line and spread it, will become a rectangular film with length ℓ, width πD and thickness d.

As $d \ll D$, then the resistance of this film will be $R = \frac{\rho\ell}{\pi Dd} = \frac{12\cdot 10^{-3}\text{Ohm}\cdot\text{m}\ 15\cdot 10^{-3}\text{m}}{6{,}3\cdot 10^{-3}\text{m}\cdot 5\cdot 10^{-6}\text{m}} \approx 5714\text{Ohm}$, and the dependence of R from ℓ is linear, therefore 10% variations of ℓ will lead to the same 10% variations of R.

4b128.

In material mechanics, the motion equation is:

$$m\frac{dv}{dt} = F.$$

Instead of moving electrons in the crystal, it should be written effective m^* mass:

$m^* = \frac{\hbar^2}{\frac{d^2E}{dK^2}}$.

$$\frac{\hbar^2}{\frac{d^2E}{dK^2}} \cdot \frac{dv}{dt} = F \Bigg| \rightarrow \frac{dv}{dt} = \frac{F}{\hbar^2} \cdot \frac{d^2E}{dK^2}$$

$$\frac{dE}{d\vec{K}} = 2\alpha_x k_x + 2\alpha_y k_y + 2\alpha_z k_z$$

$$\frac{d^2E}{dK^2} = 2(\alpha_x + \alpha_y + \alpha_z)$$

Answer: $\frac{\mathrm{dv}}{\mathrm{dt}} = \frac{2\mathrm{F}}{\hbar^2}(\alpha_x + \alpha_y + \alpha_z)$

4b129.

Under the terms of the problem, the issue is about $E_1 = F + \delta$ and $E_2 = F - \delta$ levels. The probability that the electron is on E_1 level will be $f(E_1) = \frac{1}{e^{\frac{F+\delta-F}{KT}}+1}$, and the probability that on E_2 level –

$f(E_2) = \frac{1}{e^{\frac{F-\delta-F}{KT}}+1}$, i.e.

$f(E_1) = \frac{1}{e^{\frac{\delta}{KT}}+1}$, multiply the numerator and the denominator of the first one by $e^{-\frac{\delta}{KT}}$.

$f(E_2) = \frac{1}{e^{-\frac{\delta}{KT}}+1}$ This will be obtained:

$$f(\delta) = \frac{e^{-\frac{\delta}{KT}}+1-1}{1+e^{-\frac{\delta}{KT}}} = 1 - \frac{1}{1+e^{-\frac{\delta}{KT}}} = 1 - f(-\delta)$$

Answer:

$$f(-\delta) = 1 - f(-\delta)$$

4b130.

Einstein's equations for the photoelectric effect is:

$$h\nu = A_{out} + \frac{mv^2}{2}$$

For the red line: $\frac{mv^2}{2} = 0$

$$h\nu = \frac{hc}{\lambda_0}, \lambda_0 = \frac{hc}{A_{out}}, A_{out} = \frac{hc}{\lambda_0} \Bigg| \lambda_{0_W} = \frac{6{,}62 \cdot 10^{-34} \cdot 3 \cdot 10^8}{4{,}17 \cdot 1{,}6 \cdot 10^{-19}} \approx 3 \cdot 10^{-7} m,$$

$$\lambda_{0_{Cz}} = \frac{6{,}62 \cdot 10^{-34} \cdot 3 \cdot 10^8}{1{,}81 \cdot 1{,}6 \cdot 10^{-19}} \approx 7 \cdot 10^{-7} \mathrm{m}$$

Answer: $\lambda_{0_W} < \lambda_{0_{Cz}}$

4b131.

The relation of mobility of charge carriers and the diffusion coefficient is given in respect of Einstein: $D = \frac{KT}{e}\mu$

$D_n = \frac{1{,}38 \cdot 10^{-23} \cdot 300}{1{,}6 \cdot 10^{-19}} \cdot 0{,}16 = 41{,}4 \cdot 10^{-2}$ m^2/ sec

$D_p = \frac{1{,}38 \cdot 10^{-23} \cdot 300}{1{,}6 \cdot 10^{-19}} \cdot 0{,}04 = 10{,}3 \cdot 10^{-2}$ m^2/sec.

4b132.

Abrupt PN junction capacitance defined as:

$C = S\sqrt{\frac{e\varepsilon N_a N_d}{2(\Phi_0 + V)(N_a + N_d)}} \equiv \frac{K}{\sqrt{(\Phi_0 + V)}}$. Therefore,

$\begin{cases} C_{max} = \frac{K}{\sqrt{\Phi_0 - V_a}} \\ C_0 = \frac{K}{\sqrt{\Phi_0}} \end{cases}$. Solving this system of equations, the magnitudes Φ_0 and K can be determined. For the minimal capacitance of the junction one has: $C_{min} = \frac{K}{\sqrt{(\Phi_0 + V_a)}}$. The problem answers are: $\Phi_0 \approx 0.67$ V, $C_{min} = 0.76$ pF.

4b133.

The condition of the wave reflection from the atomic planes is determined by Wulf-Bragg formula $2d\sin\theta = n\lambda$. Using relation $d = a/\sqrt{h^2+k^2+l^2}$ for the distance between atomic planes, one obtains: $\sin\theta = \frac{n\lambda}{2a}\sqrt{h^2+k^2+l^2}$. From $\sin\theta\big|_{\max} = 1$ and $n = 1$ conditions follows: $\left(h^2+k^2+l^2\right)_{\max} = \frac{4a^2}{\lambda^2} = 10.2$.

Therefore,

$(hkl) = (100),(110),(111),(200),(210),(211),(220),(300),(310)$ and the number of lines is equal to 9.

4b134.

The external photoelectrical effect cutoff wavelength is determined by electron work function: $\hbar c/\lambda_1 = A$. The photoconductivity cutoff wavelength is determined by semiconductor bandgap: $\hbar c/\lambda_1 = E_g$. Therefore $E_c = \hbar c/\lambda_1 - \hbar c/2\lambda_2 = 1.65$ eV because Fermi energy located on $E_g/2$. Location of E_c comparatively to vacuum, where $E = 0$, equals -0.65 eV.

4b135.

In direct current mode, diode's current expression is $I=I_0\exp(eV/kT)$. At V=0,15V

$I=15\times10^{-6}\exp(1{,}6\times10^{-19}\ 0{,}15/1{,}38\times10^{-23}\ 300)=15\times10^{-6}\exp(5{,}8)=15\times10^{-6}330{,}3=4{,}95\times10^{-3}$ A.

The static resistance of the diode $R_0=V/I=0{,}15/4{,}95\times10^{-3}=30{,}3$ Ohm.

The differential resistance expression of the diode $R_d = 1/(dI/dV) = 1/\ I_0\exp(eV/kT)\ e/\ kT = (kT/eI)$.

$R_d = (kT/e\ I) = 1{,}38\times10^{-23}\ 300/(1{,}6\times10^{-19}\times\ 4{,}95\times10^{-3}) = 5{,}23$ Ohm.

Ans. R_0 =30,3 Ohm and Rd =5,23 Ohm.

4b136.

$C_o= a/(V_0+\varphi_{cont})^{1/2}$, when V_0= 0V, and $C_1= a/(V_1+\varphi_{cont})^{1/2}$, when V_0=10V:

The value of constant a is determined from the initial condition:

$250\times10^{-12} = a/\sqrt{1+0{,}81} = a/\sqrt{1{,}81}$ and $a=3{,}36\times10^{-10}$ F $V^{1/2}$.

Then $C_0=3{,}36\times10^{-10}/0{,}9$ = 373 pF and $C_1=3{,}36\times10^{-10}/3{,}29$ =100 pF.

Answer: C_0=373 pF , C_1= 100 pF, ΔC =273 pF.

4b137.

a) In direct current mode $I_1=I_0\exp(eV_1/kT)$ and $I_2=I_0\exp(eV_2/kT)$.

Then $I_2/I_1 = I_0\exp(eV_2/kT)/\ I_0\exp(eV_1/kT) = 5$ or $V_2-V_1 = (kT/e)\ln 5$:

$V_2-V_1 = 0{,}026\times1{,}6=4{,}18\times10^{-2}$ V. So, the voltage has to be increased by 0,0418V.

b) $I_2=I_0\exp(eV_2/kT) = 100I_o$ then $V_2= (kT/e)\ln 100$:

$V_2 = 0{,}026\times 4{,}6=0{,}119$V.

Answer: a) 0,0418V, b) V_2 =0,119 V.

5. SEMICONDUCTOR TECHNOLOGY

a) Test questions

5a1. E
5a2. D
5a3. D
5a4. D
5a5. B
5a6. C
5a7. B
5a8. B
5a9. B
5a10. A
5a11. B
5a12. B
5a13. C
5a14. A
5a15. B
5a16. D
5a17. C
5a18. D
5a19. C
5a20. C
5a21. B
5a22. C
5a23. B
5a24. C
5a25. B
5a26. A
5a27. E
5a28. D
5a30. C
5a31. A
5a32. A
5a33. C
5a34. A
5a35. B
5a36. D
5a37. B
5a38. C
5a39. A
5a40. A
5a41. E
5a42. C
5a43. C
5a44. A
5a45. A
5a46. A
5a47. C
5a48. E
5a49. B
5a50. C
5a51. B
5a52. C
5a53. B
5a54. D
5a55. D
5a56. B
5a57. B
5a58. B
5a59. B
5a60. E
5a61. E
5a62. E
5a63. C
5a64. B
5a65. B
5a66. B
5a67. B
5a68. E
5a69. B
5a70. E
5a71. B
5a72. B
5a73. C
5a74. C
5a75. D
5a76. D
5a77. D
5a78. A
5a79. B

b) Problems

5b1.
$\rho_p=10^{-4}$ Ohm·m
$\rho_n=10^{-2}$ Ohm·m
$\mu_p=0,05\ m^2 V^{-1} s^{-1}$
$\mu_n=0,13\ m^2 V^{-1} s^{-1}$
$n_i=1,38x10^{16}\ m^{-3}$
T=300K
φ_c =?
The contact potential is obtained from φ_c= (kT/q)lnp_p/p_n=0,0258 lnp_p/p_n
The densities of holes and electrons are obtained using the specific resistance expressions:

$$P_P = \frac{1}{\rho_P q \mu_P} = \frac{1}{10^{-4} \cdot 1,6 \cdot 10^{-19} \cdot 0,05} = 1,25 \cdot 10^{24}\ \text{m}^{-3}$$

$$n_n = \frac{1}{\rho_n q \mu_n} = \frac{1}{10^{-2} \cdot 1,6 \cdot 10^{-19} \cdot 0,13} = 4,2 \cdot 10^{21}\ \text{m}^{-3}$$

The holes' density in n region is obtained using the mass action law:

$$P_n = \frac{n_i^2}{n_n} = \frac{2 \cdot 10^{32}}{4,2 \cdot 10^{21}} = 4,8 \cdot 10^{10}\ \text{m}^{-3}$$

The contact potential of p–n junction

φ_c=0,0258 lnp_p/p_n=ln$1,25x10^{24}/4,8x10^{10}$=0,8V.

5b2.
σ_p=100 S/cm
$\mu_p=1900\ cm^2 V^{-1} s^{-1}$
T=300 K
$n_i=2,5x10^{13}$ atom/cm^3
p_p , n_p=?
Using the expression of the specific conductance
$\sigma_p=1/q\mu_p p_p$, the holes' density

$$p_p = \frac{\sigma_p}{q\mu_p} = \frac{100}{1,6 \cdot 10^{-19} \cdot 1900} = 3,29 \cdot 10^{17}\ \text{cm}^{-3}$$

The concentration of electrons is obtained using the mass action law:

$n_p\ p_p= n_i^2$.

$$n_p = \frac{n_i^{\ 2}}{p_p} = \frac{6,25 \cdot 10^{26}}{3,29 \cdot 10^{17}} = 1,9 \cdot 10^9\ \ \text{cm}^{-3}$$

5b3.
$N_d= 10^{17}$atom/cm^3
L=100 μm
W=10 μm
d=1 μm
$\mu_n= 1500\ cm^2 V^{-1} s^{-1}$
T=300K
R and ρ_s= ?
Assuming that the impurities are fully ionized, the electrons concentration n =N_d
The specific resistance

ρ_n =1/σ =1/qnμ_n, ρ_n=1/1,6x10^{-19}x10^{17}x1500= 0,042 Ohm· cm

The resistance

R=ρ_n L/ W·d =0,042 x100·10^{-4} /10x10^{-4}x1x10^{-4}=4,2 kOhm.

The sheet resistance

ρ_s=ρ_n/ d = 0,042/1x10^{-4}= 420 Ohm/mm.

5b4.
C_{0x}=100 nF/cm^2=100x10^{-9} F/cm^2
ε_{SiO2}=3,9x8,85x10^{-14} F/cm
t_{ox}= ?
Calculate the thickness of SiO_2 layer by the intrinsic formula of MOS-capacitor's permittivity.

$C_{0x}= \varepsilon_{SiO2}/ t_{ox}$ and $t_{ox}= \varepsilon_{SiO2}/ C_{0x}$

$$t_{ox}=3{,}9x8{,}85x10^{-14}/100x10^{-9}$$
$$t_{ox}=3{,}45x10^{-6}\ cm=0{,}0345\ um.$$

To grow the high quality gate oxide, the dry oxidation process will be used.

5b5.

The gate capacitance is defined as

$$C = C_{ox}S = (\varepsilon_0\varepsilon_{ox}/t_{ox})WL$$

After the scaling by the α factor

$$C_{sc} = (\varepsilon_0\varepsilon_{ox}/t_{ox}/\alpha)\,(W/\alpha)L/\alpha\,) = (\varepsilon_0\varepsilon_{ox}/t_{ox})WL/\ \alpha = C/\alpha\ .$$

For α =2, $C_{sc}=C/2$.

The capacitance will decrease by factor two.

5b6.

For direct voltage, the current density:

when $T=T_1$ $j_1 \to \exp\left(-\frac{E_g - qV}{kT_1}\right) = \exp\left(-\frac{0.7-0.4\cdot 1.6\cdot 10^{-19}}{0.022}\right) = 1.2*10^{-6}$ A/cm^2.

when $T=T_2$ $j_2 \to \exp\left(-\frac{E_g - qV}{kT_2}\right) = \exp\left(-\frac{0.7-0.4\cdot 1.6\cdot 10^{-19}}{0.026}\right) = 9.7*10^{-6}$ A/cm^2.

therefore $\frac{j_2}{j_1}$ =8.08.

5b7.

Near the drain, the width of p-n junction when the voltage applied to drain is V = 0.1V

$$d_1=\left(\frac{2\varepsilon\varepsilon_0}{q}\cdot\frac{\varphi_{\ddot{I}}+V}{N_1}\right)^{1/2} =\left(\frac{2\cdot 12\cdot 8.86\cdot 10^{-14}}{1.6\cdot 10^{-19}}\cdot\frac{0.6+0.1}{10^{15}}\right)^{1/2}=9.64\cdot 10^{-5}\ cm$$

and in case of voltage absence: $d_2=\left(\frac{2\varepsilon\varepsilon_0}{q}\cdot\frac{\varphi_{\ddot{I}}}{N_1}\right)^{1/2}$ $=8.93\cdot 10^{-5}$cm

therefore, near the drain, the channel will narrow by d_1-d_2=$0.71\cdot 10^{-5}$cm.

5b8.

Saturation voltage of the transistor

$$V_{DSsat.} = V_{GS} - V_t = 3-1= 2V.$$
$$V_{DS} > V_{DS\ sat}$$

therefore the transistor operates in saturation mode. In this mode the drain current of the transistor equals:

$$I_D = 0{,}5\ \mu_n\ Cox\ (W/L)\ (V_{GS}- V_t)^2.$$

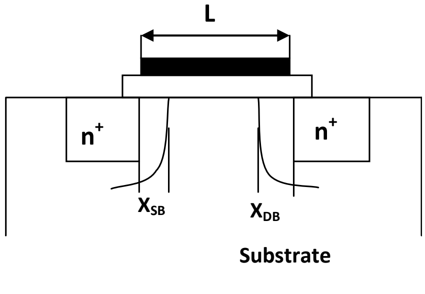
Calculate

$$Cox = (\varepsilon_0\ \varepsilon_{si\,o2})/\ t_{ox} =(3{,}9x8{,}85x10^{-14})/10x10^{-7}= 3{,}45x10^{-7}\ F/cm^2.$$
$$I_D = 0{,}5x300x3{,}45x10^{-7}(3-1)^2x\ (10/1)=2{,}07\ mA.$$

Transconductance g_m=d I_D/d V_{GS}

$$g_m= \mu_n\ Cox\ (W/L)\ (V_{GS}- V_t) =300x3{,}45x10^{-7}x10\ x2= 2\ mA$$

5b9.



$$L_{sum}= L- X_{SB}\ (V_S) - X_{DB}\ (V_D)$$

By data, L_{eff} =0, hence

$$X_{DB}\ (V_D) = L- X_{SB}\ (V_S)$$

Use the width formula of depletion region:

$$2\varepsilon_0\,\varepsilon_{Si}\,(\varphi_c - V_D)/q\,N_{sub} = (L - X_{SB}(0))^2$$
$$V_D = \varphi_c - q\,N_{sub}(L - X_{SB}(0))^2/\,2\varepsilon_0\,\varepsilon_{Si}$$

Calculate

$$\varphi_c = \varphi_T \ln N_{sub} N_{don}/\,n_i^2$$

In a room temperature

$$\varphi_T \approx 0{,}026\ \text{V and } \varphi_c \approx 0{,}935\ \text{V.}$$
$$X_{SB}(0) = \sqrt{}\ 2\varepsilon_0\,\varepsilon_{Si}\,\varphi_c / q\,N_{sub}$$
$$X_{SB}(0) = \sqrt{}2\text{x } 8{,}85\text{x}10\text{-}14\text{x}11{,}8\text{x}0{,}935/1{,}6\text{x}10^{-19}\text{x}10^{16}$$
$$X_{SB}(0) \approx 0{,}349\text{x}10^{-4}\ \text{cm.}$$

Put and calculate

$$|V_D| \approx 2{,}3\ \text{V.}$$

5b10.
Density of electronic current

$$J_n = eD_n\, dN/dx$$

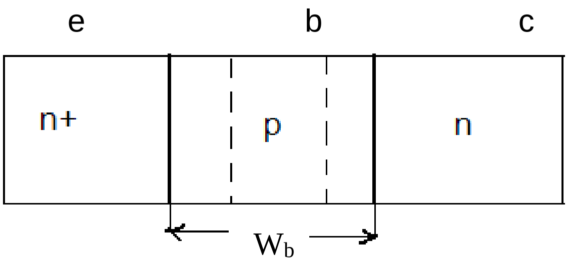
According to Einstein formula:

$$D_n = \varphi_T\ \mu_n,\ \text{ and }\ dN/dx = k$$
$$J_n = e\ \varphi_T\ \mu_n\ k$$

In a room temperature

$$\varphi_T = 0{,}026\ \text{V}$$
$$J_n = 1{,}6\ 10^{-19}\ \text{x}\ 0{,}026\ \text{x}1200\ \text{x}\ 8\ \text{x}\ 10^{18} = 39{,}936\ \text{A/cm}^2.$$

5b11.



a. Calculate the difference of contact potentials in E-B and C-B p-n junctions. At a room temperature

$$\varphi_T \approx 0{,}026\ \text{V}$$
$$\varphi_{ce} = \varphi_T \ln N_e\,N_b/\,n_i^2 \qquad \varphi_{ce} = 0{,}026\ \ln 10^{19}\text{x}10^{15}/2{,}25\text{x}10^{20} \approx 0{,}8759\ \text{V}$$
$$\varphi_{cc} = \varphi_T \ln N_b N_c/\,n_i^2 \qquad \varphi_{cc} = 0{,}026\ \ln 10^{16}\text{x}5\text{x}10^{15}/2{,}25\text{x}10^{20} \approx 0{,}7\ \text{V}$$

b. Calculate E-B depletion layer width when the external voltage =0.

$$X_{eb}(0) = \sqrt{}\ 2\varepsilon_0\,\varepsilon_{Si}\,\varphi_{ce} / q\,N_b \approx 3{,}38\text{x}10^{-5}\text{cm} = 0{,}338\ \text{um.}$$

c. For base punch-through, X_{cb} depletion layer width must be

$$X_{cb} = 0{,}6 - 0{,}338 = 0{,}262\ \text{um.}$$

d. The voltage of the collector can be obtained from the following equation:

$$X_{cb} = \sqrt{}\ 2\varepsilon_0\,\varepsilon_{Si}\,N_c\,(\varphi_{cc} - V) / q\,N_b\,(N_b + N_c).$$

Hence

$$V = \varphi_{cc} - X^2_{cb}\,q\,N_b\,(N_b + N_c)/2\varepsilon_0\,\varepsilon_{Si}\,N_c \quad \text{and} \quad |V| \approx 0{,}8765\ \text{V}$$

5b12.
As $N_d > N_{acc}$, so silicon has an n – type conductivity. The active concentration of the impurities is $N_{act} = N_{don} - N_{acc} = 9\text{x}10^{16}\ \text{cm}^{-3}$. At room temperature T= 300 K all impurity atoms are ionized, $N_{act} \approx N_{don} = n$.

The specific conductivity of the sample at room temperature

$$\sigma_n = e\ n\ \mu_n$$
$$\sigma_n = 1{,}6\text{x}10^{-19}\ \text{C x } 9\text{x}10^{16}\ \text{cm}^{-3}\ \text{ x } 1400\ \text{cm}^2/\text{V}\cdot\text{s}$$
$$\sigma_n = 20{,}16\ (\text{Ohm}\cdot\text{cm})^{-1}.$$

5b13.
The time delay in the n^+ polysilicon interconnect line t=RC. The interconnect line resistance $R = \rho_\square\ l/b$: $R = 200\text{x}1\text{x}10^3/1 = 200$kOhm.

The interconnect line capacitance to the substrate $C = C_o S$, $C = 60\text{x}10^3\text{x}1 = 60000$ aF. The time delay $t = 200\text{x}10^3\text{x}60000\text{x}10^{-18} = 12$ ns.

5b14.
The time delay in the metal interconnect line t=RC. The resistance of the metal 1 interconnect line $R=\rho_{\square}\, l/b$

$$R=0{,}1x1x10^3/0{,}2 = 500\ \text{Ohm}$$

The capacitance of the line to the substrate $C= C_0\, S$.

$$C=23 \times 10^3 \times 0{,}2=4600\ \text{aF}.$$

The time delay $t= RC = 500x4600x10^{-18}= 2{,}3$ ps.

5b15.
The p-n junction barrier layer capacitance $C=(\varepsilon_0\varepsilon_{Si}/x_{p\text{-}n})S_{p\text{-}n}$, where $x_{p\text{-}n}$ is the depletion width of the p-n junction. For the one-sided p-n junction $x_{p\text{-}n}$ is defined as

$x_{p\text{-}n} \approx x_n= \sqrt{2\varepsilon_0\varepsilon_{Si}(\varphi_k -U)/e N_d}$

$x_{p\text{-}n}=\sqrt{2x\ 8{,}85x10^{-14}x11{,}8x(0{,}7-0)/1{,}6x10^{-19}x10^{16}} =3x10^{-5}$ cm, when U=0V.

$x_{p\text{-}n}=\sqrt{2x8{,}85x10^{-14}x11{,}8x(0{,}7+5)/1{,}6x10^{-19}x10^{16}}=8{,}6x10^{-5}$ cm, when U= -5V.

The barrier layer capacitance

$C_0=(\varepsilon_0\varepsilon_{Si}/x_{p\text{-}n})S_{p\text{-}n}= (8{,}85x10^{-14}x11{,}8/3x10^{-5})\ x10^{-5}=34{,}8x10^{-14}$ F=0,348 pF.

$C_5=(\varepsilon_0\varepsilon_{Si}/x_{p\text{-}n})S_{p\text{-}n}= (8{,}85x10^{-14}x11{,}8/\ 8{,}6x10^{-5})\ x10^{-5}=12{,}14x10^{-14}$ F=0,12 pF.

5b16.
The time delay of the interconnect line

$$\tau = RC$$

The resistance of the interconnect line $R=\rho_{sq}\,(l/\ w)$

$$R=500(50/0{,}5)=50000\ \text{ohm}.$$

The capacity of the interconnect line to the substrate

$$C=\varepsilon_0\varepsilon_{ox}(l\cdot w/t_{ox})$$

$C=8{,}85\cdot 10^{-12}\cdot 3{,}9\cdot 50\cdot 10^{-6}\cdot 0{,}5\cdot 10^{-6}/0{,}2\cdot 10^{-6}=4{,}3\cdot 10^{-15}$ F

$$\tau = RC=50000\cdot 4{,}3\cdot 10^{-15}=0{,}21\ \text{ns}.$$

5b17.
Power consumption $P = I\cdot U$
The current and voltage are scaled by α factor. Thus,

$$P_{scale} = (I/\alpha)\cdot(U/\alpha)= P/\alpha^2$$

The power density $P_{den} = (I\cdot U)/(l\cdot w)= P/(l\cdot w)$

$P_{scale} =(P/\alpha^2)/(l/\alpha\cdot w/\alpha)= P/(l\cdot w)$, so the power density does not change.

Time delay $\tau = RC_G$ or $\tau = C_G\, V_D / I_D$, where C_G is the gate capacitance, and V_D / I_D is the effective resistance of the gate capacitance.

For the scaled device $\tau' = (\frac{C_G}{\alpha}\frac{V_D}{\alpha})\frac{\alpha}{I_D} = \frac{\tau}{\alpha}$.

Time delay of the gate is reduced by α factor.

The switching energy $P\cdot\tau$

$$P\cdot\tau_{scale} = (\frac{P}{\alpha^2}\frac{\tau}{\alpha}) = \frac{P\tau}{\alpha^3}:$$

The switching energy is reduced by α^3 times.

5b18.
The temperature dependence of semiconductor resistor is expressed by

$$R= R_0(1+\alpha(t-t_0)).$$

So, $R_1= R_0(1+\alpha(t_1-t_0))$ and $R_2= R_0(1+\alpha(t_2-t_0))$

$$\Delta R = R_2 - R_1 = R_0\alpha(t_2 - t_1)$$

Calculate the $R_0 = \rho_{sq}$ (l/ w)= $300(5\cdot 10^{-5}/2{,}5\cdot 10^{-6})$=6000 ohm.

$\Delta R = 6000\cdot 0{,}0024\cdot 100 = 1440$ ohm.

5b19.

The resistance of emitter n^+ region is $R=\rho_{sq}(l/b)$:

$\rho_{sq} = \rho/h$, and $\rho = 1/\sigma$, we obtain $\rho_{sq} = 1/\sigma\cdot h$.

Calculate the σ specific conductivity

$\sigma = e\cdot n\cdot \mu_n$ and $n = N_{don}$

$\sigma = 1{,}6\cdot 10^{-19}\cdot 10^{25}\cdot 0{,}14 = 2{,}24\cdot 10^5$ 1/ohm·m

$\rho_{sq} = 1/\sigma\cdot h = 1/2{,}24\cdot 10^5\cdot 10^{-7} = 44{,}6$ ohm·m:

$R = \rho_{sq}(l/b) = 44{,}6\cdot(10^{-5}/5\cdot 10^{-7}) = 892$ ohm.

5b20.

The diffusion current density of electrons equals:

$J_n = eD_n dn/dx \approx eD_n \Delta n/\Delta x$. At room temperature $n \approx N_d$.

The diffusion coefficient D_n is obtained from the Einstein relation:

$$D_n = (kT/e)\mu_n = \varphi_t\,\mu_n$$

$$D_n = 0{,}026\cdot 1200 = 31{,}2\ cm^2/s$$

The concentration gradient $\Delta n/\Delta x = (10^{18} - 5\cdot 10^{17})/3\cdot 10^{-4} \approx 1{,}66\cdot 10^{21}\ cm^{-4}$.

$$J_n = 1{,}6\cdot 10^{-19}\cdot 31{,}2\cdot 1{,}66\cdot 10^{21} = 8{,}286\cdot 10^3\ A/cm^2$$

5b21.

The resolution R and focus depth F of the optical system are expressed by:

$R = K_1\lambda/NA$ and $F = K_2\lambda/(NA)^2$ respectively.

$R = 0{,}3\text{x}193/0{,}65 = 89$ nm, $F = 0{,}5\text{x}193/(0{,}65)^2 = 228{,}4$ nm.

To improve the resolution of the optical system, immersion lithography technology is used. Immersion lithography is an optical technique of improvement that increases the effective aperture NA of the optical system. The aperture NA=n x sinα, where n is a refractive index of a fluid (such as water) between the final lens and the wafer surface. The resolution is increased by a factor equal to the refractive index of the liquid. It is possible to increase resolution while simultaneously maintaining practical depths of focus. Current immersion lithography tools use highly purified water for this liquid, achieving feature sizes below 45 nanometers.

5b22.

As $(V_{GS} - V_t) = V_{DS\,sat} < V_{DS}$, there are saturation mode and MOS transistor current:

$$I_{DS} = 0{,}5\mu C_{ox}(W/L)(V_{GS} - V_t)^2$$

Calculate $C_{ox} = \varepsilon_o\varepsilon_{ox}/t_{ox}$

$C_{ox} = 8{,}85\text{x}10^{-12}\text{x}3{,}9/15\text{x}10^{-9} = 2{,}3\text{x}10^{-3}\ F/m^2$

$I_{DS} = 0{,}5\text{x } 500\text{ x}10^{-4}\text{x}2{,}3\text{x}10^{-3}\ (5/0{,}3)\ (1{,}5 - 0{,}7)^2 = 613{,}3$ mkA.

The differential resistance R of a MOS transistor may be obtained as:

R=dV/dI= 1/dI/dV,

$$R = 1/\mu C_{ox}(W/L)(V_{GS} - V_t)$$

$R = 1/500\text{ x}10^{-4}\text{x}2{,}3\text{x}10^{-3}\ (5/0{,}3)(1{,}5 - 0{,}7) = 652$ Ohm.

5b23.

The temperature dependence of a semiconductor resistor is expressed by:

$$R = R_0(1+\alpha(t - t_0)).$$

At room temperature $t_1 = t_0$, and $R_1 = R_0(1+\alpha(t_1 - t_0)) = R_0$.

$R_2 = R_0(1+\alpha(t_2 - t_0))$ at t_2 temperature.

$R_2 = R_1 + 0{,}5\,R_1 = 1{,}5\,R_1$.

So, $R_0(1+\alpha(t_2 - t_0)) = R_0$, and $t_2 = 0{,}5/\alpha + t_0 = 178{,}5^oC$.

5b24.

The specific conductivity σ of the semiconductor is defined by the following expression:

$$\sigma = q(n\,\mu_n + p\,\mu_p).$$

In addition, the electrons and holes concentrations are connected by the $np = n_i^2$ expression. For the specific conductivity, this is obtained:

$$\sigma/q = n\mu_n + p\mu_p \quad \text{or} \quad \sigma/q = n\mu_n + n_i^2\mu_{p/}\, n$$

This expression has a minimal value when

$$d(\sigma/q)/dn = 0$$

Then $\mu_n - n_i^2\mu_p/n^2 = 0$ and $n = n_i(\mu_p/\mu_n)^{0,5}$.

5b25.

Diode’s current at U=0,1V direct voltage is:

$$I = I_0\exp(qU/kT) = 20\text{x}10^{-6}\exp(1{,}6\text{x}10^{-19}\text{x}0{,}1/1{,}38\text{x}10^{-23}\text{x}300) = 0{,}936 \text{ mA}.$$

Diode’s R_o resistance towards the constant current is:

$$R_o = U/I = 0{,}1/0{,}936\text{x}10^{-3} = 106{,}8 \text{ Ohm}.$$

Differential resistance is:

$$r_d^{-1} = dI/dU = I_0\exp(qU/kT)\text{x } q/kT = q\,I/kT \quad \text{and} \quad r_d = kT/q\,I$$

$$r_d = 1{,}38\text{x}10^{-23}\text{x}300/1{,}6\text{x}10^{-19}\text{x}0{,}936\text{x}10^{-3} = 27{,}5 \text{ Ohm}.$$

5b26.

The flight time $t = l / V_d = l/\mu_nE = l^2/\mu_nU$. The electrons mobility μ_n can be found using specific resistance expression $\rho=1/q\mu_nn$. Then for the flight time:

$$t = l^2 q\rho n/U = 1\text{x}10^{-4}\text{x}1{,}6\text{x}10^{-19}\text{x}10\text{x}10^{-2}\text{x}10^{21}/5$$

$$t = 3{,}2\text{x}10^{-4} \text{ s}.$$

5b27.

The differential resistance R of the transistor’s channel is R=dV/dI= 1/ dI/dV.

$$R_1 = 1/\mu C_{ox}(W/L)(V_{GS1} - V_t) \quad \text{and} \quad R_2 = 1/\mu C_{ox}(W/L)(V_{GS2} - V_t).$$

Then $R_2 = 1{,}5\, R_1$, and $R_2/R_1 = (V_{GS1} - V_t)/(V_{GS2} - V_t) = 1{,}5$

$(1{,}0 - 0{,}3)/(V_{GS2} - 0{,}3) = 1{,}5$ and $V_{GS2} = 0{,}77$ V:

So, voltage V_{GS1} applied to the MOS transistor’s gate must be decreased by 0,23 V.

5b28.

1) First define the nominal value of M_1 and M_2 metal fragments’ overlapping area:
$S_{nom} = (x_{2nom} - x_{1nom})\text{x}(y_{2nom} - y_{1nom}) = (12-10)\text{x}(13-8) = 10 \text{ um}^2$
2) The nominal value of capacitance, corresponding to S_{nom} area will be:
$C_{nom} = 10\text{x}0{,}2 = 2{,}0$ fF
3) The absolute deviations of x_2 and y_2 values will be 0,4 and 0,6 um respectively. So maximum and minimum values of S area will be:
$S_{max} = (12-10+0{,}1+0{,}4)\text{x}(13-8+0{,}1+0{,}6) = 14{,}25 \text{ um}^2$
$S_{min} = (12-10-0{,}1-0{,}4)\text{x}(13-8-0{,}1-0{,}6) = 6{,}45 \text{ um}^2$
4) Values of capacitances, corresponding to S_{max} and S_{min} area will be:
$C_{max} = 14{,}25\text{x}0{,}2 = 2{,}85$ fF
$C_{min} = 6{,}45\text{x}0{,}2 = 1{,}29$ fF
Answer: $C = 2^{+0{,}85}_{-0{,}71}$ fF

5b29.

The resistance of a rectangular resistor is $R = \rho_\square(l/b)$. Then

$$l/b = R/\rho_\square = 1\text{x}10^4/2\text{ x}10^3 = 5 \quad \text{and} \quad l = 5\,b.$$

The resistor area is $S = l\text{x}b = 5b^2$ and power density is

$$P_o = P/S = P/5b^2 \le 1\text{W/mm}^2.$$

Therefore $0{,}5\text{x}10^{-3}/5b^2 \le 1\text{W/mm}^2$ and $b \ge 10^{-2}$ mm or 10 mkm.
Accept b = 10 mkm and l =5x10 =50 mkm.
Solution: length is 50 mkm and width is 10 mkm

5b30.

The resistance of diffusion rectangular resistor is $R=\rho_{\square}$ (l/ b). Then

$$l/b = R/\rho_{\square} = 5x10^3/400=12,5 \text{ and } l=12,5\, b.$$

The resistor area is $S= lxb = 12,5b^2$ and power density is

$$P_o=P/S = P/12,5b^2 \leq 1W/mm^2.$$

Therefore $1x10^{-3}/12,5b^2 \leq 1W/mm^2$ and $b \geq 8,94x10^{-3}$ mm or 8,94 mkm.

Accept b = 9 mkm and l =9x12,5 =112,5 mkm.

Solution: length is 112,5 mkm and width is 9 mkm.

6. NUMERICAL METHODS AND OPTIMIZATION

a) Test questions

6a1. E
6a2. D
6a3. D
6a4. B
6a5. B
6a6. A
6a7. A
6a8. B
6a9. A
6a10. A
6a11. A
6a12. C
6a13. C
6a14. D
6a15. C
6a16. A
6a17. D
6a18. D
6a19. B
6a20. B
6a21. B
6a22. A
6a23. A
6a24. D
6a25. C
6a26. E
6a27. D
6a28. C
6a29. C
6a30. B
6a31. D
6a32. D
6a33. E
6a34. A
6a35. A
6a36. D
6a37. B
6a38. D
6a39. C
6a40. D
6a41. B
6a42. D
6a43. B
6a44. D
6a45. A
6a46. A
6a47. A
6a48. C
6a49. D
6a50. A
6a51. B
6a52. C
6a53. D
6a54. B
6a55. B
6a56. A
6a57. B
6a58. C
6a59. D
6a60. A
6a61. B
6a62. C
6a63. B
6a64. D
6a65. A
6a66. E
6a67. C
6a68. C
6a69. B
6a70. C
6a71. C
6a72. C
6a73. B
6a74. D
6a75. D
6a76. D
6a77. B
6a78. A
6a79. B
6a80. B
6a81. A
6a82. C
6a83. D
6a84. E
6a85. A
6a86. B
6a87. E
6a88. D
6a89. A
6a90. C
6a91. E
6a92. B
6a93. A
6a94. E
6a95. A
6a96. B
6a97. B
6a98. D
6a99. C
6a100. A
6a101. C
6a102. B
6a103. A
6a104. E
6a105. D
6a106. C
6a107. B
6a108. D
6a109. B
6a110. A
6a111. E
6a112. D
6a113. C
6a114. B
6a115. B
6a116. C
6a117. A
6a118. B
6a119. A
6a120. A
6a121. C
6a122. B
6a123. A
6a124. B
6a125. A
6a126. C
6a127. B
6a128. C
6a129. C
6a130. A
6a131. B
6a132. B
6a133. C
6a134. C
6a135. D
6a136. A
6a137. A
6a138. C
6a139. A
6a140. A
6a141. C
6a142. C
6a143. A
6a144. A
6a145. B
6a146. C
6a147. B
6a148. A
6a149. D
6a150. C
6a151. E

b) Problems

6b1.
Define low and upper values of the game and their corresponding optimal strategies. There is:

$$\alpha = \max_i \min_j h_{ij}, \ \alpha=2,\ i=3,\ j=1;$$

$$\beta = \max_j \min_i h_{ij}, \ \beta=3,\ i=1,\ j=1:$$

As $\alpha \neq \beta$, i.e. there is mixed strategy matrix game in case of which vector elements of $P=(p_1,p_2,p_3)^T$ probabilities are the probabilities of selecting A side corresponding strategy. $Q=(q_1,q_2,q_3)^T$ vector elements are the ones of selecting B side corresponding strategy.

$$\alpha \le V \le \beta,$$

$$\begin{cases} 3p_1 - p_2 + 2p_3 \ge V, \\ -2p_1 + 4p_2 + 2p_3 \ge V, \\ 4p_1 + 2p_2 + 6p_3 \ge V, \\ p_1 + p_2 + p_3 = 1, \end{cases} \quad \begin{cases} 3q_1 - 2q_2 + 4q_3 \le V, \\ -q_1 + 4q_2 + 2q_3 \le V, \\ 2q_1 + 2q_2 + 6q_3 \le V, \\ q_1 + q_2 + q_3 = 1, \end{cases}$$

In the result of solving the system the following is obtained:

$p_1=0$, $p_2=0$, $p_3=1$;
$q_1=2/5$, $q_2=3/5$, $q_3=0$;
$V=2$.

6b2.
Define $\Phi(t, t_0)$ by matrix method.
There is:

$$M(A(t))_{3x3} = E_{3x3} + Q^1(A(t))_{3x3} =$$

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} \int_2^1 t dt & \int_2^1 t^2 dt & \int_2^1 t^3 dt \\ \int_2^1 1 dt & \int_2^1 t dt & \int_2^1 (2-t) dt \\ \int_2^1 t^2 dt & \int_2^1 t dt & \int_2^1 t dt \end{bmatrix} = \begin{bmatrix} \left(\frac{t^2}{2} - 1\right) & \left(\frac{t^3}{3} - \frac{8}{3}\right) & \left(\frac{t^4}{4} - 4\right) \\ (t-1) & \left(\frac{t^2}{2} - 1\right) & \left(2t - \frac{t^2}{2} - 2\right) \\ \left(\frac{t^3}{3} - \frac{8}{3}\right) & \left(\frac{t^2}{2} - 2\right) & (t-1) \end{bmatrix} = \Phi(t, t_0).$$

6b3.
There is

$$H = \begin{bmatrix} 0 & 0.4472 & 0.4851 \\ 0 & 0 & 0.4851 \\ 1 & 0.8944 & 0.7276 \end{bmatrix},$$

The opposite of which

$$H^{-1} = \begin{bmatrix} -2 & 0.5 & 1 \\ 2.2361 & -2.2361 & 0 \\ 0 & 2.0616 & 0 \end{bmatrix}.$$

Therefore

$$\Phi(t) = H \cdot diag\left(e^{-\lambda_i}\right) \cdot H^{-1} = \begin{bmatrix} e^{-2t} & \left(-e^{-2t} + e^{-3t}\right) & 0 \\ 0 & e^{-3t} & 0 \\ 2\left(e^{-2t} - e^{-t}\right) & \left(\frac{1}{2}e^{-t} 2e^{-2t} + \frac{3}{2}e^{-3t}\right) & e^t \end{bmatrix}.$$

6b4.
There is

$$\lambda_1=4.4142,\ \lambda_2=1.5858,\ \lambda_3=0;$$

$$H = \begin{bmatrix} -0.3366 & -0.5615 & -0.2182 \\ -0.4760 & 0.7941 & -0.8729 \\ -0.8125 & 0.2326 & 0.4364 \end{bmatrix}, \ H^{-1} = \begin{bmatrix} -0.6731 & -0.2380 & -0.8125 \\ -1.1230 & 0.3971 & 0.2326 \\ -0.6547 & -0.6547 & 0.6547 \end{bmatrix}.$$

Therefore

$$diag(A) = H \cdot A \cdot H^{-1} = \begin{bmatrix} 4.4142 & 0 & 0 \\ 0 & 1.5858 & 0 \\ 0 & 0 & 0 \end{bmatrix}.$$

6b5.
As the constant term of characteristic polynomial (P3) is equal to the determinant of matrix, therefore it will be

$$P_3 = det\begin{bmatrix} 1 & -2 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix} = 1\cdot1\cdot1 + 2\cdot2 = 5.$$

6b6.
As

$$\|A\|_2 = \left(\sum_{i=1}^{3}\sum_{j=1}^{3} a_{ij}^2\right)^{1/2}$$

then

$$\|A\|_2 = \sqrt{1^2 + (-2)^2 + 1^2 + 2^2 + (-1)^2 + 1^2} = \sqrt{12}$$

6b7.

As coefficient of characteristic polynomial term containing λ^2 is $P_1 = -\sum_{i=1}^{3} \lambda_i$,

$$P_1 = -(1+2+3) = -6:$$

6b8.
As characteristic polynomial coefficient of the term which contains λ^2

$$P_1 = \sum_{i,j=1}^{4} \lambda_i \cdot \lambda_j \ ,$$

then

$$P_2 = \lambda_1\lambda_2 + \lambda_1\lambda_3 + \lambda_1\lambda_4 + \lambda_2\lambda_3 + \lambda_2\lambda_4 + \lambda_3\lambda_4 = 0\cdot1 + 0\cdot2 + 0\cdot3 + 1\cdot2 + 1\cdot3 + 2\cdot3 = 11.$$

6b9.
It is known that linear interpolation error is defined by the following formula:

$$R_2 = \frac{1}{8} M_2 h^2 \ ,$$

where h is the length of the step, $M_2 = \max_{x\in[0,1000]} | f''(x)|$. As $f(x) = log\ x$, then $M_2 = 1$. Therefore, in order to provide the necessary accuracy, h should be taken $\sqrt{0.008} \approx 0.089$.

Taking into consideration that $f''(x) = -x^{-2}$, i.e. for large x-es the derivative is small, then dividing the range into parts, it is possible to enlarge the division step. For example, divide $[0,1000]$ range into $[0,10],[10,100],[100,1000]$ ranges. In that case, h_1 division step in the 1st range equals 0.089 (as $M_{2,1} = \max_{x\in[0,10]} | f''(x)| = M_2 = 1$). In the 2nd range $M_{2,2} = 0.01$, therefore, h_2 step is defined from $\frac{1}{8}\cdot 0.01 \cdot h_2^2 < 0.001$ non-equation, i.e. $h_2 = 0.894$. Similarly, in the 3rd range $M_{2,3} = 0.0001$, and the step equals $h_3 = 8.94$. Thus, in order to provide the anticipated accuracy it is necessary to take approximately 100 points in each part. Other types of divisions of initial range can also be observed. The minimum number of points can be obtained by changing length of the next range in each step, i.e. in k th step h_k is selected by the following formula: $8^{-1} | x_k |^{-2} h_k^2 < 0.001$, $x_{k+1} = x_k + h_k$.

6b10.

The formula of generalized trapeziums, applied for the given integral, is $\frac{h}{2}\left(\frac{1}{b^2}+\frac{e}{1+b^2}+2\sum_{i=1}^{n-1}\frac{e^{x_i}}{x_i^2+b^2}\right)$.
In the given case the error is defined by inaccuracy formula of generalized trapeziums' formula $\frac{M_2}{12}(1-0)h^2$, where $h=x_{i+1}-x_i$ - $[0,1]$ is interval division step. Noticing $M_2=O(b^{-4})$, it is seen that the given formula does not operate in case of small b-s. Therefore, for $O(h^2)$ class provision it is necessary to divide $[0,1]$ part into subparts and to use smaller division step in 0 range. For example, by dividing $[0,1]$ into two subparts - $[0,l]$ and $[l,1]$, h_1 division step in the first range should be selected in a way that $h_1 \approx hb^2$, and in the second range $h_2 \approx h(l^2+b^2)$. Other forms of division can also be discussed.

6b11.

As $\frac{f(x)}{\sqrt{x}}$ function has uniqueness in 0 point, it is not possible to apply squarization formula at once. For that reason divide $[0,1]$ part into $[0,10^{-8}]$ and $[10^{-8},1]$ ranges. The integral with the first range allows $\left|\int_0^{10^{-8}}\frac{f(x)}{\sqrt{x}}dx\right| = |f(c)|\cdot 2\sqrt{10^{-8}} \approx C\cdot 10^{-4}$ mark ($0<c<10^{-8}$). This mark allows ignoring the first integral and calculating only the integral with the second range, where the integrating function has no uniqueness and therefore, squarization formula is possible to apply. But as $\sqrt{x}$ accepts small values in that range, it is desirable to improve the integrating function in advance by using integration in parts of $\int_{10^{-8}}^{1}\frac{f(x)}{\sqrt{x}}dx = \int_{10^{-8}}^{1} f(x)d2\sqrt{x} = 2f(1)-2f(10^{-8})10^{-4} - \int_{10^{-8}}^{1} 2\sqrt{x}f'(x)dx$. For the final integral, the formula of generalized rectangular can be applied, the error of which is estimated by $M_1\frac{h}{4}(1-10^{-8})$ formula where $M_1 \le m_1\cdot 10^2$ ($m_1 = \max_{x\in[0,1]}|f'(x)|$). In the last inequality $|f''(x)|\le 1$ condition has been used. Eventually, $h\approx 10^{-6}$.

6b12.

Notice that $x^3-20x+1=0$ equation is solved which has three $z_1<z_2<z_3$ real roots. Write the formula of iteration process in the following view $x_{n+1}-x_n=\frac{x_n^3-20x_n+1}{20}$. From this it follows that in $x_0<z_1$ or $x_0>z_3$ case, the method diverges (the difference in the left part is monotonous); $x_0=z_1$ and $x_0=z_3$ points are static; in $z_1<x_0<z_3$ case the method converges z_2.

6b13.

The constants α and β cannot be found uniquely, because the term 'smallest error' is not defined in the formulation of problem. First, it must be defined exactly what 'the smallest error' means. For example, the distance between functions f and g can be defined as $\|f-g\| = \max_{x\in[-10,10]}|f(x)+g(x)|$ (uniform norm). In this case the best approximating linear function will be $y=2.5$ (it follows from Chebyshev theorem). On the other hand, the function $y=\frac{arctg\,100}{20}\approx\frac{\pi}{40}$ gives the best approximation, when the distance between functions f and g is defined as $\|f-g\|_2 = \sqrt{\int_{-10}^{10}|f(x)-g(x)|^2dx}$ (root-mean-square norm). Also the weighting norms $\|f-g\|_{2,p}=\sqrt{\int\limits_{-10}^{10}|f(x)-g(x)|^2 p(x)dx}$ may be considered where the weighting function p is a fixed positive function. In this case the coefficients α,β will depend on p.

6b14.

The integration interval is not bounded; therefore, the multiple-application rectangle rule cannot be applied immediately. Assume the function f on interval $[1,\infty)$ is bounded by the constant C: $|f(x)|\le C$. The integral can be represented as:

$$\int\limits_1^\infty \frac{f(x)dx}{1+x^2}=\int\limits_1^{1.5C\varepsilon^{-1}}\frac{f(x)dx}{1+x^2}+\int\limits_{1.5C\varepsilon^{-1}}^{3C\varepsilon^{-1}}\frac{f(x)dx}{1+x^2}+\int\limits_{3C\varepsilon^{-1}}^{\infty}\frac{f(x)dx}{1+x^2}\equiv I_1+I_2+I_3$$

The estimate of the function f implies inequalities $|I_2|<\frac{\varepsilon}{3}$ and $|I_3|<\frac{\varepsilon}{3}$. Applying multiple-application rectangle rule for the first integral, this is obtained:

$$I_1\approx\tilde{I}_1=h\sum_{k=1}^{N}\frac{f(x_k)}{1+x_k^2},\ \text{where } N=\frac{1.5C}{h\varepsilon}.$$

The reminder term of this formula is the following:

$$R_1=\frac{M_1(1.5C-\varepsilon)h}{2\varepsilon},\ \text{where } M_1=\max_{x\ge 1}\left|\left(\frac{f(x)}{1+x^2}\right)'\right|$$

Hence for $h=\frac{4\varepsilon^2}{9CM_1}$ the necessary accuracy is obtained:

$$\left|\int\limits_1^\infty\frac{f(x)dx}{1+x^2}-\tilde{I}_1\right|<\varepsilon.$$

Notice that the obtained step h is too small, so in this case non-equidistant intervals can be used. The rectangle rule for non-equidistant intervals takes this form:

$$\tilde{I}_2=\sum_{k=1}^{N}\frac{f(x_k)}{1+x_k^2}(x_{k+1}-x_k),$$

with the reminder term

$$R_1=\sum_{k-1}^{N}\frac{M_k(x_{k+1}-x_k)^2}{2}$$

Taking into account that

$$M_k=\max_{x\in[x_k,x_{k+1}]}\left|\left(\frac{f(x)}{1+x^2}\right)'\right|\le\frac{M}{x_k^2}+\frac{C}{x_k^4},\ \text{where } M=\max_{x\ge1}|f'(x)|,$$

this is obtained

$$R_1\le\frac{M_0}{2}\sum_{k=1}^{N}\frac{1}{x_k^2}(x_{k+1}-x_k)^2,\ \text{where } M_0=max(M,C).$$

Thus, taking the partition points x_k such that $R_1<\frac{\varepsilon}{3}$, the final formula is obtained.

6b15.

The polynomial P_3 is represented as $P_3(x)=(a_0+a_1(x-x_1))(x-x_2)^2+(a_2+a_3(x-x_2))(x-x_1)^2\equiv P_{3,1}(x)+P_{3,2}(x)$. The advantage of this representation is the following. For the function $P_{3,k}$ there is $P_{3,k}(x_j)=P'_{3,k}(x_j)=0$ where $j\ne k$, $j,k=1,2$. Using the conditions $P_3^{(k)}(x_1)=P_{3,1}^{(k)}(x_1)=f^{(k)}(x_1)$, where $k=0,1$, $a_0=\frac{f(x_1)}{(x_2-x_1)^2}$,

$a_1 = \frac{f'(x_1)}{(x_1 - x_2)^2} - \frac{2f(x_1)}{(x_1 - x_2)^3}$ is obtained. The same formulas exist for a_2 and a_3. Finally, the polynomial P_3 is presented as follows:

$$P_3(x) = \left(f(x_1) + \left(f_1'(x_1) - \frac{2f(x_1)}{x_1 - x_2} \right)(x - x_1) \right) \frac{(x - x_2)^2}{(x_1 - x_2)^2}. +$$

$$+ \left(f(x_2) + \left(f_2'(x_2) - \frac{2f(x_2)}{x_2 - x_1} \right)(x - x_2) \right) \frac{(x - x_1)^2}{(x_2 - x_1)^2}$$

Using the same considerations the needed formula can be obtained for arbitrary number of the points x_k.

6b16.

There are many ways to solve this problem. For example, using successive approximations $x_{k+1} = \frac{x_k^4 + 1}{10}$, $x_0 = 0$, the root of the equation on the interval $[0,1]$ with prescribed accuracy can be found after four steps. If the bisection method on the same interval is used, seven steps will be necessary.

6b17.

Substituting $t = x - 1$, the problem is reduced to the equivalent problem of definition of quadratic function $G(t) = a_1 t^2 + b_1 t + c_1$, which gives the best approximation for the function

$$F(t) = \frac{1}{2+t} + \frac{1}{2-t}$$

in $[-1,1]$ interval. Taking into account, that F function is even in symmetric interval, and defining distance between two functions as $D_1 = \max_{[-1,1]} |F(t) - G(t)|$, or $D_2 = \int_{-1}^{1} (F(t) - G(t))^2 dt$, $b_1 = 0$ is obtained. Consider, for example, D_1 distance case. It is represented as:

$$D_1 = \max_{[-1,1]} |F(t) - G(t)| = \max_{t \in [-1,1]} \left| \frac{4}{4 - t^2} - a_1 t^2 - c_1 \right| = \max_{z \in [0,1]} \left| \frac{4}{4 - z} - a_1 z - c_1 \right|.$$

As the function $\frac{4}{4 - z}$ is convex in $[0,1]$ interval and denoting $L = \min_{a_1, c_1} D_1$, the system for the definition of the best approximation polynomial of first order is obtained.

$$\begin{cases} \frac{4}{4-0} - c_1 = L \\ \frac{4}{4-1} - a_1 - c_1 = L \\ \frac{4}{(4 - z_0)^2} - a_1 = 0 \\ \frac{4}{4 - z_0} - a_1 z_0 - c_1 = -L \end{cases}$$

Here $0, z_0, 1$ points are Chebyshev's alternance points. Solving that system this is obtained:

$$a_1 = \frac{1}{3}, \quad c_1 = \frac{4\sqrt{3} - 1}{6}, \quad L = \frac{7 - 4\sqrt{3}}{6}.$$

So, the best approximation polynomial will be $y = \frac{1}{3}(x-1)^2 + \frac{4\sqrt{3} - 1}{6}$, with minimal distance $L = min D_1 = \frac{7 - 4\sqrt{3}}{6} \approx 0.012$.

The case of distance D_2 is easier. Also, one can consider the case of weighted approximation, when $D_\rho = \int_{-1}^{1} (F(t) - G(t))^2 \rho(t) dt$, where ρ is the given positive function.

6b18.

Calculating Δ_n, $\Delta_{n+1} = 2\Delta_n - \Delta_{n-1}$ recurrent formula for $n > 1$ is obtained. Solving it, $\Delta_n = C_1 + C_2 n$ is obtained, where C_1 and C_2 are unknown constants. As $\Delta_1 = 2$ and $\Delta_2 = 3$, $\Delta_n = n + 1$. So, $\lim_{n\to\infty} \frac{\Delta_n}{n} = 1$ is obtained.

6b19.

One of possible ways. Assume the equation of AB line is $l(x, y) \equiv ax + by + c = 0$. This line splits the plane into two half-planes: $\{(x, y) : l(x, y) > 0\}$ and $\{(x, y) : l(x, y) < 0\}$. If the point D lies in triangle's interior, then substituting the coordinates of that and C point into $l(x, y)$, values of the same sign will be obtained (i.e. D and C belong to the same half-plane). The same considerations can be done for BC and AC lines. An arbitrary polygon case can be reduced to triangle case by partitioning and checking if D point lies in one of partition triangles.

6b20.

The polynomial P_4 is represented as:

$$P_4 = (x - x_2)\left(a_0 + a_1(x - x_1) + a_2(x - x_1)^2 + a_3(x - x_1)^3\right) + (x - x_1)^4 b_0 .$$

Substituting that polynomial into the given equalities, the system for determination of unknown a_k and b_0 is obtained:

$$(x_2 - x_1)^4 b_0 = y_4, \quad \begin{cases} (x_1 - x_2)a_0 = y_0 \\ a_0 + (x_1 - x_2)a_1 = y_1 \\ 2a_1 + 2(x_1 - x_2)a_2 = y_2 \\ 6a_2 + 6(x_1 - x_2)a_3 = y_3 \end{cases} .$$

The general case may be considered analogously.

6b21.

As characteristic polynomial's absolute term (P3) equals to determinant of matrix, then it will be

$$P_3 = det\begin{bmatrix} 1 & -3 & 0 \\ 0 & 1 & 2 \\ -1 & 0 & 1 \end{bmatrix} = 1\cdot 1\cdot 1 + 3\cdot 2 = 7 .$$

6b22.

As

$$\|A\|_2 = \left(\sum_{i=1}^{3}\sum_{j=1}^{3} a_{ij}^2\right)^{1/2} = \sqrt{1^2 + (-3)^2 + 1^2 + 2^2 + (-1)^2 + 1^2} = \sqrt{17} .$$

6b23.

As the coefficient of first degree of λ in the characteristic polynomial $P_1 = \sum_{i=1}^{3} \lambda_i$, then $P_1 = 1 + 4 + 2 = 7$:

6b24.

A As the coefficient of first degree of λ^2 in the characteristic polynomial $P_1 = \sum_{i,j=1}^{4} \lambda_i \cdot \lambda_j$, then

$$P_2 = \lambda_1\lambda_2 + \lambda_1\lambda_3 + \lambda_1\lambda_4 + \lambda_2\lambda_3 + \lambda_2\lambda_4 + \lambda_3\lambda_4 = 4\cdot 1 + 4\cdot 2 + 4\cdot 3 + 1\cdot 2 + 1\cdot 3 + 2\cdot 3 = 35$$

6b25.

There are five linearly independent conditions for determination of the P_n polynomial coefficients.

Therefore, the minimal value of n for which the problem has a solution for arbitrary values y_j and z_k cannot be less than four. Forth order polynomial which satisfies given conditions, can be found explicitly, similar to Lagrange interpolation polynomial. First, find basic polynomials Φ_j and Ψ_k, satisfying conditions:

$$\Phi_j^{(i)}(1) = \delta_{ij},\ i = 0,1,2, \quad \Phi_j^{(q)}(0) = 0,\ q = 0,1, \quad \text{for } j = 0,1,2$$
$$\Psi_k^{(i)}(1) = 0,\ i = 0,1,2, \quad \Psi_k^{(q)}(0) = \delta_{kq},\ q = 0,1 \quad \text{for } k = 0,1.$$

Here δ_{ij} is a Kronecker symbol ($\delta_{ij} = 0$ for $i \neq j$ and $\delta_{ii} = 1$). After that, the required polynomial is found by the formula

$$P_4(x) = \sum_{j=0}^{2} y_j \Phi_j(x) + z_0 \Psi_0(x) + z_1 \Psi_1(x).$$

Show how to construct basic polynomials. Consider, for example, Φ_1.
Search this polynomial in the form

$$\Phi_1(x) = x^2(x-1)(a(x-1)+b).$$

Then the constants a, b will be determined from the conditions $\Phi_1'(1) = 1,\ \Phi_1''(1) = 0$, or $b = 1,\ 2a + 4b = 0$, from which $a = -2,\ b = 1$. The remaining basic polynomials can be found analogously.

The polynomials P_4 can be found also directly, by writing it down as: $P_4(x) = x^2\left(a(x-1)^2 + b(x-1) + c\right) + (x-1)^3(dx+e)$, and determining coefficients a, b, c, d, e from problem conditions by constants y_j and z_k.

6b26.

As the function $f(x) = x^3$ is odd, and an interval $[-1,1]$ is symmetric relative to origin, then the required polynomial has to be an odd function, too. Hence, $P_1(x) = ax$, where the constant a must be determined. For the determination of this constant, consider the function $g(x) = f(x) - P_1(x) = x^3 - ax$ on the interval $[0,1]$. There is $g(0) = 0$ and $g(1) = 1 - a$. The function g is convex, therefore a can be found from the condition, that the minimal value of function g at some point x_0 of open interval $(0,1)$ is equal to $g(1) = 1 - a$ with opposite sign. Then in the interval $[-1,1]$ four points ($z_1 = -1, z_2 = -x_0, z_3 = x_0, z_4 = 1$) are obtained, where $f(z_k) - P_1(z_k) = (-1)^k \|f - P_1\|$, so, by the Chebyshev theorem, the polynomial $P_1 = ax$ will be the required polynomial of best approximation. So:

$g'(x) = 3x^2 - a$, from which $x_0 = \sqrt{\frac{a}{3}}$. Further, $g\left(\sqrt{\frac{a}{3}}\right) = -\frac{2}{3}a\sqrt{\frac{a}{3}}$, and therefore the constant a can be found from equation $1 - a = \frac{2}{3}a\sqrt{\frac{a}{3}}$. Solving this equation, $a = \frac{3}{4}$ is obtained. Finally, the polynomial of best approximation is $P_1(x) = \frac{3}{4}x$. This problem can be solved easier, using geometric considerations.

6b27.

Assume λ is eigenvalue of A matrix. In that case $\det(A - \lambda E) = 0$ (E is unit matrix). If A matrix satisfies $A^n = 0$ condition, where n is a natural number, then there is

$-\lambda^n E = A^n - \lambda^n E = (A - \lambda E)\left(A^{n-1} + \lambda A^{n-2} + \lambda^2 A^{n-3} + \ldots + \lambda^{n-1} E\right),$

therefore, using the properties of determinants
$-\lambda^n=\det\left(-\lambda^{n-1}E\right)=\det(A-\lambda E)\det\left(A^{n-1}+\lambda A^{n-2}+\lambda^2A^{n-3}+\ldots+\lambda^{n-1}E\right)=0$
i.e. $\lambda=0$. Thus if $A^n=0$, where n is a natural number, the eigenvalue of A matrix equals zero.

6b28.
Substituting 1 in the expansion of the logarithm function alternating series $\ln 2=\sum_{k=1}^{\infty}(-1)^{k+1}\frac{1}{k}$ is obtained which converges very slowly as, according to Leibniz theorem, $|\ln 2-S_N|\le\frac{1}{N+1}$, where S_N is a partial sum of the given series. Therefore, to provide the necessary accuracy it is necessary to take not less than 1000 terms of the series which leads to significant increase of round-off error. Therefore it is better to apply the following method. Define t number from equation $\frac{1+t}{1-t}=2$. $t=\frac{1}{3}$ is obtained hence, the seeking number is presented as:

$$ln2=ln\left(1+\frac{1}{3}\right)-ln\left(1-\frac{1}{3}\right)=\sum_{k=0}^{\infty}\left((-1)^{k+1}+1\right)\frac{1}{k3^k}$$

This series in the right part may be estimated by geometrical progression with $\frac{1}{3}$ denominator. Therefore in order to provide the necessary accuracy it is enough to take only 8 summands of the given series. The same method may be applied again. Other methods are also possible.

6b29.
As the absolute term (P_3) of characteristic polynomial equals to determinant of matrix, then it will be

$$P_3=det\begin{bmatrix}2&-6&0\\0&2&4\\-2&0&2\end{bmatrix}=2\cdot2\cdot2+(-6)\cdot(-2)\cdot4=56:$$

6b30.

As the coefficient of λ^2 in the characteristic polynomial is equal to $P_2=\sum_{\substack{i,j=1\\i\neq j}}^{4}\lambda_i\cdot\lambda_j$, then

$$\begin{aligned}P_2&=\lambda_1\lambda_2+\lambda_1\lambda_3+\lambda_1\lambda_4+\lambda_2\lambda_3+\lambda_2\lambda_4+\lambda_3\lambda_4=\\&=2\cdot0.5+2\cdot1+2\cdot1.5+0.5\cdot1+0.5\cdot1.5+1\cdot1.5=\\&=1+2+3+0.5+0.75+1.5=8.75:\end{aligned}$$

6b31.
As the characteristic equation looks as follows,

$$|\lambda E-A|=\begin{bmatrix}\lambda+2&0\\-1&\lambda+1\end{bmatrix}=(\lambda+1)\cdot(\lambda+2)=\lambda^2+3\lambda+2=0,$$

the eigenvalues $\lambda_1=-2,\lambda_2=-1.$ The eigenvector, which corresponds to λ_1, has to be found from the homogeneous linear system $h_1=(h_{11},h_{21})^T$:

$$\begin{bmatrix}-2&0\\1&-1\end{bmatrix}\cdot\begin{pmatrix}h_{11}\\h_{21}\end{pmatrix}=-2\cdot\begin{pmatrix}h_{11}\\h_{21}\end{pmatrix},$$

and in the same way, the eigenvector $h_2=(h_{12},h_{22})^T$, which corresponds to λ_2, may be found from

$$\begin{bmatrix}-2&0\\1&-1\end{bmatrix}\cdot\begin{pmatrix}h_{12}\\h_{22}\end{pmatrix}=-1\cdot\begin{pmatrix}h_{12}\\h_{22}\end{pmatrix},$$

hence $h_{12}=0,$ and for h_{22}, $h_{22}=1$ can be chosen.
Solving these systems, the following is obtained:

$$\begin{pmatrix}h_{11}\\h_{21}\end{pmatrix}=\begin{pmatrix}-1\\1\end{pmatrix}\begin{pmatrix}h_{12}\\h_{22}\end{pmatrix}=\begin{pmatrix}0\\1\end{pmatrix}$$

So transform matrix is

$$H = \begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}$$

for which $\mathrm{H}^{-1} \equiv \mathrm{H}$.

Finally $$\Phi(t) = H \cdot \begin{bmatrix} e^{\lambda_1 t} & 0 \\ 0 & e^{\lambda_2 t} \end{bmatrix} \cdot H^{-1} = \begin{bmatrix} e^{-2t} & 0 \\ e^{-t} - e^{-2t} & e^{-t} \end{bmatrix}.$$

$$\Phi(t) = \begin{bmatrix} e^{-2t} & 0 \\ e^{-t} - e^{-2t} & e^{-t} \end{bmatrix}$$

6b32.
It is obvious that

$$B = \begin{bmatrix} 0 & 0.5 \\ 0.5 & 0 \\ 0.5 & 1 \end{bmatrix}, \; A \cdot B = \begin{bmatrix} 0.5 & 1.25 \\ 0.25 & 0.25 \\ 0.5 & 0.5 \end{bmatrix}, \; A^2 \cdot B = \begin{bmatrix} 0.75 & 1.125 \\ 0.375 & 0.75 \\ 0.375 & 0.375 \end{bmatrix}:$$

Therefore

$$rangL_x = rang\,[B \vdots AB \vdots A^2 B] = \left[\begin{array}{cc:cc:cc} 0 & 0.5 & 0.5 & 1.25 & 0.75 & 1.125 \\ 0.5 & 0 & 0.25 & 0.25 & 0.375 & 0.75 \\ 0.5 & 1 & 0.5 & 0.5 & 0.375 & 0.375 \end{array}\right] = 3,$$

then the system is fully controllable.

6b33.

Representing the function f by the first order Taylor formula in the point $\dfrac{a+b}{2}$, the following is obtained:

$$f(x) = f\left(\frac{a+b}{2}\right) + \frac{f\left(\frac{a+b}{2}\right)}{1!}\left(x - \frac{a+b}{2}\right) + \frac{f'(c)}{2!}\left(x - \frac{a+b}{2}\right)^2$$, where $c \in (a,b)$.

Substituting this expansion in the integral I, the following inequality is obtaiend:

$$\left|I - \widetilde{I}\right| = \left|\int_a^b \left(f(x) - f\left(\frac{a+b}{2}\right)\right) dx\right| = \left|\int_a^b \frac{f''(c)}{2!}\left(x - \frac{a+b}{2}\right)^2 dx\right| \le \frac{M_2}{2!}\int_a^b \left(x - \frac{a+b}{2}\right)^2 dx = \frac{M_2}{24}(b-a)^3$$, where

$M_2 = \max\limits_{x \in [a,b]} \left| f''(x) \right|$. The final expression is the seeking estimation.

6b34.

The main part of the proof is the following: taking convexity of the function e^x into account, inequalities $\widetilde{I}_1 < I < \widetilde{I}_2$ are obtained. After that, substituting values $I, \widetilde{I}_1, \widetilde{I}_2$, the required inequality is proved.

6b35.

n times apply Rolle's theorem first to the function f, then to the derivatives of this function.

6b36.

The function $g(x) = \dfrac{1}{1+x}$ is not a contraction on the half-line $[0,\infty)$, hence modify the successive approximation process, for example, in the following way. Applying the successive approximations formula, this is obtained:

$$x_{n+2} = \frac{1+x_n}{2+x_n}, \; n \ge 0.$$

The function $g_1(x)=\dfrac{1+x}{2+x}$ is a contraction (because of $|g_1'(x)|=\dfrac{1}{(2+x)^2}\le\dfrac{1}{4}<1$ for $x\ge 0$), therefore the sequences $\{x_{2k}\}_{k=1}^{\infty}$ and $\{x_{2k+1}\}_{k=1}^{\infty}$ converge to the same limit, which is a limit of the sequence $\{x_k\}_{k=1}^{\infty}$. This limit is a positive root of the equation $x^2+x-1=0$, that is equal to $\dfrac{\sqrt{5}-1}{2}$.

6b37.

Apply standard approximate formulas (rectangles formulas, trapezoidal formulas and so on), but in this case determine the maximal value of the modules of the derivative of the function $\dfrac{\sin x}{x}$ for the estimation of the remainder term. Therefore it is better to expand the function $\sin x$ in a Taylor series, divide by x and then integrate it term by term. Finally,

$$I=\sum_{k=0}^{\infty}(-1)^k\frac{1}{2^k(2k+1)!(2k+1)}.$$

It is alternate series; therefore, its remainder is less than the first omitted term. The integral will be calculated with prescribe accuracy if only two first summands are obtained.

6b38.

As the absolute term (P_3) of characteristic polynomial equals to determinant of matrix, then it will be

$$P_3=\det\begin{bmatrix}2&1&0\\0&2&4\\-2&0&2\end{bmatrix}=2\cdot2\cdot2+1\cdot(-2)\cdot4=0.$$

6b39.

As the coefficient of λ^2 in the characteristic polynomial is equal to $\mathrm{P}_2=\sum\limits_{\substack{i,j=1\\ i\ne j}}^{4}\lambda_i\cdot\lambda_j$, then

$$\begin{aligned}\mathrm{P}_2&=\lambda_1\lambda_2+\lambda_1\lambda_3+\lambda_1\lambda_4+\lambda_2\lambda_3+\lambda_2\lambda_4+\lambda_3\lambda_4=\\&=2\cdot0.5+2\cdot1+2\cdot3+0.5\cdot1+0.5\cdot3+1\cdot3=\\&=1+2+6+0.5+1.5+3=14:\end{aligned}$$

6b40.

As the characteristic equation looks as follows:

$$|\lambda\mathrm{E}-\mathrm{A}|=\begin{bmatrix}\lambda+1&0\\-2&\lambda+2\end{bmatrix}=(\lambda+1)\cdot(\lambda+2)=\lambda^2+3\lambda+2=0,$$

the eugenvalues $\lambda_1=-1,\lambda_2=-2.$ The eugenvector, which corresponds to λ_1, has to be found from the homogeneous linear system $\mathrm{h}_1=(\mathrm{h}_{11},\mathrm{h}_{21})^{\mathrm{T}}$.

$$\begin{bmatrix}-1&0\\2&-2\end{bmatrix}\cdot\begin{pmatrix}\mathrm{h}_{11}\\\mathrm{h}_{21}\end{pmatrix}=-1\cdot\begin{pmatrix}\mathrm{h}_{11}\\\mathrm{h}_{21}\end{pmatrix},$$

hence $\mathrm{h}_{11}=1,\ h_{21}=2.$

and in the same way, the eugenvector $\mathrm{h}_2=(\mathrm{h}_{12},\mathrm{h}_{22})^{\mathrm{T}}$ which corresponds to λ_2, may be found from

$$\begin{bmatrix}-1&0\\2&-2\end{bmatrix}\cdot\begin{pmatrix}\mathrm{h}_{12}\\\mathrm{h}_{22}\end{pmatrix}=-2\cdot\begin{pmatrix}\mathrm{h}_{12}\\\mathrm{h}_{22}\end{pmatrix},$$

hence $\mathrm{h}_{12}=0,\ \mathrm{h}_{22}=1.$

So, transform matrix is

$$\mathrm{H}=\begin{bmatrix}1&0\\2&1\end{bmatrix}$$

for which $H^{-1}=\begin{bmatrix}1 & 0\\ -2 & 1\end{bmatrix}$.

Finally

$$\Phi(t)=H\cdot\begin{bmatrix}e^{\lambda_1 t} & 0\\ 0 & e^{\lambda_2 t}\end{bmatrix}\cdot H^{-1}=\begin{bmatrix}1 & 0\\ 2 & 1\end{bmatrix}\begin{bmatrix}e^{-t} & 0\\ 0 & e^{-2t}\end{bmatrix}\begin{bmatrix}1 & 0\\ -2 & 1\end{bmatrix}=$$
$$=\begin{bmatrix}e^{-t} & 0\\ 2e^{-t} & e^{-2t}\end{bmatrix}\begin{bmatrix}1 & 0\\ -2 & 1\end{bmatrix}=\begin{bmatrix}e^{-t} & 0\\ \left(2e^{-t}-2e^{-2t}\right) & e^{-2t}\end{bmatrix};$$
$$\Phi(t)=\begin{bmatrix}e^{-t} & 0\\ \left(2e^{-t}-2e^{-2t}\right) & e^{-2t}\end{bmatrix};$$

6b41.
It is obvious that

$$B=\begin{bmatrix}0 & 1\\ 1 & 0\\ 1 & 2\end{bmatrix},\ A\cdot B=\begin{bmatrix}2 & 5\\ 1 & 1\\ 2 & 2\end{bmatrix},\ A^2\cdot B=\begin{bmatrix}6 & 9\\ 3 & 6\\ 3 & 3\end{bmatrix}.$$

Therefore

$$\mathrm{rang}L_x=\mathrm{rang}[B\vdots AB\vdots A^2B]=\left[\begin{array}{cc:cc:cc}0 & 1 & 2 & 5 & 6 & 9\\ 1 & 0 & 1 & 1 & 3 & 6\\ 1 & 2 & 2 & 2 & 3 & 3\end{array}\right]=3,$$

The system is fully controllable.

6b42.
The characteristic equation looks as follows:

$$|\lambda E-A|=\begin{vmatrix}\lambda+1 & 0\\ 1 & \lambda+3\end{vmatrix}=(\lambda+1)(\lambda+3)=\lambda^2+4\lambda+3=0,$$

hence eigenvalues $\lambda_1=-1,\quad \lambda_2=-3$. Therefore for $h_1=(h_{11},\ h_{21})^T$ Eigen vector, corresponding to Φ_1, there is the following linear homogeneous algebraic system of equations:

$$\begin{bmatrix}-1 & 0\\ 1 & -3\end{bmatrix}\cdot\begin{pmatrix}h_{11}\\ h_{21}\end{pmatrix}=-1\cdot\begin{pmatrix}h_{11}\\ h_{21}\end{pmatrix}$$, hence $h_{11}=1$, $h_{21}=1$,

and for $h_2=(h_{12},\ h_{22})^T$ Eigen vector, corresponding to Φ_2:

$$\begin{bmatrix}-1 & 0\\ 1 & -3\end{bmatrix}\cdot\begin{pmatrix}h_{12}\\ h_{22}\end{pmatrix}=-3\cdot\begin{pmatrix}h_{12}\\ h_{22}\end{pmatrix}$$, hence $h_{12}=0$, $h_{22}=1$.

So the transform matrix:

$$H=\begin{bmatrix}1 & 0\\ 1 & 1\end{bmatrix},$$

And its inverse:

$$H^{-1}=\begin{bmatrix}1 & 0\\ -1 & 1\end{bmatrix};$$

Therefore:

$$\Phi(t)=H\cdot\begin{bmatrix}e^{\lambda_1 t} & 0\\ 0 & e^{\lambda_2 t}\end{bmatrix}\cdot H^{-1}=\begin{bmatrix}e^{-t} & 0\\ \left(e^{-t}-e^{-3t}\right) & e^{-3t}\end{bmatrix}.$$

6b43.
It is obvious that

$$B=\begin{bmatrix}1&0\\0&1\\1&1\end{bmatrix},\quad A\cdot B=\begin{bmatrix}2&1\\1&2\\1&1\end{bmatrix},\quad A^2\cdot B=\begin{bmatrix}3&2\\2&3\\3&3\end{bmatrix}:$$

therefore

$$\text{rang}L=\text{rang}\left[B\,\vdots\,AB\,\vdots\,A^2B\right]=\text{rang}\begin{bmatrix}1&0&\vdots&2&1&\vdots&3&2\\0&1&\vdots&1&2&\vdots&2&3\\1&1&\vdots&1&1&\vdots&3&3\end{bmatrix}=3,$$

then the system is fully controllable.

6b44.

As

$$C^T=\begin{bmatrix}1&3\\2&2\\0&1\end{bmatrix},\quad A^T\cdot C^T=\begin{bmatrix}5&8\\2&7\\2&3\end{bmatrix},\quad \left(A^2\right)^T\cdot C^T=\begin{bmatrix}9&22\\12&19\\9&18\end{bmatrix},$$

then

$$\text{rang}K=\text{rang}\left[C^T\,\vdots\,A^TC^T\,\vdots\,\left(A^2\right)^TC^T\right]=\text{rang}\begin{bmatrix}1&3&\vdots&5&8&\vdots&9&22\\2&2&\vdots&2&7&\vdots&12&19\\0&1&\vdots&2&3&\vdots&9&18\end{bmatrix}=3\cdot$$

Therefore the system is fully observable.

6b45.

The differential equation, corresponding to additional $x_0(t)$ variable:

$$\dot{x}_0(t)=u_1^2(t)+u_2^2(t).$$

Then Hamilton's function:

$$H=\Psi_0(t)\cdot\dot{x}_0(t)+\Psi_1(t)\cdot\dot{x}_1(t)+\Psi_2(t)\cdot\dot{x}_2(t)=$$
$$=\Psi_0(t)\cdot\left(u_1^2(t)+u_2^2(t)\right)+\Psi_1(t)\cdot\left(x_1(t)+x_2(t)+u_1(t)\right)+\Psi_2(t)\cdot\left(x_2(t)+u_1(t)+u_2(t)\right)\xrightarrow{\quad}\max_{u_1(t),u_2(t)},$$

where $\Psi_0(t)$, $\Psi_1(t)$ and $\Psi_2(t)$ are corresponding complementary variables.

Therefore the system of complementary variables will be:

$$\begin{cases}\dot{\Psi}_0(t)=-\dfrac{\partial H}{\partial x_0(t)}=0, & \text{hence } \Psi_0(t)=\text{const},\\ \dot{\Psi}_1(t)=-\dfrac{\partial H}{\partial x_1(t)}=-\Psi_1(t), & \\ \dot{\Psi}_2(t)=-\dfrac{\partial H}{\partial x_2(t)}=-\Psi_1(t)-\Psi_2(t), & \end{cases}$$

And for the functions of optimal control:

$$\begin{cases}\dfrac{\partial H}{\partial u_1(t)}=2\cdot\Psi_0(t)\cdot u_1(t)+\Psi_1(t)+\Psi_2(t)=0,\\ \dfrac{\partial H}{\partial u_2(t)}=2\cdot\Psi_0(t)\cdot u_2(t)+\Psi_2(t)=0:\end{cases}$$

Therefore:

$$u_{1opt}(t) = -\frac{\Psi_1(t)+\Psi_2(t)}{2\Psi_0(t)},$$

$$u_{2opt}(t) = -\frac{\Psi_2(t)}{2\Psi_0(t)}:$$

6b46.

From matrix structure it is not difficult to see the multiplicity of its intrinsic values (characteristic equation roots), i.e. $\lambda_1 = \lambda_2 = \lambda_3 = 2$. Therefore

$$\lambda_1^3 + \lambda_2^3 + \lambda_3^3 = 3 \cdot \lambda_1^3 = 3 \cdot 2^3 = 24.$$

6b47.

It is obvious that the matrix of state variables of the system is cososymmetric. On the other hand, it is known that for such systems:

$\psi^T(t) \cdot \psi(t)_{|\forall t} = x^T(t) \cdot x(t)_{|\forall t} = x^T(t) \cdot x(t)_{|t=0} = x^T(0) \cdot x(0) = const$, where

$x(t) = \left(x_1(t),\ x_2(t),\ x_3(t)\right)^T$ – vector of state variables.

Therefore $\quad \psi^T(t) \cdot \psi(t)_{|t=2} = x^T(0) \cdot x(0) = \sum_{i=1}^{3} x_i^2(0) = (-1)^2 + (2)^2 + (1)^2 = 6.$

6b48.

Scalar differential equation, corresponding to additional $X_0(t)$ variable:

$$\dot{X}_0(t) = U_1^2(t) + U_2^2(t):$$

Therefore Hamilton's function:

$$H = \psi_0(t) \cdot \dot{X}_0(t) + \psi_1(t) \cdot \dot{X}_1(t) + \psi_2(t) \cdot \dot{X}_2(t) = \psi_0(t) \cdot \left(U_1^2(t) + U_2^2(t)\right) +$$
$$+\psi_1(t)\left(X_1(t) + 2X_2(t) + U_1(t)\right) + \psi_2(t)\left(2X_1(t) + U_1(t) + U_2(t)\right) \xrightarrow[U_1(t),U_2(t)]{} min,$$

where $\psi_0(t)$, $\psi_1(t)$ and $\psi_2(t)$ – respective conjugate variables. Therefore the system of conjugate variables will be:

$$\begin{cases} \dot{\psi}_0(t) = -\dfrac{\partial H}{\partial X_0(t)} = 0, \ \ hence \quad \psi_0(t) = const, \\ \dot{\psi}_1(t) = -\dfrac{\partial H}{\partial X_1(t)} = -\psi_1(t) - 2\psi_2(t), \\ \dot{\psi}_2(t) = -\dfrac{\partial H}{\partial X_2(t)} = -2\psi_1(t), \end{cases}$$

and optimal control functions will be defined from the following regularity condition of Hamilton function:

$$\begin{cases} \dfrac{\partial H}{\partial U_1(t)} = 2\psi_0(t) \cdot U_1(t) + \psi_1(t) + \psi_2(t) = 0, \\ \dfrac{\partial H}{\partial U_2(t)} = 2\psi_0(t) \cdot U_2(t) + \psi_2(t) = 0. \end{cases}$$

Therefore:

$$U_{1_{opt}}(t) = -\frac{\psi_1(t) + \psi_2(t)}{2\psi_0(t)},$$

$$U_{2_{opt}}(t) = -\frac{\psi_2(t)}{2\psi_0(t)} \ :$$

6b49.

From matrix structure it is not difficult to see the multiplicity of its intrinsic values (characteristic equation roots), $\lambda_1 = \lambda_2 = 2$; $\lambda_3 = 4$. Therefore

$$\lambda_1^2 + \lambda_2^2 + \lambda_3^2 = 2^2 + 2^2 + 4^2 = 24$$

6b50.

It's obvious that

$$B = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix}, \quad A \cdot B = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} 2 & 1 \\ 1 & 1 \\ 1 & 2 \end{bmatrix},$$

$$A^2 \cdot B = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \cdot \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} 2 & 3 \\ 3 & 2 \\ 3 & 3 \end{bmatrix}:$$

Therefore

$$rang[B \vdots AB \vdots A^2B] = rang\left[\begin{array}{cc|cc|cc} 0 & 1 & 2 & 1 & 2 & 3 \\ 1 & 0 & 1 & 1 & 3 & 2 \\ 1 & 1 & 1 & 2 & 3 & 3 \end{array}\right] = 3,$$

Therefore the system is fully controllable.

6b51.
It is obvious that the matrix of state variables of the system is cososymmetric. On the other hand, it is known that for such systems:
$\psi^T(t) \cdot \psi(t)_{|\forall t} = x^T(t) \cdot x(t)_{|\forall t} = x^T(t) \cdot x(t)_{|t=0} = x^T(0) \cdot x(0) = \text{const}$, where

$x(t) = \left(x_1(t),\ x_2(t),\ x_3(t)\right)^T$ is vector of state variables.

So $\psi^T(t) \cdot \psi(t)_{|t=2} = x^T(0) \cdot x(0) = \sum_{i=1}^{3} x_i^2(0) = 1^2 + 0^2 + 1^2 = 2$:

6b52.
Let $y=0$. Then $f(x)=\dfrac{f(x)+f(0)}{1-f(x)f(0)}$, or $\left(1+f^2(x)\right)f(0)=0$, that is $f(0)=0$. Differentiate both sides by x. There is

$$f'(x+y)=\frac{f'(x)\left(1+f^2(y)\right)}{\left(1-f(x)f(y)\right)^2}.$$

Let $x=0$. Get the following differential equation $f'(y)=C\left(1+f^2(y)\right)$, where $f'(0)=C$. Solving that equation with the initial condition $f(0)=0$, this is obtained $f(x)=\tan Cx$.

6b53.
Represent x in the form $x=[x]+\alpha$, where $0\le\alpha<1$. Then, for some integer k, $0<k\le n$, there is $\dfrac{n-k}{n}\le\alpha<\dfrac{n-k+1}{n}$, therefore:

$$\left[x+\frac{j}{n}\right]=[x],\text{ for } 0\le j\le k-1;\ \left[x+\frac{j}{n}\right]=[x]+1,\text{ for } k\le j\le n-1.$$

Hence,

$$[x]+\left[x+\frac{1}{n}\right]+\left[x+\frac{2}{n}\right]+\cdots+\left[x+\frac{n-1}{n}\right]=n[x]+n-k.$$

On the other side, $[nx]=[n[x]+n\alpha]=n[x]+n-k$. Identity is proved.

6b54.
The quantity of points with integer coordinates in the domain D is defined by the formula:

$$A=[f(a)]+[f(a+1)]+\cdots+[f(b-1)]+[f(b)].$$

Using this formula we get that S is a number of points with integer coordinates in the domain $D=\left\{(x,y):1\le x\le p-1,\ 0\le y\le\dfrac{q}{p}x\right\}$. There are no points with integer coordinates in the segment $y=\dfrac{q}{p}x$, for $1\le x\le p-1$, (p and q are relatively prime integers), therefore S is equal to the half of the quantity of points with integer coordinates in the domain $G=\{(x,y):1\le x\le p-1,\ 1\le y\le q-1\}$, or

$$S=\frac{(p-1)(q-1)}{2}.$$

6b55.
Add to all the n^2 elements the variable x. The obtained determinant

$$F(x)=\begin{vmatrix} r_1+x & a+x & \cdots & a+x \\ b+x & r_2+x & \cdots & a+x \\ \cdots & \cdots & \cdots & \cdots \\ b+x & b+x & \cdots & r_n+x \end{vmatrix}$$

is a linear function and therefore is defined by two values. Hence, considering that $F(-a)=f(a)$ and $F(-b)=f(b)$, this is obtained:

$$F(x)=\frac{f(a)-f(b)}{b-a}x+\frac{f(a)b-f(b)a}{b-a}.$$

Thus, taking into account, that $F(0)=\Delta$, there is:

$$\Delta=\frac{f(a)b-f(b)a}{b-a}.$$

6b56.

Represent the desired limit in the form:

$$A=\lim_{n\to\infty}\sum_{k=1}^{n}\left(\frac{k}{n}\right)^{\alpha-1}\frac{1}{n}=\lim_{n\to\infty}\sum_{k=1}^{n}\left(\frac{k}{n}\right)^{\alpha-1}\left(\frac{k}{n}-\frac{k-1}{n}\right).$$

The sum under last limit is an integral sum of the function $x^{\alpha-1}$ on the interval $[0,1]$, therefore

$$A=\int_0^1 x^{\alpha-1}dx=\frac{1}{\alpha}.$$

6b57.

Find the derivatives of both parts by y. Get

$$f'\left(\frac{x+y}{2}\right)\frac{1}{2}=\frac{f'(y)}{2}.$$

Let $y=0$. Get a differential equation $f'\left(\frac{x}{2}\right)=f'(0)$. Solving this equation, $f(x)=Ax+B$ is obtained where A and B are arbitrary constants.

6b58.

Using identity

$$\begin{pmatrix} A^{-1} & -A \\ 0 & I \end{pmatrix}\begin{pmatrix} A & B \\ A^{-1} & C \end{pmatrix}=\begin{pmatrix} 0 & A^{-1}B-AC \\ A^{-1} & C \end{pmatrix},$$

one gets

$$\det A^{-1}\det\begin{pmatrix} A & B \\ A^{-1} & C \end{pmatrix}=-\det\left(A^{-1}\left(A^{-1}B-AC\right)\right),$$

which proves the sought equality.

6b59.

Represent the given equation in the form $0.5\left((f'(x))^2\right)'=0$ which implies that $f'(x)=const$. Therefore: $f(x)=ax+b$, where a,b are arbitrary constants.

6b60.

For $y(x)=\int_0^x (x-t)f(t)dt$, $f(x)=y''(x)$ and $y(0)=y'(0)=0$. After the substitution, Cauchy problem is obtained for a linear equation with constant coefficients $y''-9y=3x$. Solving this problem, results in $f(x)=sh3x$.

6b61.

From the equation, $f(x)-f\left(\frac{x}{4}\right)=\frac{x}{4}$. Substituting x with $\frac{x}{4}$, $f\left(\frac{x}{4}\right)-f\left(\frac{x}{16}\right)=\frac{x}{16}$ and further $f\left(\frac{x}{4^k}\right)-f\left(\frac{x}{4^{k+1}}\right)=\frac{x}{4^{k+1}}$. Adding the obtained equations from 1 to n $f(x)-f\left(\frac{x}{4^{n+1}}\right)=x\left(\frac{1}{4}+\frac{1}{4^2}+\cdots\frac{1}{4^{n+1}}\right)$When n tends to infinity, $f(x)-f(0)=x\frac{1}{3}$ or $f(x)=\frac{x}{3}+8$ is obtained.

6b62.

The first player needs to win two rounds to win the game, the second player – three rounds. Therefore, the match ends after four rounds.
X – the first player's win
Y – the second player's win
The first player can win in these cases:
XX – the first player wins in two consecutive rounds
XYX – the first player wins once in the first two rounds and then wins in the third round
XYYX – the first player wins once in the first three rounds and then wins in the fourth round

The corresponding probability equals to $\left(\frac{1}{2}\right)^2+\left(C_2^1\frac{1}{2}\cdot\frac{1}{2}\right)\cdot\frac{1}{2}+\left(C_3^1\frac{1}{2}\cdot\left(\frac{1}{2}\right)^2\right)\cdot\frac{1}{2}=\frac{11}{16}$

The second player can win in these cases:
YYY – the second player wins in three consecutive games
YXYY – the second player wins twice in the first three rounds and then wins the fourth round

The corresponding probability equals to $\left(\frac{1}{2}\right)^3+\left(C_3^1\frac{1}{2}\cdot\left(\frac{1}{2}\right)^2\right)\cdot\frac{1}{2}=\frac{5}{16}$

Therefore the fair division of the stake is 11:5, i.e. 11/8 A\$ for the first player 5/8 A\$ for the second.

6b63.

Present $a_n=\frac{n}{a^n}\sum_{k=1}^{n}\frac{a^k}{k}$ in the form:

$$a_n=n\sum_{k=1}^{n}\frac{1}{k}a^{-(k-n)}=n\sum_{m=0}^{n-1}\frac{1}{n-m}a^{-m}=\sum_{m=0}^{n-1}\frac{n}{n-m}a^{-m}=$$

$$=\sum_{m=0}^{n-1}a^{-m}+\sum_{m=0}^{n-1}\frac{m}{n-m}a^{-m}=\frac{1-\frac{1}{a^n}}{1-\frac{1}{a}}+I_n$$

Then $0\le I_n=\sum_{m=0}^{\left[\frac{n}{2}\right]}\frac{m}{n-m}a^{-m}+\sum_{m=\left[\frac{n}{2}\right]+1}^{n-1}\frac{m}{n-m}a^{-m}\le\frac{1}{\frac{n}{2}}\sum_{m=0}^{\left[\frac{n}{2}\right]}ma^{-m}+\sum_{m=\left[\frac{n}{2}\right]+1}^{n-1}ma^{-m}$.

Considering that the series $\sum_{m=0}^{\infty}ma^{-m}$ converge, we get $\sum_{m=0}^{\left[\frac{n}{2}\right]}ma^{-m}<c$ and $\sum_{m=\left[\frac{n}{2}\right]+1}^{n-1}ma^{-m}\to 0$ when $n\to\infty$, i.e. $I_n\to 0$ when $n\to\infty$. Finally $\lim a_n=\frac{a}{a-1}$.

6b64.

$x_{n+1}=\cos x_n \quad x_1=\cos x\in[0,1]$
$g(x)=\cos x \quad g:[0,1]\to[0,1]$
$|g'(x)|=|\sin x|<\frac{\sqrt{3}}{2}<1$, for $x\in[0,1]\Rightarrow g$ is contractive, i.e. $x_n\to x$. $x=\cos x\approx 0,732$

6b65.

Put $tgu = x, tgv = y$ in place of x and y. Get $f(tgu) + f(tgv) = f(tg(u+v))$ i.e. $\phi(u) = f(tgu)$ satisfies the conditions $\phi(u) + \phi(v) = \phi(u+v)$. Therefore $\phi(0) = 0$ and $\phi'(u) = \phi'(u+v)$. For $u = 0$, this is obtained: $\phi'(v) = 0$ thus $\phi(v) = cv$. Finally $f(tgx) = cx$ and $f(x) = arctgx$.

7. DISCRETE MATHEMATICS AND THEORY OF COMBINATIONS

a) Test questions

7a1. E
7a2. A
7a3. B
7a4. A
7a6. A
7a7. C
7a8. E
7a9. E
7a10. D
7a11. C
7a12. D
7a13. A
7a14. B
7a15. A
7a16. C
7a17. D
7a18. D
7a19. E
7a20. A
7a21. E
7a22. A
7a23. B
7a24. B
7a25. E
7a26. D
7a27. B
7a28. C
7a29. E
7a30. A
7a31. E
7a32. D
7a33. E
7a34. B
7a35. A
7a36. C
7a37. D
7a38. B
7a39. A
7a40. B
7a41. C
7a42. B
7a43. B
7a44. C
7a45. B
7a46. E
7a47. E
7a48. D
7a49. C
7a50. C
7a51. B
7a52. C
7a53. C
7a54. B
7a55. C
7a56. C
7a57. B
7a58. B
7a59. B
7a60. B
7a61. C
7a62. D
7a63. C
7a64. B
7a65. C
7a66. B
7a67. C
7a68. E
7a69. B
7a70. B
7a71. C
7a72. C
7a73. E
7a74. A
7a75. C
7a76. C
7a77. A
7a78. E
7a79. C
7a80. C
7a81. D
7a82. C
7a83. B
7a84. D
7a85. E
7a86. A
7a87. B
7a88. C
7a89. A
7a90. E
7a91. C
7a92. D
7a93. A
7a94. B
7a95. D
7a96. B
7a97. E
7a98. C
7a99. B
7a100. E
7a101. A
7a102. C
7a103. B
7a104. B
7a105. E
7a106. C
7a107. E
7a108. D
7a109. B
7a110. C
7a111. E
7a112. E
7a113. D
7a114. D
7a115. E
7a116. D
7a117. A
7a118. B
7a119. D
7a120. C
7a121. A
7a122. B

b) Problems

7b1.

As ξ_1=w, ξ_2=w, ξ_3=w, but $\xi_1+\xi_2$=w, $\xi_1+\xi_3$=w and $\xi_2+\xi_3$=w, therefore the corresponding threshold function will be:

$$x_1x_2 \vee x_1x_3 \vee x_2x_3,$$

to get Zhegalkin polynomial of which it is enough to use the following equation:

$$a \vee b = a \oplus b \oplus ab,$$

$$x_1x_2 \vee x_1x_3 \vee x_2x_3 = (x_1x_2 \oplus x_1x_3 \oplus x_1x_2x_3) \vee x_2x_3 = x_1x_2 \oplus x_1x_3 \oplus x_1x_2x_3 \oplus x_2x_3 \oplus (x_1x_2 \oplus x_1x_3 \oplus x_1x_2x_3) *$$
$$* x_2x_3 = x_1x_2 \oplus x_1x_3 \oplus x_1x_2x_3 \oplus x_2x_3 \oplus x_1x_2x_3 \oplus x_2x_3 \oplus x_1x_2x_3 \oplus x_1x_2x_3 = x_1x_2 \oplus x_1x_3 \oplus x_2x_3:$$

7b2.

To verify the wholeness of the system it is enough to use Post theorem, i.e. find out if the system is fully included in any of classes of T_0, T_1, S, M, L?

- It is not included in T_0 as $x_1 \rightarrow x_2 \notin T_0$;
- It is not included in T_1 as $x_1x_2\overline{x_3} \notin T_1$;
- It is not included in S as $x_1 \vee x_2 \notin S$ (the functions depending on two variables are not self-dual at all);
- It is not included in M as $x_1 \rightarrow x_2 \notin M$ (00 set proceeds 10 set, whereas $0 \rightarrow 0 = 1$ and $1 \rightarrow 0 = 0$, i.e. monotony condition is violated);
- It is not included in L as $x_1 \oplus x_2 \oplus x_1x_2$ function is $x_1 \vee x_2$ Zhegalkin polynomial and contains sum of variables, i.e. it is not linear - $x_1 \vee x_2 \notin L$

According to Post theorem, the system is complete.

7b3.

It is clear $\overline{x} \notin T_0$, $\overline{x} \notin T$, $1 \notin S$ (as its table consists only of 1s and self-duality condition is violated – anti-symmetry towards middle line), $\overline{x} \notin M$ (as $0 \prec 1$, but $\overline{0} > \overline{1}$), $(x_1 \rightarrow x_2) \rightarrow x_3 \notin L$, as $a \rightarrow b = \overline{a} \vee b$, therefore $(x_1 \rightarrow x_2) \rightarrow x_3 = (x_1 \vee x_2) \rightarrow x_3 = \overline{\overline{x_1} \vee x_2} \vee x_3 = x_1\overline{x_2} \vee x_3$, and from $a \vee b = a \oplus b \oplus ab$ equation it follows that $x_1\overline{x_2} \vee x_3 = x_1\overline{x_2} \oplus x_3 \oplus x_1\overline{x_2}x_3 = x_1(1 \oplus x_2) \oplus x_3 \oplus x_1x_3(1 \oplus x_2) = x_1 \oplus x_1x_2 \oplus x_3 \oplus x_1x_3 \oplus x_2x_3 \notin L.$

According to Post theorem, the system is complete.

7b4.

Search the solution in the form of indefinite coefficients.

x_1	x_2	x_3	$(x_1 \rightarrow x_2)^{\overline{x_3}}$
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$(x_1 \rightarrow x_2)^{\overline{x_3}} = a_0 \oplus a_1x_1 \oplus a_2x_2 \oplus a_3x_3 \oplus a_{12}x_1x_2 \oplus a_{13}x_1x_3 \oplus a_{23}x_2x_3 \oplus a_{123}x_1x_2x_3$

$1 = a_0$

$0 = a_3 \oplus 1$, $a_3 = 1$

$1 = 1 \oplus a_2$, $a_2 = 0$

$0 = 1 \oplus 1 \oplus a_{23}$, $a_{23} = 0$

$0 = 1 \oplus a_1$, $a_1 = 1$

$1 = 1 \oplus 1 \oplus 1 \oplus a_{13}$, $a_{13} = 0$

$1 = 1 \oplus 1 \oplus a_{12}$, $a_{12} = 1$

$0 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus a_{123}$, $a_{123} = 0$

Answer $1 \oplus x_1 \oplus x_3 \oplus x_1x_2$.

7b5.

Applying "divide to own" standard tactics, it is possible to get the solution of the problem by the following method:

a. Counting the number of units in couples
b. Summing couples
c. Counting the number of units in tetrads
d. Summing tetrads
e. The same continues for objects, 16-bit, 32-bit and other sequences

f. At the end of the process the number contains the number of units.

An example of solution for 16-bit number:

```
Count (n)
        n = (n & 0x5555) + ((n >> 1) & 0x5555)
        n = (n & 0x3333) + ((n >> 2) & 0x3333)
        n = (n & 0x0F0F) + ((n >> 4) & 0x0F0F)
        n = (n & 0x00FF) + ((n >> 8) & 0x0F0F)
return n;
```

7b6.

Taking binary arithmetic property into consideration, that N&(N-1) reduces the amount of units in the number by 1, which follows from the fact that N-1 makes all zeros at the end of the number into 1, and junior class unit - 0,leaving all high classes without change. Now, applying this action in the cycle, the amount of units in the number can be counted.

```
Count (n)
C = 0;
while (n <> 0)
        n = (n&(n-1))
        C = C + 1
Return C
```

7b7.

Applying partition procedure, which is applied in QuickSort family algorithms, it is possible to get the following linear algorithm:

```
select(a, k, left, right)
pivotNewIndex = partition(a, left, right, pivotIndex)
while (k <> pivotNewIndex)
        if k < pivotNewIndex
                right = pivotNewIndex-1
        else
                left = pivotNewIndex + 1
        pivotNewIndex = partition(a, left, right, pivotIndex)
return k;
```

7b8.

Heap building is implemented in O(NlogN) period of time. Accordingly, applying the following algorithm, the elements can be classified in O(NlogN) period of time. The first (minimum or maximum) element is selected, substituted by the latter, after which the last element is shifted down its position in the heap, using ShiftDown standard procedure which requires O(logN) time. Applying N-1 procedure, sorted array in O(NlogN) period of time is obtained.

7b9.

Disjunctive normal form of this function having the mentioned table will be:

$$f = \bar{x}_1\bar{x}_2\bar{x}_3 \vee \bar{x}_1\bar{x}_2 x_3 \vee \bar{x}_1 x_2 x_3 \vee x_1\bar{x}_2\bar{x}_3 \vee x_1 x_2\bar{x}_3 \vee x_1 x_2 x_3$$

x_1	x_2	x_3	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Applying the first part of Qwine algorithm (“assembling”), the following will be obtained:

$\bar{x}_1\bar{x}_2\bar{x}_3 \vee \bar{x}_1\bar{x}_2 x_3 \vee \bar{x}_1 x_2 x_3 \vee x_1\bar{x}_2\bar{x}_3 \vee x_1 x_2\bar{x}_3 \vee x_1 x_2 x_3 \vee \bar{x}_1\bar{x}_2 \vee \bar{x}_2\bar{x}_3 \vee \bar{x}_1 x_3 \vee x_2 x_3 \vee x_1\bar{x}_3 \vee x_1 x_2$

Applying the second part of Qwine algorithm (“absorption”), the following will be obtained: $\bar{x}_1\bar{x}_2 \vee \bar{x}_2\bar{x}_3 \vee \bar{x}_1 x_3 \vee x_2 x_3 \vee x_1\bar{x}_3 \vee x_1 x_2$

7b10.

Search Zhegalkin polynomial in the following form:

$$f(x_1, x_2, x_3) = a_0 \oplus a_1 x_1 \oplus a_2 x_2 \oplus a_3 x_3 \oplus a_{12} x_1 x_2 \oplus a_{13} x_1 x_3 \oplus a_{23} x_2 x_3 \oplus a_{123} x_1 x_2 x_3$$

x_1	x_2	x_3	$f(x_1,x_2,x_3)$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Substituting the right and left parts of the equation, sequentially all the possible values to x_1, x_2 and x_3 variables, this will be obtained:

$1=a_0$

$1=1\oplus a_3,\ a_3=0$

$1=1\oplus a_2,\ a_2=0$

$1=1\oplus 1\oplus a_{23},\ a_{23}=1$

$1=1\oplus a_1,\ a_1=0$

$1=1\oplus a_{13},\ a_{13}=0$

$1=1\oplus 1\oplus a_{12},\ a_{12}=0$

$1=1\oplus 1\oplus 1\oplus a_{123},\ a_{123}=0$

Putting the obtained values of the coefficients, Zhegalkin polynomial of the function will be obtained.

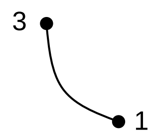
$$f(x_1,x_2,x_3)=1\oplus x_2\oplus x_2x_3$$

7b11.

As the length of Cayley h(G)=(3,5,4,4,5,6,7,8) vertex is equal 8, therefore the number of tree nodes equals 8+2=10. The numbers of those nodes are:

(1,2,3,4,5,6,7,8,9,10)

From those numbers choose the number from the left which is missing in Cayley code. That number is 1. Connect the node of 1 number with number one node of the vertex by edge.



Delete 1 and 3 from the list of the number of nodes and vertex. The following will be obtained.

$(\cancel{1},2,3,4,5,6,7,8,9,10)$

$(\cancel{3},5,4,4,5,6,7,8)$

Do the same action after delete with the numbers of nodes and those numbers of nodes written in the code. This time connect the nodes of 2 and 5 numbers by edge and 2 and 5 numbers will be deleted from the list. This will be obtained:

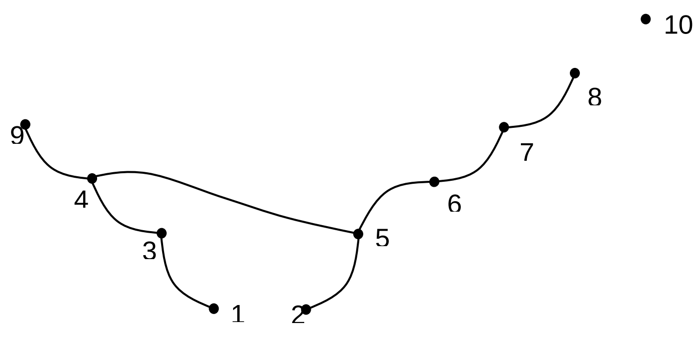
$(\cancel{1},\cancel{2},3,4,5,6,7,8,9,10)$

$(\cancel{3},\cancel{5},4,4,5,6,7,8)$

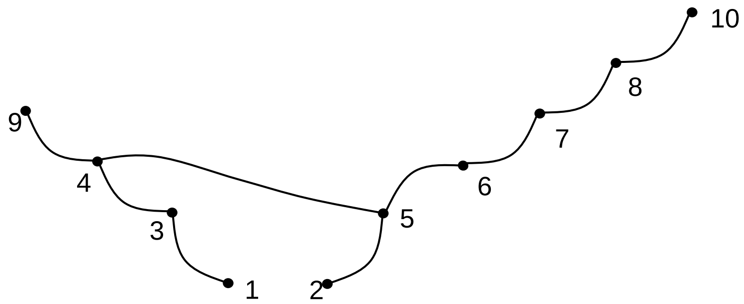
Continuing this action in the 8th step, this will be obtained

$(\cancel{1},\cancel{2},\cancel{3},\cancel{4},\cancel{5},\cancel{6},\cancel{7},8,\cancel{9},10)$

$(\cancel{3},\cancel{5},\cancel{4},\cancel{4},\cancel{5},\cancel{6},\cancel{7},\cancel{8})$



The last, final step is the connection of nodes with 8 and 10 numbers.



7b12.

x_1	x_2	x_3	$x_1^{x_2} \vee x_2^{x_3}$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

$x_1^{x_2} \vee x_2^{x_3} \notin S$, as the table is not antisymmetric.

$x_1\bar{x}_2 \notin M$, as for (1,0) and (1,1) the monotony condition is violated.

$x_1 \to x_2 \notin T_0$, as $0 \to 0 = 1$.

$x_1\bar{x}_2 \notin T_1$, as $1 \cdot \bar{1} = 0$.

$x_1\bar{x}_2 \notin L$, as $x_1\bar{x}_2 = x_1 \oplus x_1x_2$.

The system is complete.

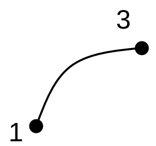
7b13.

As the code length equals 8, the number of tree nodes equals 10. The numbers of those nodes and tree code are:

(1,2,3,4,5,6,7,8,9,10)

(3,2,4,4,5,6,8,8)

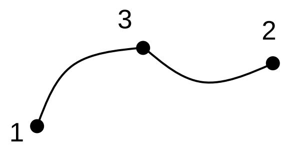
From those numbers choose the number from left to right which is missing in the code. It is 1. Connect the node of that number with number one node of the code from the left and delete those two numbers. The following will be obtained:



$(\cancel{1},2,3,4,5,6,7,8,9,10)$

$(\cancel{3},2,4,4,5,6,7,8)$

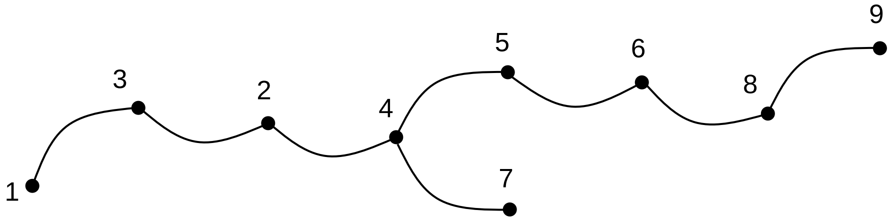
Apply the same process sequentially towards the obtained results. Once more the first number of the node from the left, which is missing in the code is 3. Connect the node of 3 number with the recurrent number of the node 3 and delete the two nodes. The following will be obtained:



$(\cancel{1},2,\cancel{3},4,5,6,7,8,9,10)$

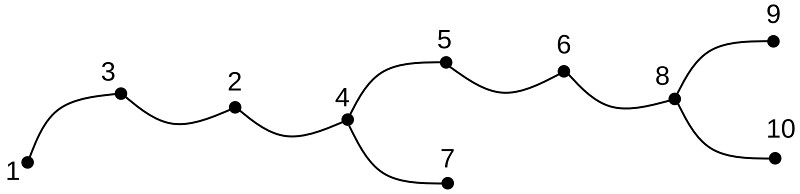
$(\cancel{3},\cancel{2},4,4,5,6,7,8)$

Continuing this action until deleting all the numbers in the code, this is obtained:



$$(\cancel{1},\cancel{2},\cancel{3},\cancel{4},\cancel{5},\cancel{6},\cancel{7},8,\cancel{9},10)$$
$$(3,2,4,4,5,6,7,8)$$

The last, final step in the connection of not deleted nodes with 8 and 10 numbers in the end.



7b14.

To verify the wholeness of $\left\{x_1^{x_3} v x_2^{x_1}, x_1 \to \bar{x}_2, x_1 \oplus x_2\right\}$ system it is enough to use Post theorem. It is clear that

$x_1 \to \bar{x}_2 \notin T_0$, as $0 \to \bar{0} = 1$;

$x_1 \oplus x_2 \notin T_1$, as $1 \oplus 1 = 0$;

$x_1 \oplus x_2 \notin S$, as the functions depending on two variables are not self-dual;

$x_1 \oplus x_2 \notin M$, as $(0,1) \le (1,1)$ whereas $0 \oplus 1 = 1$, $1 \oplus 1 = 0$;

$x_1 \to \bar{x}_2 \notin L$, as $x_1 \to \bar{x}_2 = \bar{x}_1 \vee \bar{x}_2 = \overline{x_1 x_2} = 1 \oplus x_1 x_2$, i.e. Zhegalkin polynomial contains sum of variables.

Therefore, the system is complete.

7b15.

$\xi_1 = 2$, $\xi_2 = 5$, $\xi_3 = 7$, $\xi_4 = 10$, w=10.

As $\xi_2 + \xi_3 = 5 + 7 = 12 > 10$ and $\xi_4 \ge 10$, the threshold function will be:

$$x_2 x_3 \vee x_4,$$

x_1 variable's activity of this function equals 0, as x_1 is fictitious variable.

$$\omega_2^{x_2 x_3 \vee x_4} = \left\|\bar{x}_4\right\| \omega_2^{x_2 x_3} = \frac{1}{2} \cdot \left\|x_3\right\| = \frac{1}{2} \cdot \frac{1}{2} = \frac{1}{4}.$$

Due to symmetry

$$\omega_3^{x_2 x_3 \vee x_4} = \frac{1}{4}.$$

$$\omega_4^{x_2 x_3 \vee x_4} = \left\|\overline{x_2 x_3}\right\| \omega_4^{x_4} = 1 - \left\|x_2 x_3\right\| = 1 - \frac{1}{4} = \frac{3}{4}.$$

7b16.

To verify the wholeness of $\left\{x_1 x_2, x_1 \to x_2, x_1 \oplus x_2, x_1 v x_2\right\}$ system it is enough to use Post theorem. It is clear that

$x_1 \to x_2 \notin T_0$, as $0 \to 0 = 1$;

$x_1 \oplus x_2 \notin T_1$, as $1 \oplus 1 = 0$;

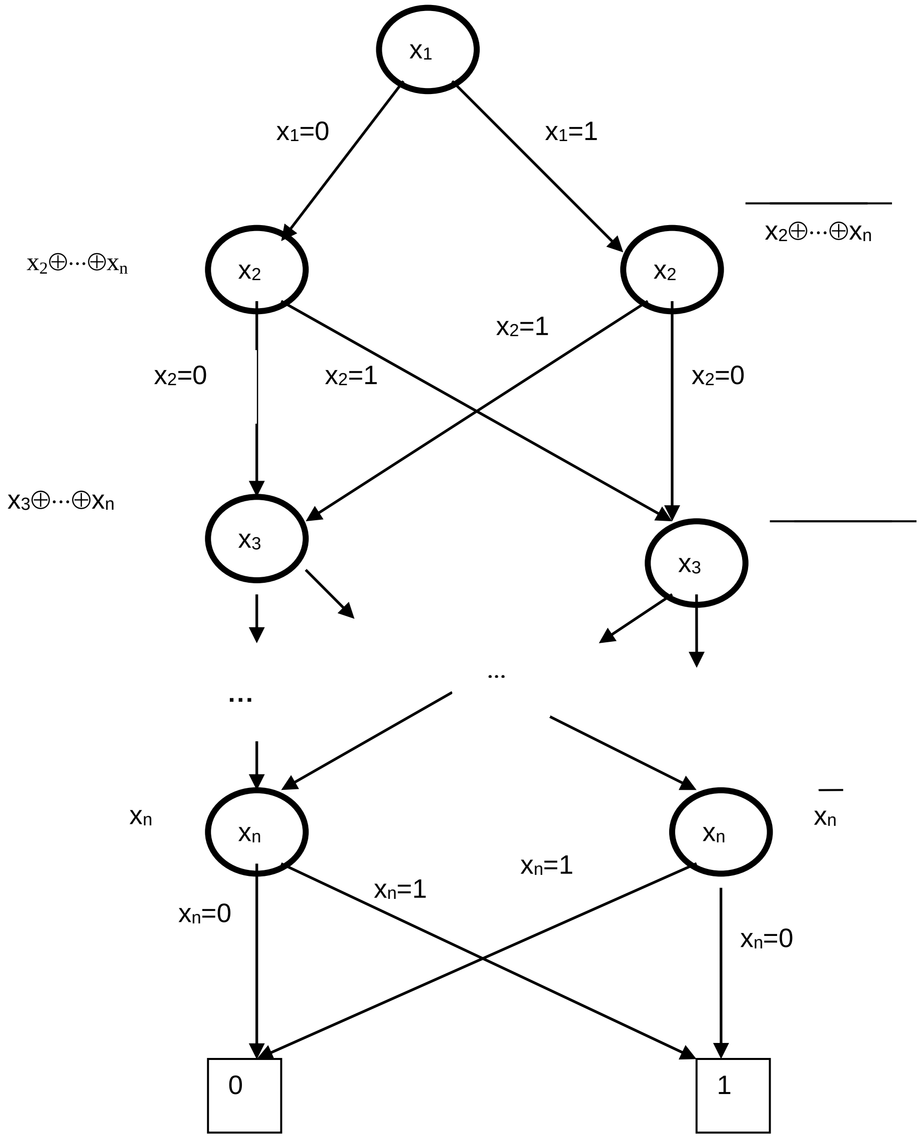
$x_1 \oplus x_2 \notin S$, as $\overline{\bar{x}_1 \oplus \bar{x}_2} = \overline{x_1 \oplus x_2} + x_1 \oplus x_2$;

$x_1 \oplus x_2 \notin M$, as $(0,1) \le (1,1)$ whereas $0 \oplus 1 = 1$, $1 \oplus 1 = 0$;

$x_1 \to \bar{x}_2 \notin L$, as $x_1 \to x_2 \equiv x_1 \oplus x_2 = x_1 x_2$, i.e. Zhegalkin polynomial contains sum of variables.

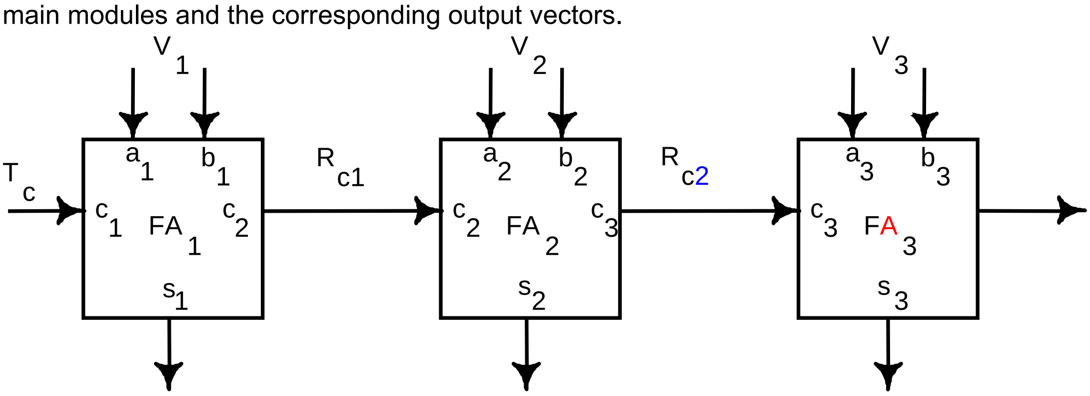
Therefore, the system is complete.

7b17.



7b18.

The figure depicts the corresponding modular form of an n-bit adder, as well as the input vectors of the main modules and the corresponding output vectors.



T_c	V_1
0	00
0	01
0	10
0	11
1	00
1	01
1	10
1	11

R_{c1}	V_2
0	00
0	01
0	10
1	00
0	11
1	01
1	10
1	11

R_{c2}	V_3
0	00
0	01
0	10
0	11
1	00
1	01
1	10
1	11

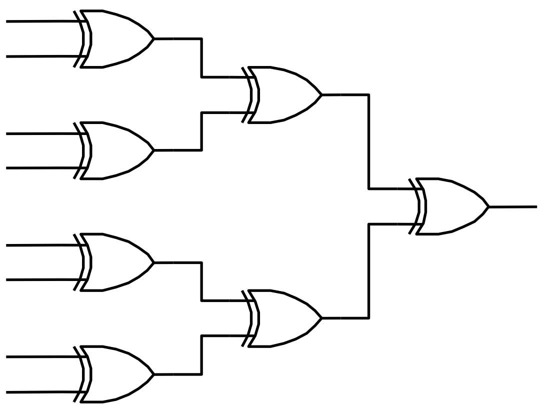
The input variables for module F_1 are the only variable c_1 of set T_c and the variables a_1, b_1 of set V_1. For modules F2, F3,etc, the input variables are c_2, c_3, etc., of group R_c, as well as the variables a_2, b_2, a_3, b_3, etc., of groups V_2, V_3, etc. The output variable c_{i+1} of module F_i is an input for the input variable c_{i+1} directly connected with the input variable of module F_{i+1}. The variables of groups T_c and V_i are independent, and the variables of groups R_c are dependent (not independent). The variables of groups T_c and R_{c1} take exhaustively all 8 possible values. The variables of groups R_{ci} and V_{i+1} also take exhaustively all 8 possible values.

Tc	V1	V2	V3
0	00	00	00
0	01	01	01
0	10	10	10
0	11	00	11
1	00	11	00
1	01	01	01
1	10	10	10
1	11	11	11

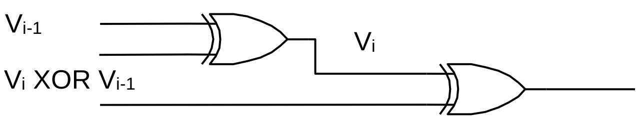
Thus, taking all 8 test vectors depicted in the figure it is possible to provide all 3 inputs for all modules F_i exhaustively all 8 test vectors which will exhaustively detect all possible faults on all input and output lines of module F_i.

7b19.

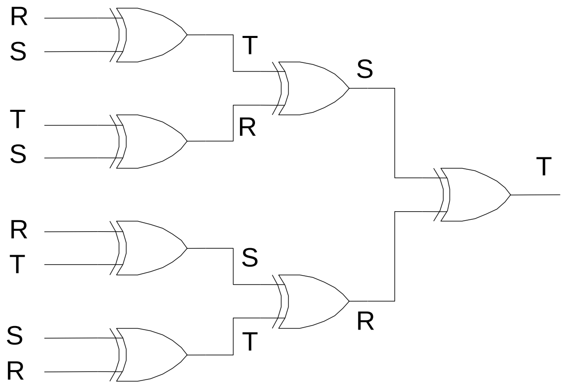
The figure depicts the corresponding circuit of an N-input parity tree.



In 1970, Bossen proved that is easily testable by means of only 4 test vectors. By taking the test consisting of 4 exhaustive tests for Modulo 2 logical element (gate XOR): { 00, 01, 10, 11}, and performing the following assignment for input vectors: R=1100, S=1010, T=0110, and after the following labeling in the parity tree it can be shown that for any V_i, V_j, $V_k \in \{R, S, T\}$, $V_i \neq V_j \neq V_k$ there is $V_i \oplus V_j = V_k$.



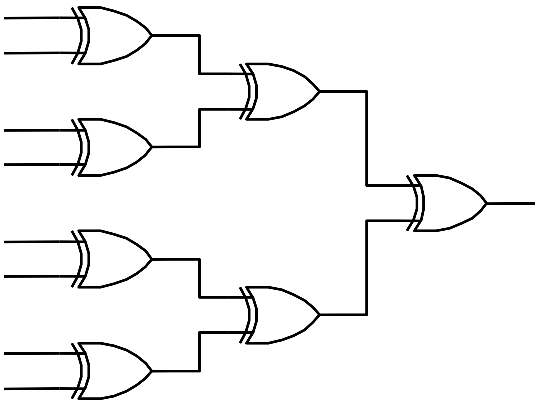
Then performing any labeling in the parity tree of the first figure, the next figure is obtained and it is possible to show that the whole parity tree can be tested by means of only 4 test vectors.



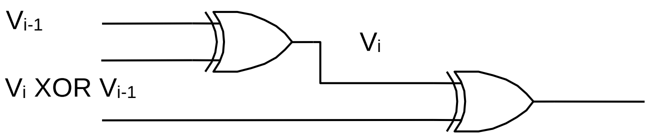
Vector	R	S	T	S	R	T	S	R
1	1	1	0	1	1	0	1	1
2	1	0	1	0	1	1	0	1
3	0	1	1	1	0	1	1	0
4	0	0	0	0	0	0	0	0

7b20.

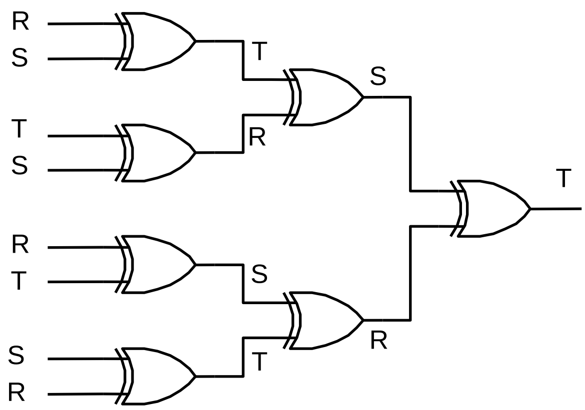
The figure depicts the circuit of N-input tree with negated Modulo 2 elements (gates NXOR).



By taking the exhaustive test consisting of 4 vectors for Modulo 2 element (gate NXOR): { 00, 01, 10, 11}, and performing the following assignment for input vectors: R=1010, S=0110, T=0011, and making the following labeling in our tree, the following is obtained:



and it is possible to show that for any V_i, V_j, $V_k \in$ {R, S, T}, $V_i \neq V_j \neq V_k$ there is $V_i \oplus V_j = V_k$. Then by performing any labeling in the tree of the figure:



It is possible to show that by means of only 4 test vectors the whole tree can be tested.

Vector	R	S	T	S	R	T	S	R
1	1	0	0	0	1	0	0	1
2	0	1	0	1	0	0	1	0
3	1	1	1	1	1	1	1	1
4	0	0	1	0	0	1	0	0

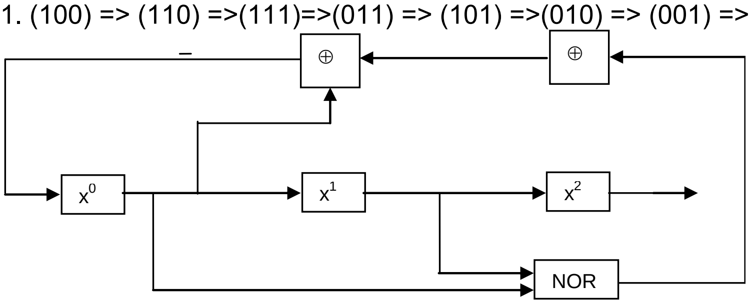
7b21.
The number of all faults is equal

$$\sum_{k=2}^{N}\binom{m}{k}2^{m} = 3^{N} - \binom{N}{0}2^{0} - \binom{N}{1}2^{1} = 3^{N} - 2N - 1.$$

Therefore, the number of all stuck-at-0 and stuck-at-1 faults will be
$3^{1000000} - 1999999$.

7b22.
2 subsets are obtained, the corresponding cycles of which include the following sets:
1. (100) => (110) =>(111)=>(011) => (101) =>(010) => (001) => (001)=>(100)
2. (000) =>(000)

7b23.
After adding NOR element, the obtained new circuit generates the only subset of the following patterns:
1. (100) => (110) =>(111)=>(011) => (101) =>(010) => (001) => (001)=>(000) =>(100).



7b24.
First, it is needed to construct the truth table.

x_1	x_2	x_3	$x_1 \oplus x_3^{x_1 \vee x_2}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Search Zhegalkin polynomial of mentioned function in the following form:

$f=a_0\oplus a_1x_1\oplus a_2x_2\oplus a_3x_3\oplus a_{12}x_1x_2\oplus a_{13}x_1x_3\oplus a_{23}x_2x_3\oplus a_{123}x_1x_2x_3$

The solution of the problem is to find coefficients in the presented form.
Function equals 1 with values 0,0,0 of arguments x1, x2, x3 . Placing these values on right side of equation:
$1= a_0$

For values 0,0,1 it will be
$0=1\oplus a_3$ therefore: $a_3=1$:

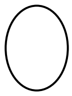
Substituting the right and left parts of the equation, sequentially all the possible values to x_1, x_2 and x_3 variables, the following will be obtained:

$0 = 1\oplus a_2$,	$a_2 = 1$,
$1 = 1\oplus 1\oplus 1\oplus a_{23}$,	$a_{23} = 0$,
$1 = 1\oplus a_1$,	$a_1 = 0$,
$0 = 1\oplus 1\oplus a_{13}$,	$a_{13} =1$,
$1 = 1\oplus 1\oplus a_{12}$,	$a_{12} =1$’
$0 = 1\oplus 1\oplus 1\oplus 1\oplus 1\oplus a_{23}$,	$a_{23} = 0$,

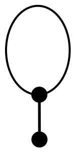
Putting the obtained values of the coefficients, Zhegalkin polynomial of the function will be obtained.

$$f=1\oplus x_2\oplus x_3\oplus x_1x_2\oplus x_1x_3\oplus x_1x_2x_3$$

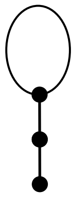
7b25.
There is some tree corresponding to 000101001111, mark it using the folowing symbol:



As the code cannot be divided into 2 parts, each containing equal number of 1s and 0s, the tree will have the following view:



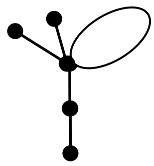
the ring code of which is 0010100111, which is derived from base code by removing 0 and 1 from each side.



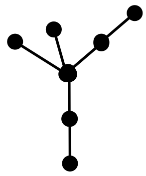
and 01010011.

Repeating this procedure to new code, the following will be obtained respectively:

In the next step, the code is divided to 01, 01 and 0011 parts and this will be obtained:



In the last step, as 0011 cannot be divided into 2 parts, this will be obtained:



7b26.

$$\omega_1^{x_1x_2\oplus(x_1\vee x_2x_3)}=\left\|x_2x_3\oplus(x_2\oplus 1)\right\|=\left\|x_2x_3\oplus\bar{x}_2\right\|=\left\|x_2x_3\right\|+\left\|\bar{x}_2\right\|=\frac{1}{4}+\frac{1}{2}=\frac{3}{4}$$

$$\omega_2^{x_1x_2\oplus(x_1\vee x_2x_3)}=\left\|x_1\oplus(x_1\oplus(x_1\vee x_3))\right\|=\left\|x_1\oplus x_1\oplus(x_1\vee x_3)\right\|=\left\|x_1\vee x_3\right\|=\frac{1}{2}+\frac{1}{2}-\frac{1}{4}=\frac{3}{4}$$

$$\omega_3^{x_1x_2\oplus(x_1\vee x_2x_3)}=\left\|(x_1x_2\oplus x_1)\oplus(x_1x_2\oplus(x_1\vee x_2))\right\|=\left\|(x_1x_2\oplus x_1\oplus x_1x_2\oplus(x_1\vee x_2))\right\|=$$

$$=\left\|(x_1\oplus(x_1\vee x_2))\right\|=\frac{1}{2}+\frac{3}{4}-2\left\|(x_1\oplus(x_1\vee x_2))\right\|=\frac{1}{2}+\frac{3}{4}-1=\frac{1}{4}$$

7b27.

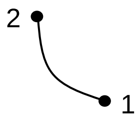
As the code length equals 7, therefore the number of tree nodes equals 9. The numbers of those nodes and tree code are:

1, 2, 3, 4, 5, 6, 7, 8, 9:

From those numbers choose the number from left to right which is missing in the code. It is 1. Connect the node of that number with number one node of the code from the left (which is 2) and delete those two numbers. The following will be obtained:

3, 3, 4, 5, 5, 8

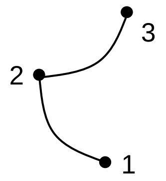
2, 3, 4, 5, 6, 7, 8, 9:



Apply the same process sequentially towards the obtained results, connect the node of 3 number with the node 3. The following will be obtained:

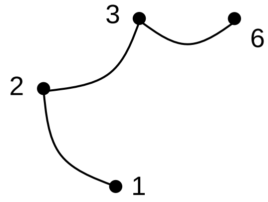
3, 4, 5, 5, 8

3, 4, 5, 6, 7, 8, 9

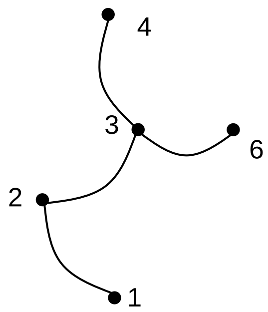


Continuing this action until deleting all the numbers in the code, this is sequentially obtained:

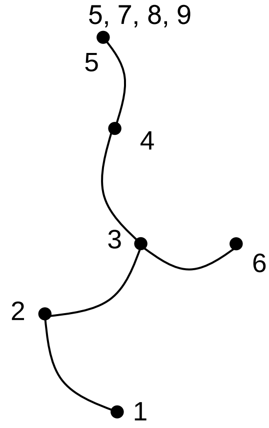
4, 5, 5, 8
3, 4, 5, 7, 8, 9



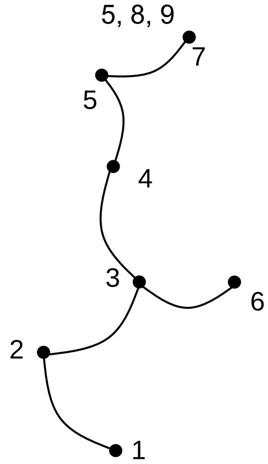
5, 5, 8
4, 5, 7, 8, 9



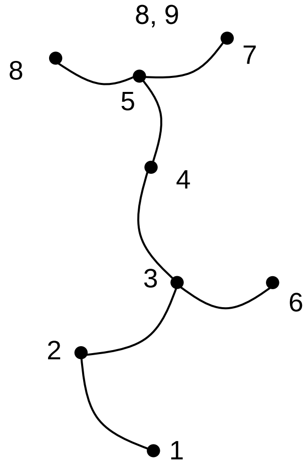
5, 8
5, 7, 8, 9



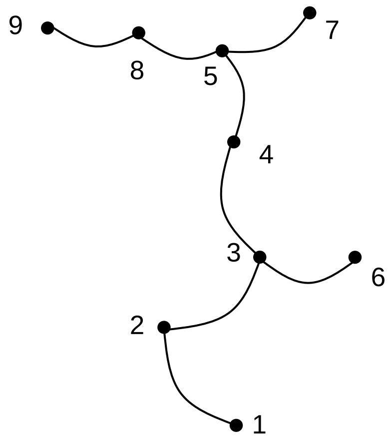
8
5, 8, 9



8, 9



Finally, the remaining 8 and 9 nodes are connected to each other.



7b28.
Let F1 be the fault “line A stuck-at-1”, F2 be “line B stuck-at-1” and F3 be “line Z* be stuck-at-1”. Then it is easy to check that F1 = F2 = F3 since F1={(00)}, F2={(00)}, F3={(00)}.

7b29.
According to McCluskey, the number of input patterns for the pseudoexhaustive test is $2^{n1} + 2^{n2} + \ldots + 2^{n5} = 2^{12} + 2^{14} + 2^{16} + 2^{18} + 2^{20} = 2^{12}(1+4+16+64+256) = 341.\ 2^{12} = 1396736$.

7b30.
Since T(F1)={(0,0)}, T(F2)={(0,0)}, T(F3)={(0,0)}, then T(F1) = T(F2) = T(F3).

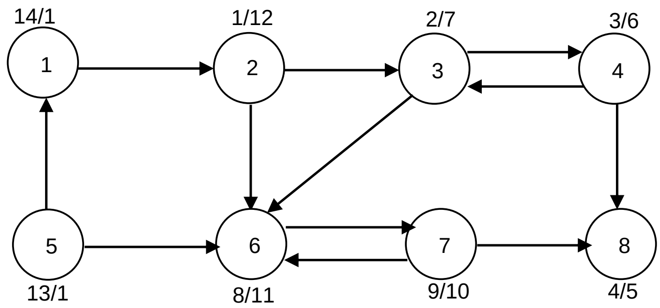
7b31.
Denote by F1 the fault ”line A stuck-at-0”, F2 – “line B stuck-at-0” and F3 – “line Z stuck-at-0”. Prove that single faults F1, F2 and F3 are equivalent.
Since T(F1)={(1,1)}, T(F2)={(1,1)}, T(F3)={(1,1)}, then T(F1) = T(F2) = T(F3).

7b32.
Search strategy is the following:
1) Starting from the 2nd vertex, go deeper in any path as it is still possible.
2) Return by searching other paths.
3) Repeat the 1st and the 2nd steps until detecting all possible vertices.
4) If there are still undetected vertices, select one of them and repeat 1-3 steps.

5) Repeat 1-4 steps until detecting all the vertices of the graph.

Mark the numbers of detection and completion steps on vertices.

Answer



7b33.

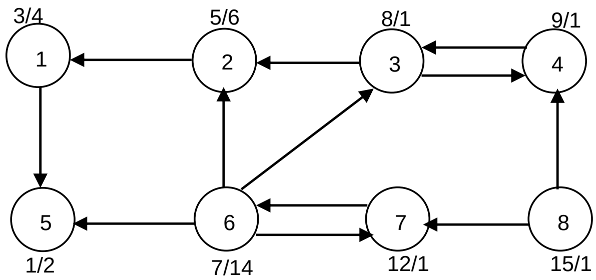
Separate strongly connected components in the given directed graph.

Solution:

1) Search according to depth starting with any vertex.
2) Construct the transported graph of the given graph.
3) Search according to depth in transported graph. In each cycle, start from the vertex with the highest value of process completion.

Each search cycle will separate strongly connected components.

Answer: Observe the solution on the previous example.



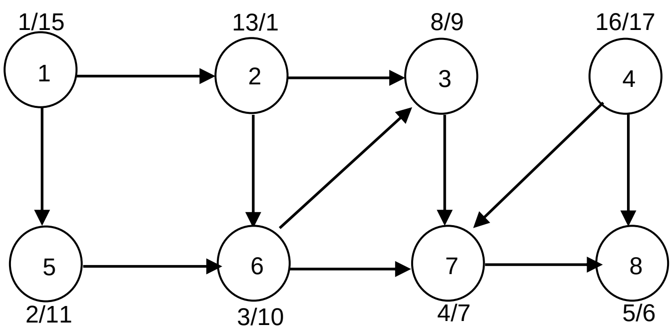
In the previous example, the completions of vertex processing according to decrease are the following: 5, 1, 2, 6, 7, 3, 4, 8.

Therefore the search will start from 5th vertex.

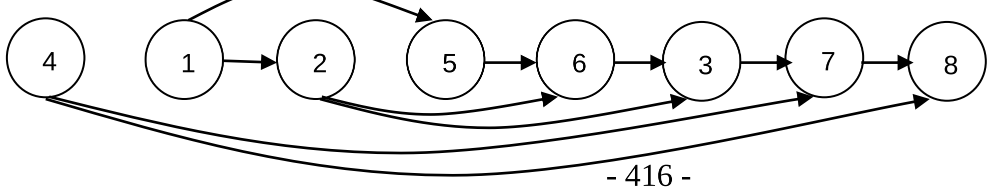
The strongly connected components will be a) 5; b) 1; c) 2; d) 3, 4, 6, 7; e) 8

7b34.

1) Search according to density, starting from any vertex.
2) Classify the vertices from left to right, according to the decrease of ends of vertex processing.



Answer



7b35.
The objective function will be $f = 2f_1 + f_2$.
Answer:

7	5	6	7	8	9	10	11
6	4	5	6	7	8	11	12
5	3	6	7		9	12	11 B
4	2	3	4		8	11	10
3	1	2	3	6	7		9
2	0	1	2	5	6	7	8
1	1	2	3	6	7		9
	1	*2*	*3*	*4*	*5*	*6*	*7*

7b36.
The matrix of orthogonal distances is built, calculating the orthogonal distance between contacts.

$l_{a,b} = | 2\text{-}8 | + | 9\text{-}8 | = 7$;

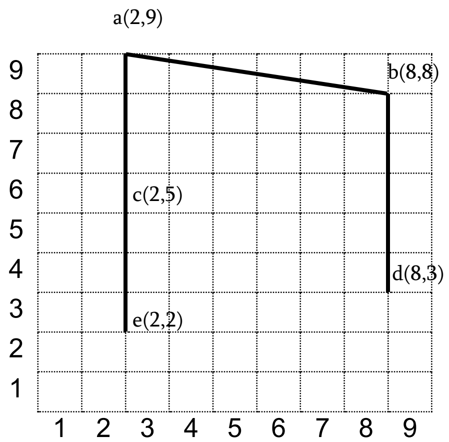
$l_{ac} = 4$; $l_{ad} = 13$; $l_{ae} = 7$:
$l_{bc} = 9$; $l_{bd} = 5$; $l_{be} = 12$; $l_{cd} = 8$;
$l_{ce} = 3$; $l_{de} = 7$

The matrix will have the following view:

	a	b	c	d	e
a	0	7 v	4 v	12	7
b	7	0	9	5 v	12
c	4	9	0	8	3 v
d	12	5	8	0	7
e	7	12	3	7	0
	2	3	1		

d ⟵ b ⟵ a ⟵ c ⟵ e

Answer:



7b37.
The adjacency matrix and the solution process are the following:

	1	2	3	4	5	6	f_0	f_1		
1	0	1	0	2	1	0	4	X	X	
2	1	0	1	0	0	2	4	2	2	
3	0	1	0	1	0	0	2	2	0	X
4	2	0	1	0	0	0	3	-1	X	
5	1	0	0	0	0	2	3	1	1	

6	0	2	0	0	2	0	4	4	4	

Answer:
1st group - 1, 3, 4;
2nd group - 2, 5, 6.

7b38.

The adjacency matrix and the solution process are the following:

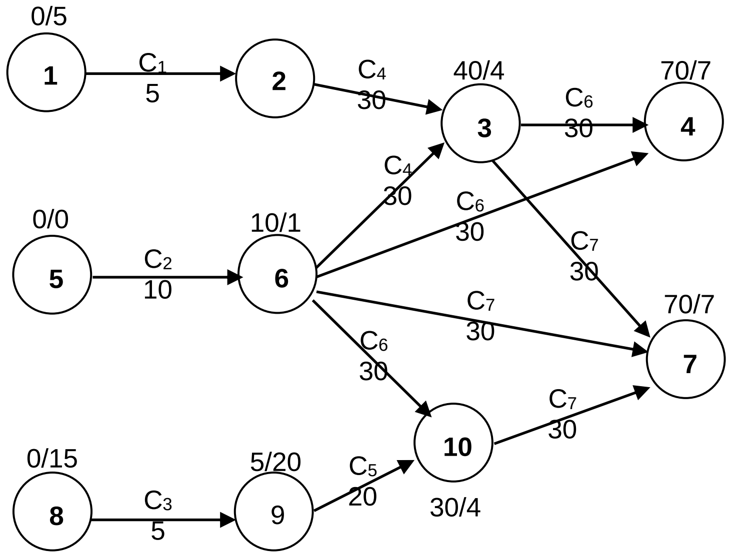
	l_1	l_2	l_3	l_4	l_5	f_0	f_1	f_2	f_3	f_4
l_1	0	0	1	1	0	$\underline{2}$	X	X	X	X
l_2	0	0	1	1	0	2	2	$\underline{0}$	X	X
l_3	1	1	0	0	1	3	$\underline{1}$	X	X	X
l_4	1	1	0	0	1	3	1	1	$\underline{-1}$	X
l_5	0	0	1	1	0	2	2	0	0	

Answer:

$l_1 \longrightarrow l_3 \longrightarrow l_2 \longrightarrow l_4 \longrightarrow l_5$

7b39.

Timing graph and calculation process are the following:



Answer:

The critical paths are two and have 70 unit of delay.

a) $5 \rightarrow 6 \longrightarrow 3 \longrightarrow 4$ b) $5 \rightarrow 6 \rightarrow 3 \rightarrow 7$

7b40.
See the solution of 7b24.

7b41.
See the solution of 7b25.

7b42.
See the solution of 7b26.

7b43.

$f(x_1,x_2,x_3)= x_1,x_2 \vee x_3$, as $\xi_1 + \xi_2 = 7 > 5$ and $\xi_3 = 6 > 5$. Construct the table for perfect disjunctive normal form of the function.

x_1	x_2	x_3	$x_1\ x_2 \vee x_3$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Perfect disjunctive normal form of the function will be:

$$f(x_1, x_2, x_3) = \overline{x_1}\,\overline{x_2}\,x_3 \vee \overline{x_1}x_2x_3 \vee x_1\overline{x_2}x_3 \vee x_1x_2\overline{x_3} \vee x_1x_2x_3$$

7b44.

To check the completeness of the system, use Post theorem. It is obvious that $\overline{x_1} \to x_2$ function preserves 0 constant $\overline{0} \to 0 = 1 \to 0 = 0$. The other functions of the system also preserve 0 constant: 0•0=0 and $0 \vee 0 = 0$.

Therefore, the system is fully included in the class that preserves 0 constant functions. Hence, according to Post theorem, it follows that the system is not complete.

7b45.

Zhegalkin polynomial is searched in the form of indefinite coefficients:

$$f(x_1,x_2,x_3) = a_0 \oplus a_1x_1 \oplus a_2x_2 \oplus a_3x_3 \oplus a_{12}x_1x_2 \oplus a_{13}x_1x_3 \oplus a_{23}x_2x_3 \oplus a_{123}x_1x_2x_3$$

The table of the function looks as follows:

X_1	X_2	X_3	$F(x_1,x_2,x_3)$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

On the right and left parts of the equation, giving the mentioned values to x_1, x_2 and x_3 variables sequentially, the following will be obtained:

$1 = a_0$

$1 = 1 \oplus a_3,\ a_3 = 0$

$0 = 1 \oplus a_2,\ a_2 = 1$

$0 = 1 \oplus 1 \oplus a_{23},\ a_{23} = 0$

$1 = 1 \oplus a_1,\ a_1 = 0$

$0 = 1 \oplus a_{13},\ a_{13} = 1$

$1 = 1 \oplus 1 \oplus a_{12},\ a_{12} = 1$

$1 = 1 \oplus 1 \oplus 1 \oplus 1 \oplus a_{123},\ a_{123} = 1$

Putting the obtained values of the coefficients in the formula, presented by indefinite coefficients, Zhegalkin polynomial of the function will be obtained:

$$f(x_1,x_2,x_3) = 1 \oplus x_2 \oplus x_1x_2 \oplus x_1x_3 \oplus x_1x_2x_3$$

7b46.

$$\omega_1^{(x_1 \vee \overline{x_2}) \oplus (x_1 \vee \overline{x_3}x_4)} = \left\|(\overline{x_2} \oplus \overline{x_3}x_4) \oplus (1 \oplus 1)\right\| = \left\|(\overline{x_2} \oplus \overline{x_3}x_4)\right\| = \left\|\overline{x_2}\right\| + \left\|\overline{x_3}x_4\right\| - 2\left\|\overline{x_2}\,\overline{x_3}x_4\right\| = \frac{1}{2} + \frac{1}{4} - \frac{1}{4} = \frac{1}{2}$$

$$\omega_2^{(x_1 \vee \overline{x_2}) \oplus (x_1 \vee \overline{x_3}x_4)} = \left\|1 \oplus (x_1 \vee \overline{x_3}x_4) \oplus x_1 \oplus (x_1 \vee \overline{x_3}x_4)\right\| = \left\|\overline{x_1}\right\| = \frac{1}{2}$$

$$\omega_3^{(x_1 \vee \overline{x_2}) \oplus (x_1 \vee \overline{x_3}x_4)} = \left\|(x_1 \vee \overline{x_2}) \oplus (x_1 \vee x_4) \oplus (x_1 \vee \overline{x_2}) \oplus x_1\right\| = \left\|(x_1 \vee x_4) \oplus x_1\right\| = \left\|x_1 \vee x_4\right\| + \left\|x_1\right\| - 2\left\|x_1\right\| =$$

$$= \frac{3}{4} + \frac{1}{2} - 1 = \frac{1}{4}$$

$$\omega_4^{(x_1 \vee \overline{x_2}) \oplus (x_1 \vee \overline{x_3}x_4)} = \left\|(x_1 \vee \overline{x_2}) \oplus x_1 \oplus (x_1 \vee \overline{x_2}) \oplus (x_1 \vee \overline{x_3})\right\| = \left\|x_1 \oplus (x_1 \vee \overline{x_3})\right\| = \left\|x_1\right\| + \left\|x_1 \vee \overline{x_3}\right\| - 2\left\|x_1\right\| =$$

$$= \frac{1}{2} + \frac{3}{4} - 1 = \frac{1}{4}$$

7b47.

It is clear that $x_1^{x_3} \to x_2^{x_1} \in T_0$ and $x_1 \oplus x_2 \in T_1$. It is also clear that $x_1x_2 \notin S$, as no function of two variables is self-dual. Then $x_1 \oplus x_2 \notin M$, as (0,1) precedes (1,1), but $0 \oplus 1 = 1$ and $1 \oplus 1 = 0$, i.e. the monotony condition is violated, therefore $x_1 \oplus x_2 \notin M$. It is also obvious that $x_1x_2 \notin L$. Therefore, according to Post's theorem, the mentioned system is complete.

7b48.

It is obvious that the threshold function with $\xi_1 = 2, \xi_2 = 3, \zeta_3 = 4,$ $W = 4$ parameters has $x_1x_2 \vee x_3$ formula, as $\xi_1 + \xi_2 > W$ and $\zeta_3 = w$.

$$\omega_1^{x_1x_2\vee x_3} = \left\|(x_1x_2 \vee x_3) \oplus (\overline{x_1}x_2 \vee x_3)\right\| = \left\|x_3 \oplus (x_2 \vee x_3)\right\| = \|x_3\| + \|x_2 \vee x_3\| - 2\|x_3(x_2 \vee x_3)\| =$$

$$= \frac{1}{2} + \frac{3}{4} - 2\|x_3\| = \frac{1}{2} + \frac{3}{4} - 1 = \frac{1}{4}$$

Due to symmetry it is clear that $\omega_2^{x_1x_2\vee x_3} = \frac{1}{4}$.

$$\omega_3^{x_1x_2\vee x_3} = \left\|\overline{x_1x_2}\right\|\omega_3^{x_3} = 1 - \frac{1}{4} = \frac{3}{4}.$$

7b49.

As $\xi_1 = 2, \xi_2 = 3, \xi_3 = 4, \xi_4 = 5,$ W=8 and $\xi_2 + \xi_4 = W,$ $\xi_3 + \xi_4 > W,$ $\xi_1 + \xi_2 + \xi_3 > W,$ the threshold function will have the following disjunctive normal form:

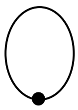
$$x_2x_4 \vee x_3x_4 \vee x_1x_2x_3.$$

As $a \vee b = a \oplus b \oplus ab,$ Zhegalkin polynomial of the obtained function will be got in the following way:

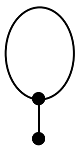
$$x_2x_4 \vee x_3x_4 \vee x_1x_2x_3 = x_2x_4 \oplus x_3x_4 \oplus x_2x_3x_4 \vee x_1x_2x_3 = x_2x_4 \oplus x_3x_4 \oplus x_2x_3x_4 \oplus x_1x_2x_3 \oplus$$
$$\oplus x_1x_2x_3x_4 \oplus x_1x_2x_3x_4 \oplus x_1x_2x_3x_4 = x_2x_4 \oplus x_3x_4 \oplus x_2x_3x_4 \oplus x_1x_2x_3 \oplus x_1x_2x_3x_4$$

7b50.

Some tree corresponds to 000100011111, which is conventionally denoted by

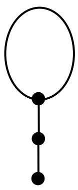


symbol. As the code cannot be divided into 2 such parts each of which containing equal number of 0s and 1s, it would have the following view: the code of



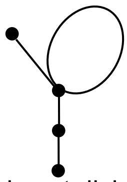
part of the ring would be 0010001111. It is obtained from the main code by removing 0 and 1 from its left and right.

Performing the same action towards the obtained new code, the following will be obtained correspondingly:

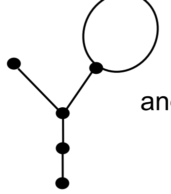


and 01000111.

In the next step the code is divided into 01 and 000111 parts and the following is obtained:

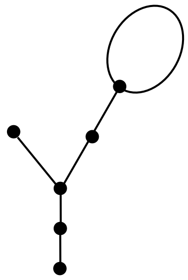


In the recurrent step 000111 is not divided into 2 parts, therefore the following result will be obtained:

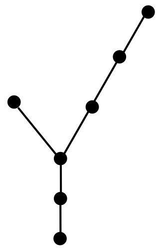


and 0011.

Continuing, the following will be obtained:



and 0011



as 0011 is not divided into 2 parts.
Finally, final result will be in the last step:

7b51.
All the solutions should satisfy the following equation:
$g(x)df(x,g(x))/dg(x)=g(x)[f(x,g=0) \oplus f(x,g=1)]=g(x)(x_3 \oplus 1) = x_1 x_2 \bar{x}_3 = 1$:
The equation has only one solution - T = {(110)}.
7b52.
All the solutions should satisfy the following equation:
$\overline{g(x)}\, df(x,g(x))/dg(x) = \overline{g(x)}\,[f(x,g=0) \oplus f(x,g=1)] = \overline{g(x)}\,(x_3 \oplus 1) = (\bar{x}_1 \vee \bar{x}_2)\bar{x}_3 = \bar{x}_1 \bar{x}_3 \vee \bar{x}_2 \bar{x}_3 = 1$.
The equation has three solutions, i.e.
T = {(000), (010),(100)}.
7b53.
The number of all possible, two and more, faults equals to
$$S = \sum_{m=2}^{N} 2^m C_N^m = \sum_{m=0}^{N} 2^m C_N^m - 2N - 1 = 3^N - 2N - 1$$
.
7b54.
The number of all possible, three and more, faults equals to
$$S = \sum_{m=2}^{N} 2^m C_N^m = \sum_{m=0}^{N} 2^m C_N^m - \sum_{m=0}^{1} 2^m C_N^m = 3^N - 2N^2 - 2{,}5N - 1$$
.
7b55.
The recalculation coefficient of the counter is equal to 5. The output of NOR cell functions as the 5th output. When pulses are given from generator, logic 1 moves through 5 outputs of the counter. Appearance of logic 1 in 0, 1, 2, 4 and 8 outputs of the decoder corresponds to the states of the counter. Therefore, the pulse frequency in the 2nd output of the decoder will be 5 times smaller than the frequency of the generator.

7b56.
The given logic function is represented in Perfect Disjunctive Normal Form (DNF) and takes 1 value for three sets of A, B, C input variables - sixth, fifth and third (the numbers of sets are obtained by means of summation of weight coefficients of address inputs of multiplexers that correspond to direct values of variables. Logic zeros should be given to those information inputs of multiplexers because the function is formed in inverse output. Therefore the answer will be 10010111.

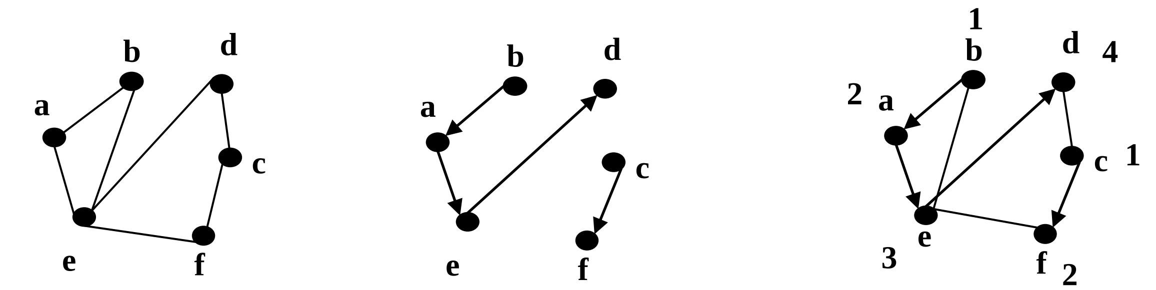
7b57.
By summing 48H and 29H numbers, given to A and B inputs of the circuit, 48H+29H=71H number will be obtained in the output of the adder. High rank of the obtained number will be given to the left indicator from internal decoder, and low rank – to the right indicator. Thus, number 71 will be depicted on the indicator.

7b58.
The adjacency matrix of the given circuit and solution process is shown in the table.

	e1	e2	e3	e4	e5	f_0	f_1	f_2	f_3	f_4
e1	-	1	0	0	0	1	X	X	X	X
e2	1	-	1	2	0	4	4-2*1=2	X	X	X
e3	0	1	-	2	1	4	4-2*0=4	4-2*1=2	2-2*2=-2	X
e4	0	2	2	-	1	5	5-2*0=5	5-2*2=1	X	X
e5	0	0	1	1	-	2	2-2*0=2	2-2*0=2	2-2*1=0	

The element with maximum connections with already selected elements and minimum connections with not yet selected elements is chosen in each step. This is the key requirement for calculation. The calculation is carried out by the following recurrent formula:
$f_{ij}=f_{(i-1)j}-2*r_{jk}$,
where f_{ij} is f pretender function value in i-th step of calculation for j-th element. r_{jk} is the number of connections of j-th element with k-th element, selected in (i-1)-th step. As a recurrent element, the element with min f_{ij} is chosen in each step. If they are more than one, anyone can be chosen.
As seen from the table, initial row placement of the given circuit will have the following sequence: e1 →e2→ e4 →e3→ e5.

7b59.
Build the graph of horizontal and vertical constraints of a, b, c, d, e, f nets. Build the combined graph and heuristically define its chromatic number as shown in the figure below. Besides, bottom-up numbering of horizontal paths is conditional. Hence it follows that the numbers in the beginning of directed edges that correspond to vertical constraints should be smaller than the numbers in the end of the edges.

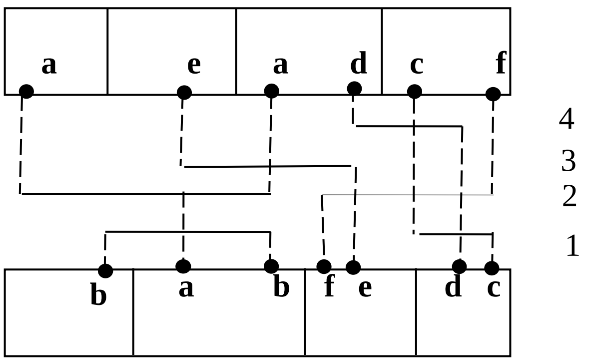


a) A graph of horizontal constraints

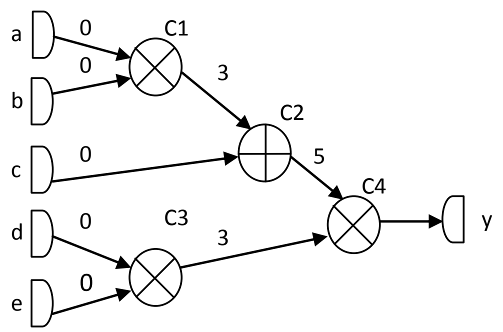
b) A graph of vertical constraints

c) A combined graph

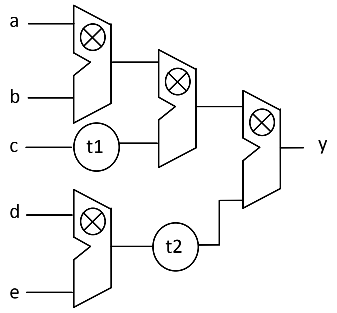
As seen from the figure, the chromatic number of the graph is equal to 4. Hence it follows that at least 4 horizontal channels are needed for two-layer orthogonal mounting of the given nets.



7b60.
Data Flow Graph of the circuit is shown in the figure. The earliest times of data appearance are shown on the edges. As seen from the figure, there is signal racing in the inputs of C2 and C4 elements with 3 and 2 c.u. sizes respectively. Therefore to exclude signals racing, delay elements are to be added before corresponding inputs.

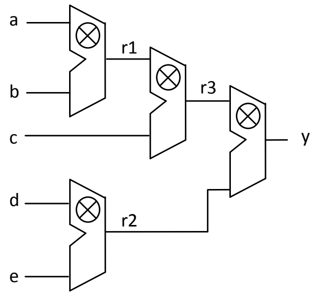


The functional circuit of the device together with delay elements is shown in the figure. t1and t2 delay elements are with 3 c.u. and 2 c.u. respectively.



7b61.

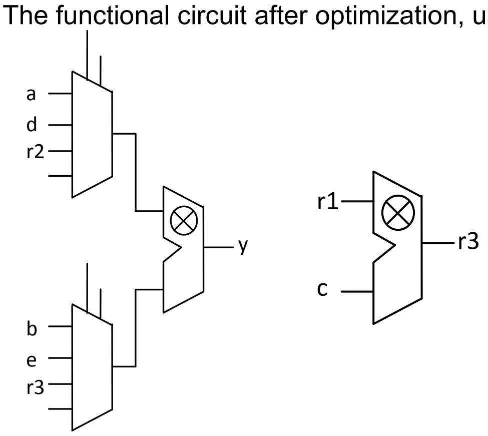
The functional circuit without using multiplexers, will be:



The operating cycles of the circuit and the actions, taken at each cycle are presented in the table.

Functional unit	Quantity	Cycle 1	Cycle 2	Cycle 3
⊗	3	r1=a*b, r2=d*e	-	y=r2*r3
⊕	1	-	r3=r1+c	-

The functional circuit after optimization, using multiplexers, will be:

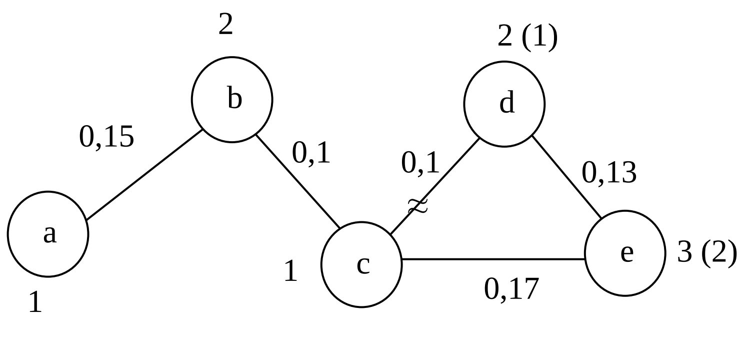


The operating cycles of the optimized circuit and the actions, taken at each cycle are presented in the table.

Functional unit	Quantity	Cycle 1	Cycle 2	Cycle 3
⊗	1	r1=a*b	r2=d*e	y=r2*r3

$\oplus$	1	-	r3=r1+c	-

7b62.
The weighted graph of nets overlap will have the following form:



The chromatic number of the graph will be equal to 3, therefore the internal boundary of needed metal layers, necessary for net routing, will be 3.

The weights of graph edges are calculated by the formula, presented in the condition of the task.

As seen from the weights of edges, from the perspective of providing maximum routability, (b,c) and (c,d) pairs are of equal nets. But the union of (b,c) pair in the same level does not change the chromatic number of the graph, and the union of (c,d) pair in the same level allows reducing the chromatic number of the graph by one (new numbers are shown in brackets). So, (a,c,d) nets will be executed in the 1st level, and (b,e) nets in the 2nd one.

7b63.
The left part of the equation tends to zero faster than first order x. Hence, the equation has a solution if and only if $f(x)=x^2\varphi(x)$, where φ is integrable function. Denote $v(x)=\int_0^x y(t)dt$. Then the equation will represented in the form:

$$xv'(x)-v(x)=x^2\varphi(x).$$

Let $v(x)=xw(x)$. The equation is reduced to the form $x^2w'(x)=x^2\varphi(x)$. The following is obtained:

$$w(x)=\int_0^x \varphi(t)dt+C,$$

therefore, $v(x)=x\int_0^x \varphi(t)dt+Cx$ and the solution y is determined by the formula $y(x)=x\varphi(x)+\int_0^x \varphi(t)dt+C$.
Thus, the solution is not unique and the corresponding homogeneous problem (for $f\equiv 0$) has one linearly independent solution.

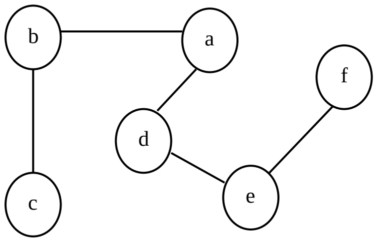
7b64.
Divide both parts of the equation by |x-y| and proceed to the limit for $y\to x$. Then, using the definition of the derivative, the function f is differentiable and $f'(x)=0$ for all x. Using connectivity of the interval [a,b], f=const is obtained.

7b65.
Suppose that the equation has not less than three solutions. Then by Roll's theorem, the derivative of the left part of equation $(x^n+ax+b)'=nx^{n-1}+a$ will have no less than two roots, what is impossible because n is even. For odd n this derivative may have no more than two roots, therefore, the equation has no more than two roots, what is contradiction.

7b66.

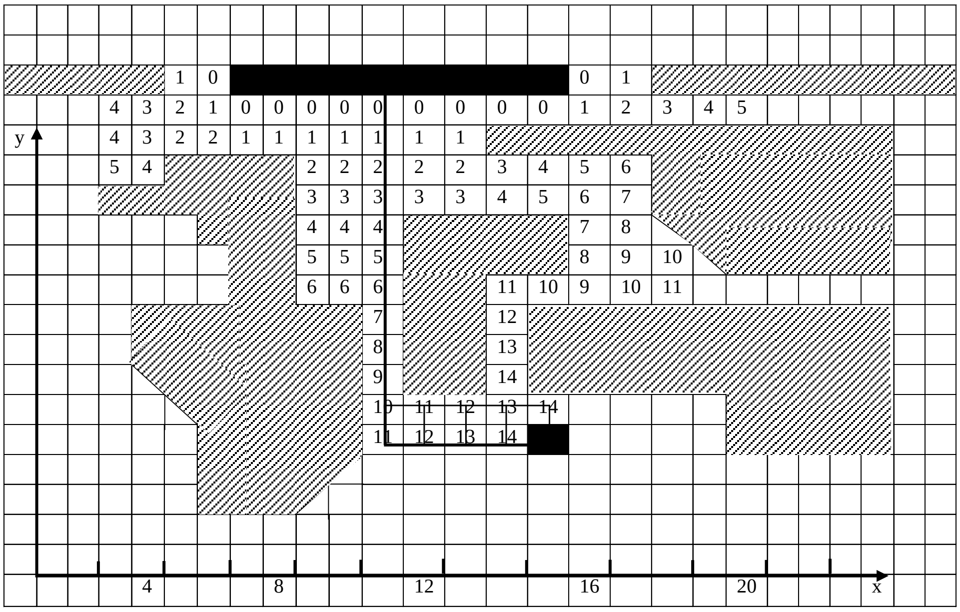
Differentiate both parts of the equality by y and substitute y=0. $f'(x) = f'(0)f(x)$ is obtained. Denoting $f'(0) = k$ and solving this differential equation, find $f(x) = Ce^{kx}$, where C is an arbitrary constant.

7b67.



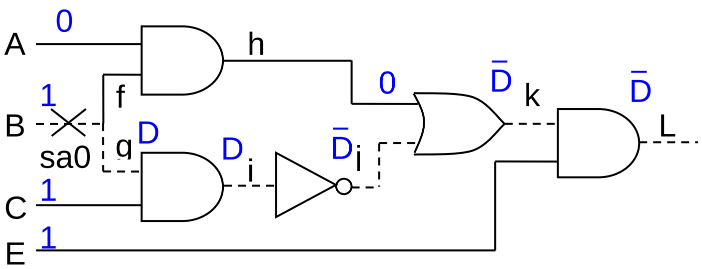
z	$L_{min}(d,a)$	$L_{min}(d,b)$	$L_{min}(d,c)$	$L_{min}(d,e)$	$L_{min}(d,f)$
a	2	5	7	3	∞
e		4	7	3	6
b		4	7		5
f			6		5
			6		

7b68.

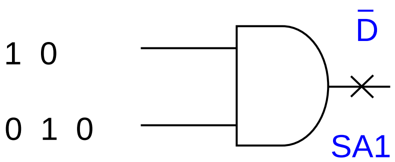


7b69.

The sensitive path is marked with red in the figure below.



7b70.



PDCF PDCF PDCF

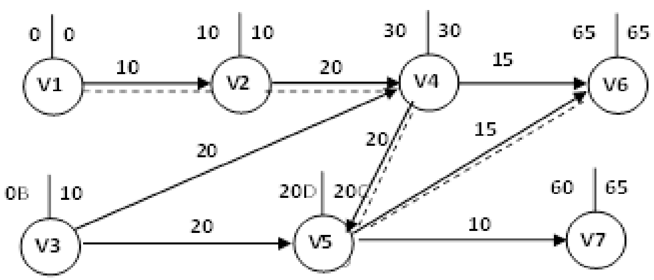
{0,0,D̄} {0,1,D̄} {1,0,D̄}

7b71.
The initial set of faults is: {a/0, a/1, b/0, b/1, c/0, c/1, d/0, d/1, e/0, e/1, f/0, f/1, g/0, g/1, h/0, h/1, i/0, i/1, j/0, j/1, k/0, k/1, z/0, z/1}: According to the mentioned theorem, the test set of mentioned type can be restricted by considering the corresponding faults on checkpoints. After reduction the following set of faults is obtained; {a/0, a/1, b/0, b/1, c/0, c/1, d/0, d/1, e/0, e/1, , f/0, f/1, h/0, h/1, i/0, i/1}:
Thus, instead of consideration of the initial set of 28 faults, only 16 is considered. The initial set is reduced by 57.14 %.

7b72.
(1, 1, 1) and (0, 0, 0)

7b73.
As the given expression can be substituted by the following equivalent expression: $C\cdot\overline{(A+B)} = C\cdot\overline{A}\cdot\overline{B}$, it is obvious that the answer should be the part of cycle C which excludes parts, belonging to cycles A and B. So the answer is the 7th segment.

7b74.
The timing graph of the circuit will have this form:



The earliest times of signal formation are at the top left side, and the latest times – on the right side of vertices corresponding to circuits. Time savings are defined by the difference of the latest and the earliest times and for the circuits from V1 to V7 will be 0, 0, 10, 0, 0, 0, 5 respectively. The critical path is shown in dotted line, and its delay is equal to 65.

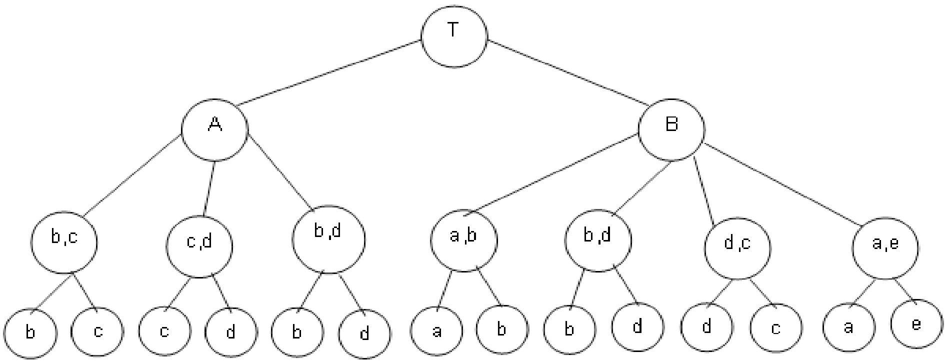
7b75.
The adjacency matrix of the given circuit and the solution process are presented in the table:

	e1	e2	e3	e4	e5	e6	f0	f1	f2	f3
e1	-	1	0	2	2	0	5	5-2*2=1	X	X
e2	1	-	2	0	0	1	4	4-2*0=4	4-2*1=2	
e3	0	2	-	0	0	2	4	4-2*0=4	4-2*0=4	
e4	2	0	0	-	1	0	3	X	X	X
e5	2	0	0	1	-	2	5	5-2*1=3	3-2*2=-1	X
e6	0	1	2	0	2	-	5	5-2*0=5	5-2*0=5	

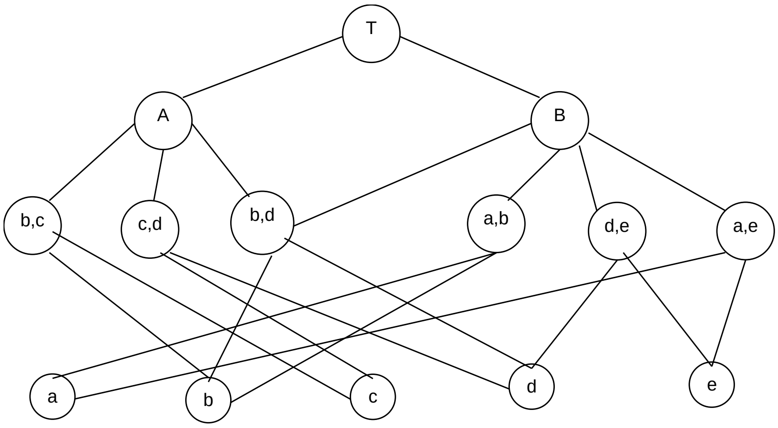
Vertices (e1, e4, e5) will be in one of the parts and (e2, e3, e6) will be in another one.
The veritice with maximum connections with already selected vertices and minimum connections with not yet selected vertices is chosen in each step. This is the key requirement for calculation. The calculation is carried out by the following recurrent formula:
$f_{ij}=f_{(i-1)j}-2*r_{jk}$,
where f_{ij} is f pretender function value in i-th step of calculation for j-th element. r_{jk} is the number of connections of j-th element with k-th element, selected in (i-1)-th step. As a recurrent element, the element with min f_{ij} is chosen in each step. The process continues until the group is formed. In the given example, the group is formed in 3 steps as the 6 vertices of the graph should be partitioned into 2 equal parts.

7b76.
Representing P topological image as a sum of two simpler A and B images, which in their turn are composed of separate sides, and the sides are composed of end-points the coordinates of which are

given, it is possible to construct hierarchic and set graph models of data representation, illustrated in Figures a) and b) respectively.



a) Hierarchic graph model



b) Set graph model

7b77.

First find the logarithm of two sides of the equation:

$$\log f(x)+\log f(-x)=2\log|c|$$

or

$$\log f(x)-\log|c|=-\log f(-x)+\log|c|=-(\log f(-x)-\log|c|).$$

This equality shows that the function $F(x)=\log f(x)-\log|c|$ is odd. So $f(x)=|c|e^{F(x)}$, where F is arbitrary odd function.

7b78.

Changing the places of s and t, the following is obtained:

$$e^{as}f(t)=f(t+s)-f(s),\ \ e^{at}f(s)=f(t+s)-f(t).$$

Subtracting the second equation from the first one, this is obtained:

$$e^{as}f(t)-f(t)=e^{at}f(s)-f(s),$$

or

$$\left(e^{as}-1\right)f(t)=\left(e^{at}-1\right)f(s).$$

It should be noted that from the conditions of the problem it follows that $f(0)=0$. If $ts\neq 0$, then

$$\frac{f(t)}{e^{at}-1}=\frac{f(s)}{e^{as}-1}:$$

Noting, that there are functions of different variables on the two sides of equation, the final form of the function f is found:

$$f(t) = c\left(e^{at} - 1\right).$$

7b79.

The convergence of the sequence is followed from the lemma of nested segments. Reduce the recurrent formula to the following form:

$$x_n - x_{n-1} = -\frac{1}{n}\left(x_{n-1} - x_{n-2}\right),$$

and denote $y_n = x_n - x_{n-1}$. Then $y_n = -\frac{1}{n} y_{n-1}$ is obtained, and hence,

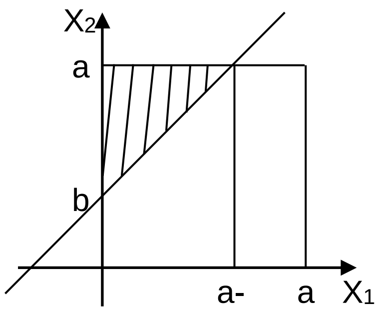
$$y_n = -\frac{1}{n} y_{n-1} = \left(-\frac{1}{n}\right)\left(-\frac{1}{n-1}\right) y_{n-2} = \ldots = \frac{(-1)^{n-1}}{n!} y_1 .$$

Further, there is $x_n = x_0 + \sum_{k=1}^{n} y_k$, therefore

$$\lim_{n\to\infty} x_n = x_0 + \sum_{k=1}^{\infty} y_k = x_0 - \sum_{k=1}^{\infty} \frac{(-1)^k}{k!} y_1 = x_0 - \left(e^{-1} - 1\right) y_1 = e^{-1} x_0 + \left(1 - e^{-1}\right) x_1 .$$

This will be the sought limit.

7b80.



Suppose the first person is in the point with x_1 coordinate and the other - x_2 coordinate. In this case the point (x_1, x_2) is positioned in the square with the side a . Problem conditions will be satisfied if the coordinates are determined by inequalities:

$$0 < x_1 < a - b,\ b + x_1 < x_2 < a .$$

In the graphic that area is shaded. Therefore the sought probability is determined by this formula:

$$P = 2\frac{0.5(a-b)^2}{a^2} = \left(1 - \frac{b}{a}\right)^2$$

(2 multiplier is necessary because two people can be in the x_k point with equal probability). The general case may be solved similarly using density of uniform distribution.

7b81.

On line C the stuck-at-1 fault (C/1) is redundant since the output in the circuit below and in the circuit with the corresponding fault implements the same logical function f=a+!b where !b is the negation of variable b and the following identity is true: a&b + (!b) = a + b.

7b82.

No it is impossible.

7b83.

{⇳ (w0, r0, w1, r1)}:

7b84.

⇳ (w0), ⇳ (r0), ⇳ (w1), ⇳(r1):

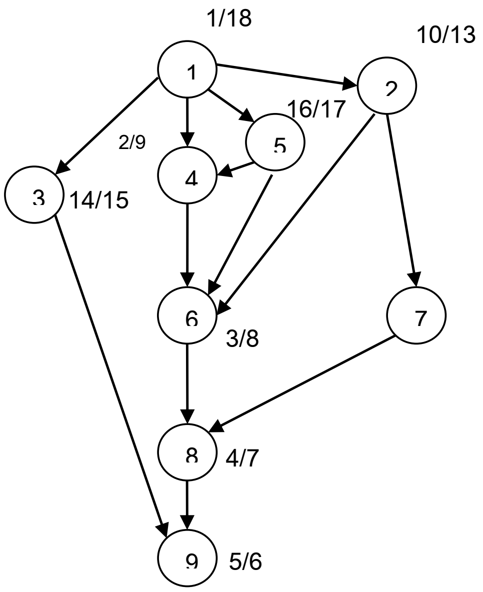
7b85.

Using sets' logic addition, multiplication and negation laws, the following results will be obtained:

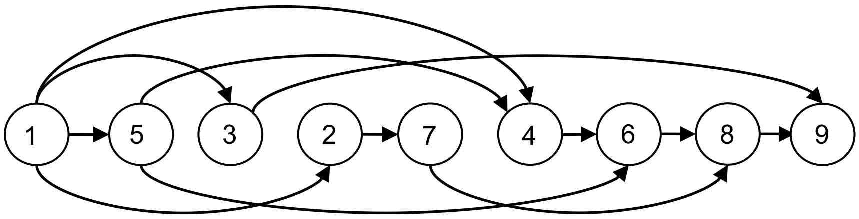
1) F{1, 2}= A·B
2)F{1, 4}=B·C
3) F{1, 2, 4}=A·B+B·C
4) F{4, 7}= $\bar{A}$·C
5) F{1, 2, 4, 7}=A·B+B·C+$\bar{A}$·C
6) F{1, 2, 3, 4, 5, 7}=A+A·B+B·C+ $\bar{A}$·C

7b86.

1. Implementing searching by depth, the start and end of vertices' development will be obtained, as shown in the figure.



2. Sorting the vertices from left to right is done based on time reduction of completing their developments.

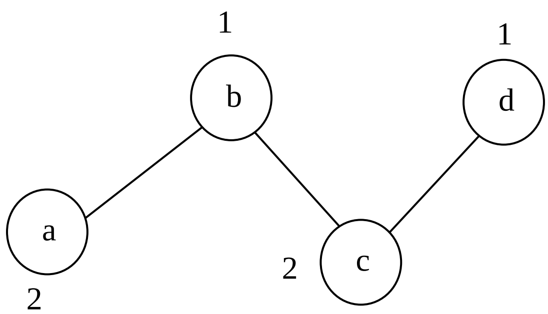


7b87.

Calculate the vertex coordinates of rectangles, including nets:
a(x)min=1 ; a(y)min=4 ;
a(x)max=7 ; a(y)max=6 ;
b(x)min=4 ; b(y)min=3 ;
b(x)max=11; b(y)max =5 ;
c(x)min=9 ; c(y)min=1 ;
c(x)max=21 ; c(y)max=4 ;
d(x)min=16 ; d(y)min=3 ;
d(x)max=19 ; d(y)max=6:

2. Define overlapping of rectangles, including nets. For overlapping of rectangles to occur, it is necessary that the vertex coordinates of rectangles overlap one another, both my x and y coordinates. For example, the x (1-7) and y (4-6) coordinates of rectangle, corresponding to the net, cover corresponding coordinates of b - (4-11) and (3-5), therefore they overlap. And for example, there is overlap between a and c only by y coordinate, therefore they don't overlap.

3. Defining overlaps, present among all nets, construct the graph of overlappings and heuristically define its chromatic number, as depicted in the figure:



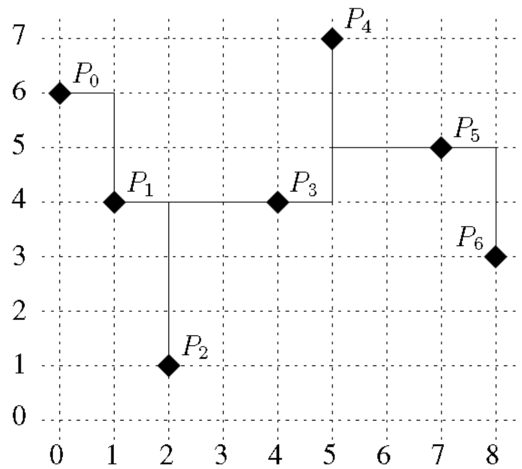
Answer: The upper limit of the number of minimum layers, necessary for implementation of interconnects will be 2.

7b88.

For example, 1. N=1, Answer 1: N=3, Answer 3.

```
#include <iostream>

long long int fib(unsigned n)
{
	long long int f[] = {0, 1};
	for(unsigned i = 2; i <= n; ++i) {
		f[1&i] = f[0] + f[1];
	}
	return f[1&n];
}
int main()
{
	unsigned N;
	std::cin >> N;
	if(0 == N) {
		std::cout << 0;
	} else {
		std::cout << fib(N+1);
	}
	std::cout << " different paths" << std::endl;
	return 0;
}
```

7b89.



14 length units

7b90.

Step i	1	2	3	4
Edge e	(a,c)	(a,b)	(d,e)	(c,e)
Weight d	10	12	19	22

8. OBJECT-ORIENTED PROGRAMMING

1. Test questions

8a1.	B	8a58.	C	8a115.	D
8a2.	B	8a59.	E	8a116.	C
8a3.	E	8a60.	A	8a117.	D
8a4.	D	8a61.	D	8a118.	E
8a5.	B	8a62.	A	8a119.	C
8a6.	C	8a63.	A	8a120.	C
8a7.	A	8a64	B	8a121.	C
8a8.	B	8a65.	A	8a122.	B
8a9.	C	8a66.	E	8a123.	B
8a10.	D	8a67	A	8a124.	A
8a11.	B	8a68	B	8a125.	D
8a12.	D	8a69	D	8a126.	B
8a13.	C	8a70	C	8a127.	C
8a14.	A	8a71	B		
8a15.	A	8a72	A		
8a16.	C	8a73	B		
8a17.	E	8a74	B		
8a18.	E	8a75.	A		
8a19.	C	8a76.	D		
8a20.	A	8a77.	E		
8a21.	D	8a78.	E		
8a22.	B	8a79.	B		
8a23.	E	8a80.	D		
8a24.	E	8a81.	E		
8a25.	C	8a82.	A		
8a26.	D	8a83.	C		
8a27.	C	8a84.	D		
8a28.	C	8a85.	C		
8a29.	E	8a86.	D		
8a30.	B	8a87.	C		
8a31.	E	8a88.	A		
8a32.	D	8a89.	D		
8a33.	B	8a90.	B		
8a34.	A	8a91.	A		
8a35.	B	8a92.	B		
8a36.	A	8a93.	A		
8a37.	B	8a94.	C		
8a38.	A	8a95.	A		
8a39.	B	8a96.	B		
8a40.	E	8a97.	A		
8a41.	E	8a98.	C		
8a42.	C	8a99.	A		
8a43.	B	8a100.	C		
8a44.	D	8a101.	B		
8a45.	D	8a102.	A		
8a46.	D	8a103.	C		
8a47.	C	8a104.	C		
8a48.	E	8a105.	A		
8a49.	D	8a106.	A		
8a50.	B	8a107.	B		
8a51.	D	8a108.	C		
8a52.	C	8a109.	B		
8a53.	D	8a110.	A		
8a54.	D	8a111.	C		
8a55.	B	8a112.	C		
8a56.	A	8a113.	B		
8a57.	C	8a114.	B		

b) Problems

8b1.

The length of the greatest common subsequence can be computed using the following program:

```
#include <stdio.h>
#define N 1000
#define max(a,b) ((a>b) ? a : b)
int L[N][N];
int main(){
    char a[N];
    char b[N];
    int i, j, n, m;
    int yes = 0;
    scanf("%s", a);
    scanf("%s", b);
    n = strlen(a);
    m = strlen(b);
    for( j = 0; j < m ; j++ )    {
       if( b[j] == a[0] ) yes = 1;
       L[0][j] = yes;
    }
    yes = 0;
    for(i = 0; i < n; i++)    {
       if( a[i] == b[0] ) yes = 1;
       L[i][0] = yes;
    }
    for(i = 1; i < n; i++)    {
       for(j = 1; j < m ; j++)       {
          if( a[i] == b[j] )
             L[i][j] = L[i-1][j-1] + 1;
          else
             L[i][j] = max( L[i-1][j], L[i][j-1] );
       }
    }
    printf( "%d\n",  L[n-1][m-1] );
    return 0;
}
```

8b2.

AM(10,10)= 7368

8b3.

Sum of digits =150

Q=3.752002426043100302699428993946639820.

8b4.

```
Subs(n,k):=
  If (n==k) then Ss={{1,2,3,...,n}};
                    goto END;
              else A={1,...,k}
  end;
  Ss={};
  p=k;
  label P
  Ss=Ss⊕A;
  If (A(k)==n) then p=p-1
                 else p=k
  end;
  If (p>=1) then i=k+1;
                 label Q;
                 i-i-1;
                 If(i>=p) then A(i)=A(p)+i-p+1;
                                  goto Q
                            else goto P;
                 end;
  end;
label END;
Rerurn(Ss)
```

8b5.
Use Induction. The loop invariant is the following: $x_j y_j^{z_j} = y_0^{z_0}$

8b6.
Use Induction.

8b7.
Use Induction.

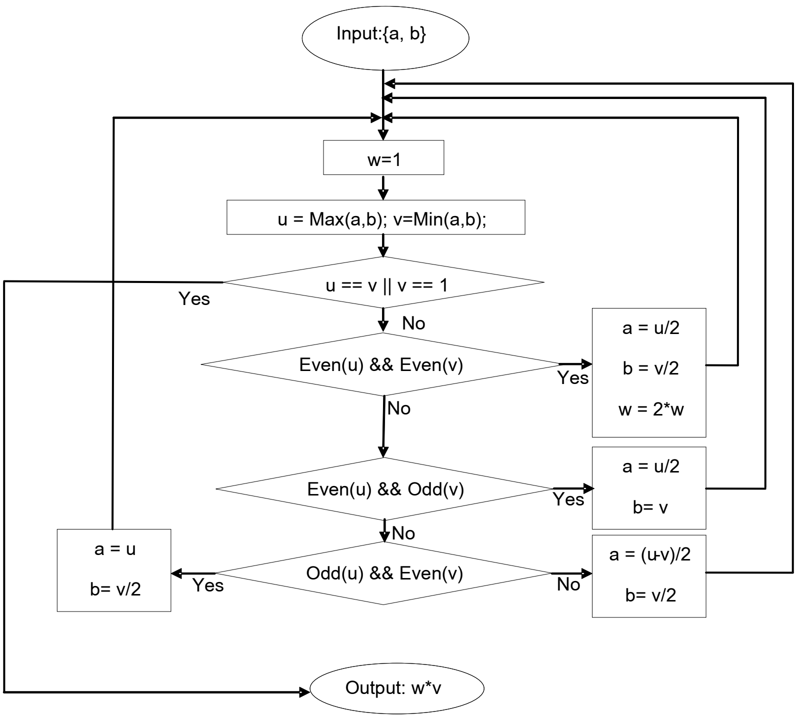
8b8.
```
#include <iostream>
using namespace std;
int main(){
	int n;
	cin >> n;
	cout << n - (n/2 + n/3 + n/5 - n/6 - n/15 - n/10 + n/30) << endl;
	return 0;
}
```
8b9.
```
#include <iostream>
#include <fstream>
#include <cmath>
#include <algorithm>
#include <set>
#include <queue>
#include <stack>
#include <iomanip>

using namespace std;

struct matric {
	int a[2][2];
};

matric a1;

matric mul(matric a,matric b) {
	int i,j,k;
	matric h;
	for (i=0;i<2;i++)
		for (j=0;j<2;j++)
			h.a[i][j]=0;
	for (i=0;i<2;i++)
		for (j=0;j<2;j++)
			for (k=0;k<2;k++)
			{
				h.a[i][j]= ((__int64)h.a[i][j] + (__int64)a.a[i][k]*b.a[k][j])
% 1000007;
				h.a[i][j]%=1000007;
			}
	return h;
}
matric stepen(matric a,int n) {
	if (n==1)
		return a;
	matric h=stepen(a,n/2);
	h=mul(h,h);
	if (n&1)
		h=mul(h,a1);
	return h;
}
int main() {
	int n;
	cin >> n;
	a1.a[0][0]=1;a1.a[0][1]=1;
	a1.a[1][0]=1;a1.a[1][1]=0;
	matric h1 = stepen(a1,n);
	cout << h1.a[0][0] << endl;
	return 0;
}
```

8b10.

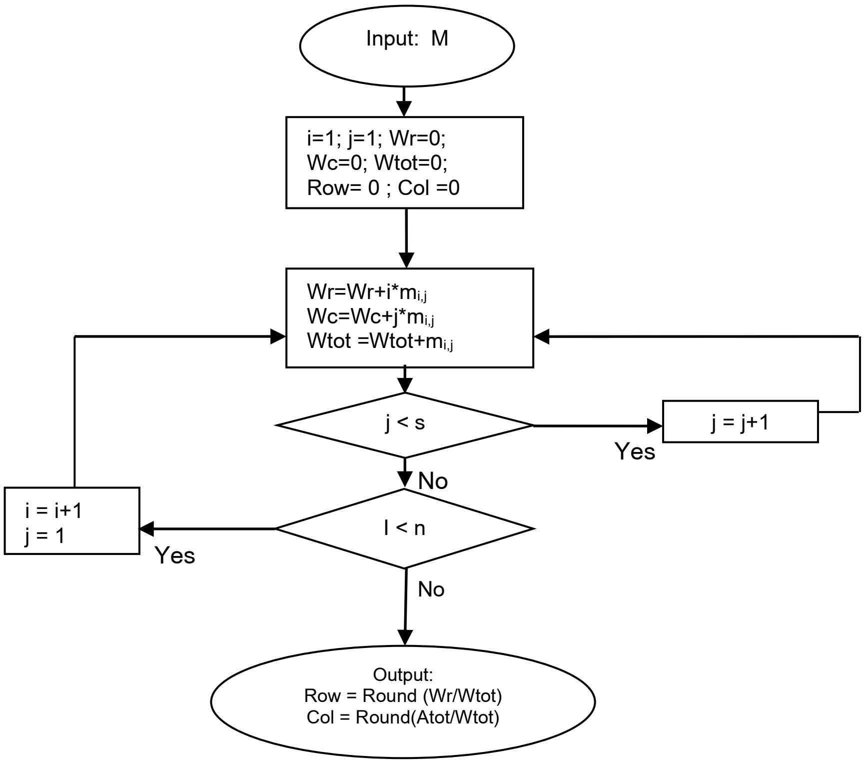
```
#include <iostream>
#include <fstream>

using namespace std;

ifstream in("15.in");
ofstream out("15.out");
int number,arr[5000],ans[5000];
int i,j,max;
int main()
{
	in >> number;
	for (i=0;i<number;i++)
		in >> arr[i];
	for (i=0;i<number;i++)
	{
		max=0;
		for (j=0;j<i;j++)
			if (arr[j]<arr[i] && max<ans[j])
				max=ans[j];
		ans[i]=max+1;
	}
	max=0;
	for (i=0;i<number;i++)
		if (ans[i]>max)
			max=ans[i];
	out << max << endl;
	return 0;
}
```

8b11.

Assume that detection Odd/Even as well as division of even integers by 2 are operations that are to be made with the last position of binary representations and hence do not use the deletion in common sense.

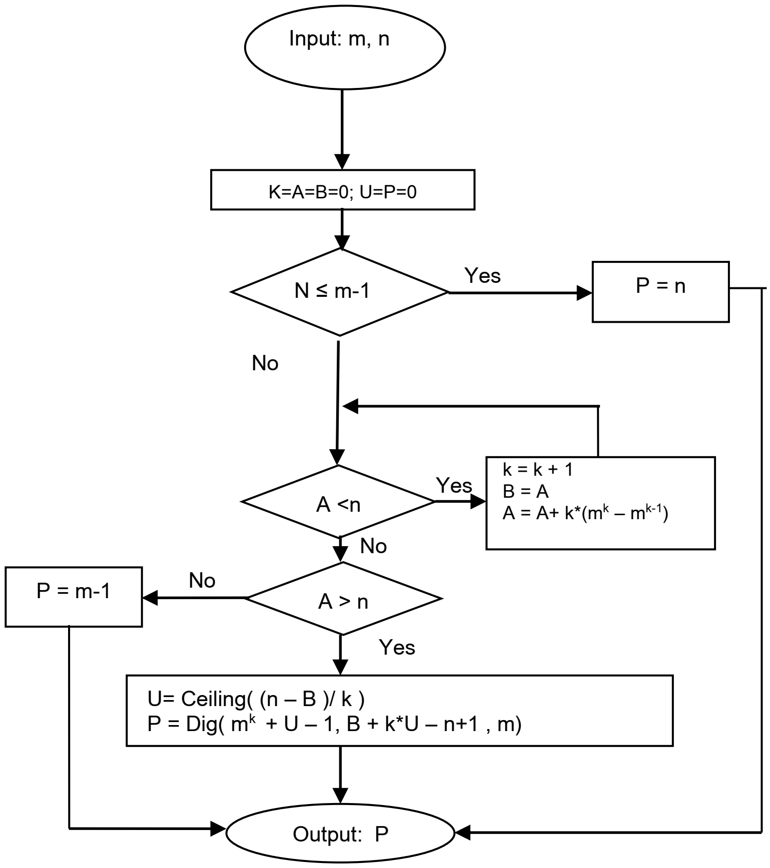


8b12.
A.

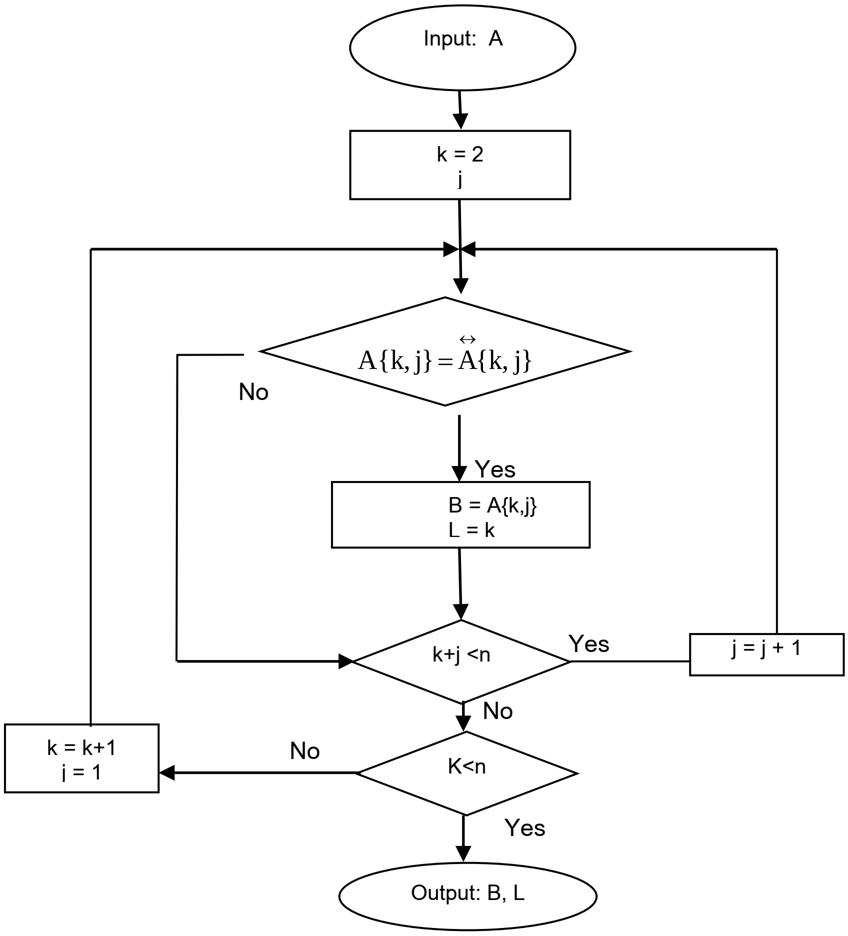


B. O(n*s).

8b13.
Dig(x,y,z) = Mod(Floor(x/z^{y-1}), z), i.e Dig(x,y,z) is equal to y-th digit (from the right side) in z-ary representation of the number x.



8b14.



Here $A\{k, j\}$ denotes a fragment of A having length k and startpoint j, and $\overset{\leftrightarrow}{A}\{k, j\}$ denotes the reflection (in miror) of $A\{k, j\}$.

8b15.

```
#include <iostream>
#include <cmath>

int main()
{
    const int n = 1000;
    const int size = 200;
    int prime_numbers[size] = {0};
    int index = 0;

    for (int i = 2; i <= n; ++i) {
        int limit = (int)sqrt(i);
        int j = 2;
        for (; j <= limit; ++j) {
            if (0 == i % j) {
                break;
            }
        }
        if (j > limit) {
            prime_numbers[index] = i;
            ++index;
        }
    }

    for (int k = 0; k < index; ++k) {
        std::cout << prime_numbers[k] << " ";
    }
    std::cout << std::endl;
    return 0;
}
```

8b16.

```
#include <iostream>

int main(){
    const int n = 1000;
    const int size = 20;
    int perfect_numbers[size];
    int index = 0;

    for (int i = 2; i <= n; ++i) {
        int sum = 0;
        int limit = i/2;
        for (int j = 1; j <= limit; ++j) {
            if (0 == i % j) {
                sum += j;
            }
        }
        if (i == sum) {
            perfect_numbers[index] = i;
            ++index;
        }
    }

    for (int k = 0; k < index; ++k) {
        std::cout << perfect_numbers[k] << " ";
    }
    std::cout << std::endl;

    return 0;
}
```

8b17.

```
#include <iostream>

long reverse_number(long n);

int main(){
    std::cout << "Please enter the number: ";
    long n;
    std::cin >> n;
    long reverse_n = reverse_number(n);
    if (n == reverse_n) {
        std::cout << "Yes"  << std::endl;
    } else {
        std::cout << "No" << std::endl;
    }

    return 0;
}
long reverse_number(long n){
    long reverse = 0;
    do  {
        reverse = reverse * 10 + n % 10;
        n /= 10;
    } while (n != 0);

    return reverse;
}
```

8b18.

```
#include <iostream>

// Output a partition:
void output_partition(const int n, const int *x, const int how_many_partitions){
       std::cout << "Partition(" << how_many_partitions << ")" << " = ";
       for (int i = 1; i <= n; i++)    {
              // Can't show negative numbers:
              if (x[i] > 0)             {
                     if (i == n)
                            std::cout << x[i];
                     else
```

```
                        std::cout << x[i] << " + ";
                }
        }
        std::cout << std::endl;
}

// This is the function which generates the partitions of a given number "n".
void generate_partitions(int *x, const int n){
        int k, s = 0;
        int how_many_partitions = 0;
        for (k = 1; k < n; k++)
                x[k] = -1;
        k = 1;
        while (k > 0)       {
                // Generated a solution, let's output it then:
                if (k == n)        {
                        how_many_partitions++; // Increase the number of generated
partitions
                        x[n] = n - s;
                        output_partition(n, x, how_many_partitions);
                        k--;
                        s = s - x[k];
                }
                else        {
                        // Check for another solution:
                        if (((n - k + 1) * (x[k] + 1)) <= n - s)     {
                                x[k]++;
                                if (x[k] >= x[k - 1])
                                {
                                        s = s + x[k];
                                        k++;
                                }
                        }
                        else    {

                                x[k] = -1;
                                k--;
                                s = s - x[k];
                        }
                }
        }
}

int main() {

        char str[100];
        int number;
        std::cout << "n= " ;
        while(true)  {
                std::cin >> str;
                if (sscanf(str, "%d", &number) != 1 || number<2){
                        std::cout << "Please enter number >= 2!" <<std::endl;
                        std::cout << "n = ";
                }
                else{
                        break;
                }
        };

        int *x = new int[number + 1];
        if (x == NULL)
                throw std::bad_alloc("");
        x[0] = 0;
        std::cout << "Partitions of " << number << ":\n\n";
        generate_partitions(x, number);

        delete [] x;
```

```
	std::cin.ignore();
	std::cin.get();
	return 0;
}
```

8b19.

a.

```
pick n,m;
n_factorial = 1;
m_factorial = 1;
n_m_factorial = 1;
for (count1= 2, n)
	n_factorial = n_factorial *count1;
end for
for (count2 = 2, m)
	m_factorial = m_factorial *count2;
end for
for (count2 = 2, n-m)
	m_n_factorial = m_n_factorial *count2;
end for
return (m_factorial *  n_factorial / m_n_factorial);
```

b.

```
pick n,m;

m_factorial = 1;
n_m_factorial = 1;
temp = 2;
for (count1 = 2, m)
	m_factorial = m_factorial *count1;
end for
n_factorial = m_factorial
for (count2 = m, n)
	m_n_factorial = m_n_factorial * temp;
	temp++;
	n_factorial = n_factorial *count2;
end for
return (m_factorial *  n_factorial / m_n_factorial);
```

c.

$C_1(n,m) = n*m(n-m)$

$C_2(n,m) = m(n-m)$

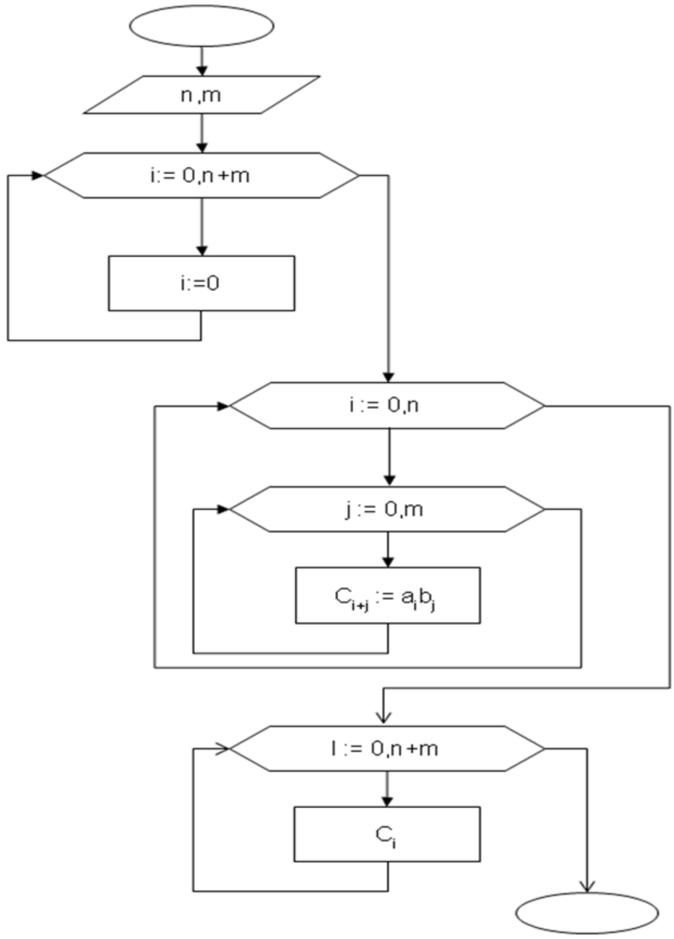
d.

For the simplest algorithm (n=100, m=90), 202 multiplication and division actions will be required. For the given algorithm, 112 multiplication and division actions will be required.

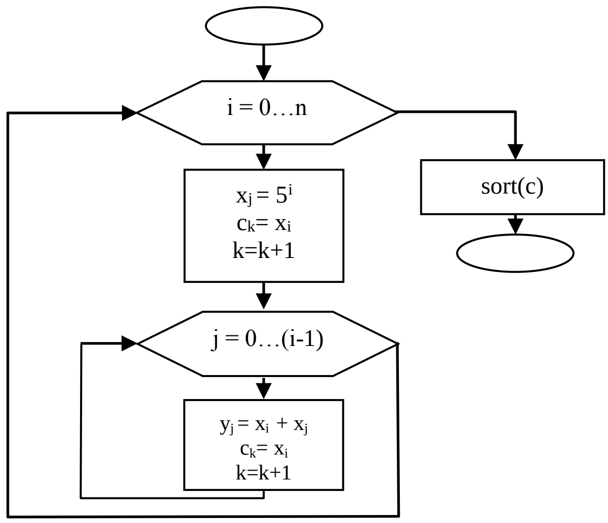
8b20.

$$a_i, i=\overline{0,n} \quad b_j, j=\overline{0,m}$$

$$C_k = \sum_{\substack{i+j=k \\ 0\le i\le n \\ 0\le j\le m}} \prod a_i b_j, k=\overline{0,n+m}$$



8b21.



8b22.

```
#include <iostream>
struct rect{
       rect()
              : left(), bottom(), right(), top()
       {}
        double left;
        double bottom;
        double right;
        double top;
};
std::ostream& operator <<(std::ostream& out, const rect& r){
         out << "(" << r.left << ", " << r.top << ") ("
                     << r.right << ", " << r.bottom << ")";
         return out;
```

```
}

std::istream& operator >>(std::istream& in, rect& r){
        in >> r.left >> r.top >> r.right >> r.bottom;
         return in;
}

void intersection(const rect& a, const rect& b, rect& r){
        r.left = std::max(a.left, b.left);
        r.bottom = std::max(a.bottom, b.bottom);
        r.right = std::min(a.right, b.right);
        r.top = std::min(a.top, b.top);
}

bool is_valid(const rect& r){
        return (r.left <= r.right) && (r.bottom <= r.top);
}

int main(){
        rect a, b;
        std::cin >> a >> b;
        rect r;
        intersection(a, b, r);
        if ( is_valid(r) ) {
                std::cout << r << std::endl;
        } else {
                std::cout << "Has no intersection!" << std::endl;
        }
         return 0;
}
```

8b23.

```
#include <iostream>
int main() {
        unsigned long long n;
        std::cin >> n;
        // The number of intersection of diagonals when no 3 intersect in one
        // point is equal to 4-combinations of a n, as every 4 point introduce
        // a new intersection point.
        unsigned long long s = n;
        s = s * (n - 1) / 2;
        s = s * (n - 2) / 3;
        s = s * (n - 3) / 4;
        std::cout << s << std::endl;
        return 0;
}
```

8b24.

```
#include <iostream>
#include <vector>

struct point{
       point(const double& a, const double& b)
              : x(a), y(b)
       {}
       point()
              : x(0), y(0)
       {}

       double x;
       double y;
};

typedef std::vector<point> polygon;

int sign(const double& x){
        return x == 0 ? 0 : (x > 0 ? 1 : -1);
}

double cross_product(const point& a, const point& b, const point& c){
        return (b.x - a.x) * (c.y - b.y) - (c.x - b.x) * (b.y - a.y);
}

bool is_convex(const polygon& p){
```

```
        if (p.size() < 3) {
                return false;
        }
        const size_t n = p.size();
        int s = sign(cross_product(p[n - 1], p[0], p[1]));
        if ( s == 0 ) {
                return false;
        }
        for (size_t i = 0; i < n - 2; ++i) {
                if ( s * cross_product(p[i], p[i + 1], p[i + 2]) <= 0 ) {
                        return false;
                }
        }
        return s * cross_product(p[n - 2], p[n - 1], p[0]) > 0;
}

int main(){
        size_t n;
        std::cin >> n;
         polygon p(n);
        for ( size_t i = 0 ; i < n ; ++i ) {
                std::cin >> p[i].x >> p[i].y;
        }
         if ( is_convex(p) ) {
             std::cout << "Yes" << std::endl;
         } else {
             std::cout << "No" << std::endl;
         }
         return 0;
}
```

8b25.

```
#include <iostream>
int main()
{
        unsigned long long m, n;
        std::cin >> m >> n;
        // The number of rectangles is equal to 2-combinations of a (m + 1)
        // multiplied with 2-combinations of a (n + 1).
        unsigned long long s = m + 1;
        s = s * m / 2;
        s = s * (n + 1) * n / 2;
        std::cout << s << std::endl;
        return 0;
}
```

8b26.

```
#include <iostream>
int main()
{
        unsigned int n;
        std::cin >> n;
        if ( --n == 0 ) {
                std::cout << 2;
        } else {
                unsigned long long s = 3;
                while ( --n ) {
                        s *= 10;
                }
                std::cout << 8 * s;
        }
        return 0;
}
```

8b27.

```
#include <iostream>
int main()
{
        unsigned long long n;
        std::cin >> n;
        unsigned long long s = 0;
        while ( (n /= 5) != 0 ) {
                s += n;
```

```
        }
        std::cout << s;
        return 0;
}
```

8b28.

```
#include <iostream>
int main()
{
        unsigned int n;
        std::cin >> n;
        unsigned long long s = 1;
        unsigned long long c = 1;
        while ( --n ) {
                s = s* 10 + 1;
                c *= 5;
        }
        std::cout << s * c * 15;
        return 0;
}
```

8b29.

```
#include <iostream>
int main()
{
        unsigned int n;
        std::cin >> n;
        unsigned long long d = 1;
        unsigned long long o = 1;
        while ( --n ) {
                d *= 10;
                o *= 8;
        }
        std::cout << 9 * d - 7 * o;
        return 0;
}
```

8b30.

Schedule: $t_{v1}=1$, $t_{v2}=1$, $t_{v3}=1$, $t_{v4}=3$, $t_{v5}=3$, $t_{v6}=5$
Latency=5
3 Multipliers and 1 Adder

8b31.

```
#include <iostream>
bool is_in_matrix(int** a, int n, int m, int h)
{
      int i = 0;
      int j = m - 1;
      while (i < n && j >= 0) {
            if (h == a[i][j]) {
                  return true;
            }
            if (h < a[i][j]) {
                  --j;
            } else {
                  ++i;
            }
      }
      return false;
}

int main()
{
      int n, m;
      std::cin >> n >> m;
      int** a = new int*[n];
      for (int i = 0; i < n; ++i) {
            a[i] = new int[m];
      }
      for (int i = 0; i < n; ++i) {
            for(int j = 0; j < m; ++j) {
```

```
                        std::cin >> a[i][j];
                }
        }
        int k;
        std::cin >> k;
        for(int i = 0; i < k; ++i) {
                int h;
                std::cin >> h;
                std::cout << is_in_matrix(a, n, m, h) << std::endl;
        }
        return 0;
}
```

8b32.

```
#include <iostream>
#include <cstring>
void reverse(char* s)
{
        size_t l = std::strlen(s) - 1;
        for (int i = 0; i <= l / 2; ++i)
        {
                std::swap(s[i], s[l - i]);
        }
}
void rotate(char* s, size_t n)
{
          size_t l = std::strlen(s);
          n %= l;
          if ( n == 0 ) {
                  return;
          }
        reverse(s);
        reverse(s + l - n);
        char t = s[l - n];
        s[l - n] = '\0';
        reverse(s);
        s[l - n] = t;
}
int main()
{
          size_t l;
          size_t c;
          std::cin >> l;
          char* s = new char[l];
          std::cin >> s;
          std::cin >> c;
          rotate(s, c);
          std::cout << s << std::endl;
          return 0;
}
```

8b33.

```
#include <iostream>
#include <queue>
int main()
{
        size_t N;
             size_t M;
        std::cin >> M;
        std::cin >> N;
        int n;
        std::priority_queue<int> p;
        for (size_t i = 0; i < M; ++i) {
                        std::cin >> n;
                p.push(n);
                if (p.size() > N) {
```

```
                p.pop();
            }
        }
        while (!p.empty()) {
            std::cout << p.top() << " ";
            p.pop();
        }
        return 0;
    }
```

8b34.

```
#include <iostream>
#include <cmath>
bool is_square(size_t k)
{
        size_t p = std::sqrt(k);
        return p * p == k;
}
int main()
{
        size_t N, k;
        std::cin >> N;
        std::cin >> k;
        std::cout << (is_square(k) ? "Open" : "Close") << std::endl;
        return 0;
}
```

8b35.

For example, 1. N=1, Answer 1: N=3, Answer 3.

```
#include <iostream>

long long int fib(unsigned n)
{
        long long int f[] = {0, 1};
        for(unsigned i = 2; i <= n; ++i) {
                f[1&i] = f[0] + f[1];
        }
        return f[1&n];
}

int main()
{
        unsigned N;
        std::cin >> N;
        if(0 == N) {
                std::cout << 0;
        } else {
                std::cout << fib(N+1);
        }
        std::cout << " different paths" << std::endl;
        return 0;
}
```

8b36.

For example, 5, (1, 0), (0, 1), (-1, 0), (0, -1), (0, 0); Answer 5,7.

8b37.

```
#include <iostream>

void swap(double& a, double& b)
{
        double t(a);
        a = b;
        b = t;
}

void find_min_max(double p[], int N, double& min, double& max)
```

```
{
        int i, j;
        for(i = 0, j = N-1; j - i > 1; ++i, --j) {
                if(p[j] < p[i]) {  //  N/2 compare
                        swap(p[j], p[i]);
                }
        }
        min = p[0];
        for(int k = 1; k <= i; ++k) {
                if(p[k] < min) { // N/2-1 compare
                        min = p[k];
                }
        }
        max = p[j];
        for(int k = j+1; k <= N-1; ++k) {
                if(p[k] > max) { //N/2-1 compare
                        max = p[k];
                }
        }
}

int main()
{
        int N;
        std::cin >> N;
        double p[N];
        for(int i = 0; i < N; ++i) {
                std::cin >> p[i];
        }
        double min, max;
        find_min_max(p, N, min, max);
        std::cout << "min == " << min << " max == " << max << std::endl;
}
```

8b38.

8b39.

8b36; 8b38; 8b39 are theoretical questions and don't require implementation with C++, as long C++ code is required to solve it.

8b40.

```
#include <bits/stdc++.h>
#define DB(a) cerr << __LINE__ << ": " << #a << " = " << (a) << endl;
using namespace std;

const int MAXN = 2005;
int n, x[MAXN], y[MAXN], a1[MAXN], a2[MAXN], m1, m2, t;

int match[MAXN], used[MAXN], n1 /*  n1 is the number of nodes in the left side
      */;
vector<int> g[MAXN];

bool find (int u)
{
      if (u == -1)
            return true;

      for (int i = 0; i < g[u].size(); ++i)
      {
            int v = g[u][i];

            if (!used[v])
            {
                  used[v] = true;

                  if (find(match[v]))
                  {
```

```
                        match[v] = u;
                        match[u] = v;
                        return true;
                  }
            }
      }
      return false;
}

int main ()
{
      ios_base::sync_with_stdio(0);
      cin.tie(0);

      m1 = m2 = 0;
      for (int i = 0; i < MAXN; ++i)
            g[i].clear();
      cin >> n;
      for (int i = 0; i < n; ++i)
      {
            cin >> x[i] >> y[i];
            a1[m1++] = x[i];
            a2[m2++] = y[i];
      }
      sort(a1, a1 + m1);
      sort(a2, a2 + m2);
      m1 = unique(a1, a1 + m1) - a1;
      m2 = unique(a2, a2 + m2) - a2;

      for (int i = 0; i < n; ++i)
      {
            x[i] = lower_bound(a1, a1 + m1, x[i]) - a1;
            y[i] = lower_bound(a2, a2 + m2, y[i]) - a2;
      }
      for (int i = 0; i < n; ++i)
            g[x[i]].push_back(y[i] + m1);

      int ans = 0;
      memset(match, -1, sizeof match);

      for (int i = 0; i < m1; ++i)
      {
            memset(used, 0, sizeof used);
            ans += find(i);
      }

      cout << ans << endl;
      return 0;
}
```

8b41.

```
#include <cstdio>
#include <algorithm>
using namespace std;
const int MAXN = 100005, MAXK = 2605, ITER = 25;
const int KAYAK = 20;
int N, K = 0, occur [101][101];
double speed;
pair <short, short> person [MAXN], uniq [MAXK];
inline bool comp (pair <short, short> a, pair <short, short> b)
{
return a.second - speed * a.first < b.second - speed * b.first;
}
inline bool works (double x)
```

```
{
speed = x;
sort (uniq, uniq + K, comp);
N = 0;
for (int i = 0; i < K; i++)
for (int j = 0; j < occur [uniq [i].first][uniq [i].second]; j++)
person [N++] = uniq [i];
for (int i = 0, j = N - 1; i < j; i++, j--)
if (person [i].second + person [j].second < speed * (person [i].first + person
[j].first + KAYAK))
return false;
return true;
}
int main ()
{
scanf ("%d", &N);
for (int i = 0; i < N; i++)
{
scanf ("%hd %hd", &person [i].first, &person [i].second);
occur [person [i].first][person [i].second]++;
}
for (int a = 50; a <= 100; a++)
for (int b = 50; b <= 100; b++)
if (occur [a][b] > 0)
uniq [K++] = make_pair (a, b);
double lo = 0, hi = 5.0 / 3.0;
for (int it = 0; it < ITER; it++)
{
double mid = (lo + hi) / 2;
if (works (mid))
lo = mid;
else
hi = mid;
}
printf ("%lf\n", lo);
return 0;
}
```

8b42.

```
#include <stdio.h>
#define BOUGHT 1
#define NOTBOUGHT 0
#define CREDITMAX 1002

int main(void){
int i,j,k;
int credit,iTemp;
int Type[102] = {5,2,6,1,4,3,3,1,1};
int Price[102] = {8,4,8,13,5,2,13,1,1};
int Quality[102] = {7,8,13,12,5,7,5,1};
int Money = 53, iInput = 7;
int FlagWeapons[7];
int Wallet,MaxQuality;
scanf("%d %d",&iInput,&Money);
for(i= 0; i < iInput;i++){
scanf("%d %d %d",&Type[i],&Price[i],&Quality[i]);
}
//Find the maximum quality
MaxQuality = 0;
for(i= 0; i < iInput;i++){
if(Quality[i]>MaxQuality) MaxQuality = Quality[i];
}
//Buy and test.
for(j = MaxQuality; j>0; j--){
```

```
Wallet = Money; //refill Wallet with money ;P
for(i= 1; i <= 6; i++) FlagWeapons[i] = NOTBOUGHT; //reset the cart

for(k=1;k<=6;k++){
credit = CREDITMAX;
for(i= 0; i < iInput;i++){
if(Type[i] != k ) continue; //check for current weapon only.
if(Quality[i]>= j ){
if(Wallet >= Price[i]){ //check if there is money in the wallet.
if (Price[i] < credit) credit = Price[i]; //try to buy the cheapest one just
above the quality.
}
}
}//for(i= 0; i < iInput;i++)
if(credit < CREDITMAX){
if(Wallet < credit){
// printf("Cant afford Loser");
break; //
}
Wallet -= credit; //Now buy the weapon.
FlagWeapons[k] = BOUGHT; //set the bought flag for that weapon.
}//if(credit < CREDITMAX)
}//for(k=1;k<=6;k++)
//check if all weapons have been bought
iTemp = 0;
for(i= 1; i <= 6; i++){
if(FlagWeapons[i] == NOTBOUGHT) break;
iTemp++;
}
/*--------->>>>>>Output data <<<<<<------------*/
if(iTemp == 6){
printf("\n%d",j);
return(0);
}
/*--------->>>>>>Output data <<<<<<------------*/
}//for(j = MaxQuality; j>0; j--)
/*--------->>>>>>Output data <<<<<<------------*/
printf("\n0");
/*--------->>>>>>Output data <<<<<<------------*/
return(0);
}
```

8b43.

```
#include <algorithm>
#include <cstdio>

using namespace std;

const int MAXN = 500;

int K, N;
int A[MAXN], res[MAXN+1][MAXN+1];

void solve()
{
sort(&A[0], &A[N]);

for (int j = 1; j <= N; ++j) res[1][j] = A[j-1];
for (int i = 2; i <= K; ++i)
{
for (int j = i; j <= N; ++j)
{
res[i][j] = res[i-1][j-1];
```

```
// actually, there's an O(n^2) solution
for (int k = i-1; k < j-1; ++k)
res[i][j] = min(res[i][j], res[i-1][k] + A[k-1] * (j-k-1));

res[i][j] += A[j-1];
}
}

int answer = 1000000000;

for (int j = K; j <= N; ++j)
if (answer > res[K][j] + (N-j) * A[j-1]) answer = res[K][j] + (N-j) * A[j-1];

printf("%d\n", answer);
}

int main()
{
int T; scanf("%d", &T);
for (int t = 0; t < T; ++t)
{
scanf("%d%d", &N, &K);

for (int i = 0; i < N; ++i) scanf("%d", &A[i]);
solve();
}

return 0;
}
```

8b44.

In any i-th step, the applicant pretender function of j-th element is calculated as follows:
$f_{ij}=f(i-1)_j-2r_{jk}$, where r_{jk} is the number of connections of j-th element in (i-1) step together with partitioned elements.

The adjacency matrix and calculation process is set out below:

	e1	e2	e3	e4	e5	e6	f0	f1	f2	f3
e1	0	1	0	0	0	0	<u>1</u>	X	X	X
e2	1	0	1	1	0	0	3	<u>1</u>	X	X
e3	0	1	0	1	1	1	4	4	2	
e4	0	1	1	0	1	0	3	3	<u>1</u>	X
e5	0	0	1	1	0	1	3	3	3	
e6	0	0	1	0	1	0	2	2	2	

As the first partitioning element, e1 element with the minimum connections is selected. After that, in every step, the recurrent partitioning element is selected on the condition of minimum of applicant function f pretender.

Answer:

1st part-e1, e2, e4;

2nd part-e3, e5, e6.

8b45.

Moving some i-th vertex from part A to part B, reduction of the number of connections between parts will be defined as follows:

$$F_i(A>B)= F_i(B)- F_i(A),$$

where $F_i(B)$ and $F_i(A)$ – the number of connections of i-th vertex with the vertices of B and A parts respectively.

Moving some j-th vertex from part B to part A, reduction of the number of connections between parts will be defined in analog form:

$$F_j(B>A)= F_j(A)- F_j(B):$$

Therefore in the result of transpositioning of i and j vertices, reduction of the number of connections between parts A and B will be defined as follows:

$$F_{ij}=F_i(A>B) + F_j(B>A)-2r_{ij},$$

where r_{ij} i and j – the number of connections between vertices.
Solution of the problem leads to defining the i, j pair of vertices which will lead to the maximum of F_{ij}.
For the illustrated example, the calculation is as follows:

$$F_{14}=F_1(A>B) + F_4(B>A)-2r_{14}=(2-0)+(1-0)-2*1=1;$$

With the same logic:

$$F_{15}=0 ; F_{16}=5; F_{24}=0; F_{25}=-1; F_{26}=0; F_{34}=2; F_{35}=1; F_{36}=-2:$$

The maximum value of F_{ij} was obtained for $F_{16}=5$. Therefore, in the result of transpositioning 1 and 5 vertices between A and B parts, the number of connections will be reduced by 5 and instead of the previous 6, will make 1.

9. NANOELECTRONICS

a) Test questions

9a1.	E
9a2.	C
9a3.	E
9a4.	C
9a5.	E
9a6.	D
9a7.	B

b) Problems

9b1.

It is possible to charge nanoparticles 1) under light illumination with photon energy, sufficient for photoelectric effect, 2) in case of the exchange of charge with a solvent that is controlled, in particular, by acidity level of pH environment.

Minimum charge of nanoparticles is equal modulo charge of an electron, and the maximum actually is not limited, but in practice rarely exceeds 1-2 electron charge in an electrically neutral overall colloidal solution, as a result of dynamic equilibrium with the ions in solution. The collision of particles and, consequently, the formation of agglomerates is possible if the kinetic energy of their thermal motion exceeds the potential energy of the Coulomb repulsion. For spherical silicon nanocrystals, having density of-Si equal to ρ=2 g/cm^3, can compute mass $M = \frac{4}{3}\pi R^3 \rho$ and estimate the minimum speed V_0, at which collision is possible:

$$\frac{MV_0^2}{2} + \frac{MV_0^2}{2} = \frac{q^2}{4\pi\varepsilon_0 \varepsilon 2R},$$

where ε_0 – dielectric constant, ε – permittivity of environment.

Then for nanoparticle with R=1nm and charge q =2e (e=1.6*10^{-19} Kl) in benzol (ε=2.3) the following will be obtained $V_0 = \frac{q}{2\sqrt{2\pi\varepsilon_0 \varepsilon RM}} = \frac{q}{4\pi R^2 \sqrt{\frac{2}{3}\varepsilon_0 \varepsilon\rho}}$ ≈ 155 m/s.

Estimate the average thermal speed V_T from the following relation:

$$\frac{MV_T^2}{2} = \frac{3}{2}kT,$$

where k – Boltzmann constant, T – temperature in Kelvin degrees.

Then $V_T = \sqrt{\frac{3kT}{M}} = \frac{3}{R}\sqrt{\frac{kT}{4\pi R\rho}}$ ≈ 40 m/s for $T=30$ K, which is much smaller than the above calculated V_0, and it means a conflict of nanoparticles in benzene and their subsequent agglomeration is unlikely.

At the same time for the colloidal solution of similar nanocrystals in water (ε = 80), V_0 ≈ 26 м/с < V_T is obtained which means high probability of constants of nanoparticles and, consequently, their agglomeration.

The probability of agglomeration, obviously depends on the size of nanoparticles and increases with increasing R due to a stronger dependence on the parameter values V_0.

In very dilute colloidal solutions in the above 2 partial approximation, the possibility of contact of nanoparticles in a collision does not depend on the concentration of particles. However, with the growth of the latter, the probability of collisions is obviously increasing, and thus increases the probability of agglomeration. Moreover, given the dependence of the effective permittivity on the concentration of nanoparticles, with the increase of the latter the probability of collision of charged particles may change, increasing, in particular, for silicon nanocrystals (ε = 12) in benzene.

In accordance with the above analysis, the possibility of collision of nanoparticles, obviously, depends on temperature and increases with increasing T, due to increased V_T, which should lead to an increase in the probability of agglomeration. At the same time, in case of temperature increase the agglomerates can be destroyed by thermal motion of particles. All this leads to a nonmonotonic dependence of the probability of agglomeration of the temperature.

9b2.

1) Sectional area equals to πr^2. For nanoparticles of radius, this value is $3.14\times(50\times10^{-9}\ m)^2 = 7.85\times10^{-15}\ m^2$. Then, according to the written formula $v = (2\times0.72\times0.4\ H / (1170\ kg/m^3 \times 10^7 \times 7.85\times10^{-15}\ m^2))^{1/2}$ = 79.2 m/s

2) Nanocluster has ionic structure $[W_6I_8]^{4+}(I^-)_4$. Only outer-iodine can be precipitated by silver nitrate.

$[W_6I_8]I_4 + 4AgNO_3 = 4AgI\downarrow + [W_6I_8](NO_3)_4$

Cation is octahedron of atoms of tungsten, on each edge of which iodine atom is located.

3) Any reasonable means are accepted. In particular, consider the option of breaking a compact mercury into nanoparticles with large surface area and their subsequent dispersion in the molten sulfur (this will ensure a complete course of the reaction) to form insoluble in water and most acids, mercuric sulphide, which can be used as component paints.

4) The calculation as per the given formula gives $(E_g)^2 = 1.468\times10^{-37}\ J^2$, hence $E_g = 3.83\times10^{-19}$ J. This corresponds to the wavelength $\lambda = hc/E_g = 6.62\times10^{-34}\ J\times s \times 3 \times 10^8\ m/s / (3.83\times10^{-19}\ J) = 5.2\times10^{-7} m$ = 520 nm, which corresponds to the green color.

9b3.

1) m_1 – body mass of a truck (with or without cargo) is a constant component, and the wheels are composed of two parts: a cylindrical surface and hemispheres. The mass of the cylindrical part is directly proportional to the radius, and the mass of hemisphere - square of the radius. Since perimeter of the wheel, and subsequently the radius is proportional to the number N, the following is obtained:

m_2N – the mass of the cylindrical part of the wheels;

m_3N^2 – the mass of hemispheres;

2) In cross-section the wheel of nano-truck consists of a regular N-gon. The side of the N-gon is equal to the diameter of a circle inscribed in a hexagon with side a = 1.4 Å, or the larger side of an equilateral triangle with an angle 120^0:

$$b=\sqrt{a^2+a^2+2\cdot a\cdot a\cdot\cos120^0}=a\sqrt{3}$$

During the rotation of such wheel, the position of its center oscillates from a minimum height equal to the radius of the circle inscribed in the N-gon with side b, up to the maximum height equal to the radius of the circle:

$$h_{\min}=r=\frac{b}{2tg\left(\pi/N\right)}=\frac{a\sqrt{3}}{2tg\left(\pi/N\right)}$$

$$h_{\max}=R=\frac{b}{2\sin\left(\pi/N\right)}=\frac{a\sqrt{3}}{2\sin\left(\pi/N\right)}$$

Hence the height of the jump is:

$$h=h_{\max}-h_{\min}=\frac{a\sqrt{3}}{2}\left(\frac{1}{\sin\left(\pi/N\right)}-\frac{1}{tg\left(\pi/N\right)}\right)=\frac{a\sqrt{3}\left(1-\cos\left(\pi/N\right)\right)}{2\sin\left(\pi/N\right)}$$

$$E=mgh=\frac{\left(m_1+m_2N+m_3N^2\right)\left[1-\cos\left(\pi/N\right)\right]ga\sqrt{3}}{2\sin\left(\pi/N\right)}$$

3) To find the minimum solve the equation:

$$\frac{dE}{dN}=0$$

$$\frac{dE}{dN}=\left(\frac{\left(m_1+m_2N+m_3N^2\right)\left[1-\cos\left(\pi/N\right)\right]ga\sqrt{3}}{2\sin\left(\pi/N\right)}\right)'=$$

$$=\frac{\left(m_2+2m_3N\right)\left[1-\cos\left(\pi/N\right)\right]ga\sqrt{3}}{2\sin\left(\pi/N\right)}+$$

$$+\frac{\left(m_1+m_2N+m_3N^2\right)\left(\sin^2\left(\pi/N\right)-\cos\left(\pi/N\right)\left[1-\cos\left(\pi/N\right)\right]\right)ga\sqrt{3}}{2\sin^2\left(\pi/N\right)}\cdot\left(-\frac{\pi}{N^2}\right)=$$

$$=\frac{\left(m_2+2m_3N\right)\left[1-\cos\left(\pi/N\right)\right]ga\sqrt{3}}{2\sin\left(\pi/N\right)}-$$

$$-\frac{\pi\left(m_1+m_2N+m_3N^2\right)\left[1-\cos\left(\pi/N\right)\right]ga\sqrt{3}}{2N^2\sin^2\left(\pi/N\right)}=0$$

Next, use the asymptotic formulas for trigonometric functions:

$$\frac{\left(m_2+2m_3N\right)\frac{\pi^2}{2N^2}ga\sqrt{3}}{2\left(\pi/N\right)}-\frac{\pi\left(m_1+m_2N+m_3N^2\right)\frac{\pi^2}{2N^2}ga\sqrt{3}}{2N^2\left(\pi/N\right)^2}=0$$

$$\frac{\left(m_2+2m_3N\right)\frac{\pi^2}{2N^2}}{2\left(\pi/N\right)}-\frac{\pi\left(m_1+m_2N+m_3N^2\right)\frac{\pi^2}{2N^2}}{2N^2\left(\pi/N\right)^2}=0$$

$$\frac{\left(m_2+2m_3N\right)\pi}{4N}-\frac{\pi\left(m_1+m_2N+m_3N^2\right)}{4N^2}=0$$

$$\frac{m_2+2m_3N}{N}-\frac{m_1+m_2N+m_3N^2}{N^2}=0$$

$$\frac{-m_1+m_3N^2}{N^2}=0$$

Find N:

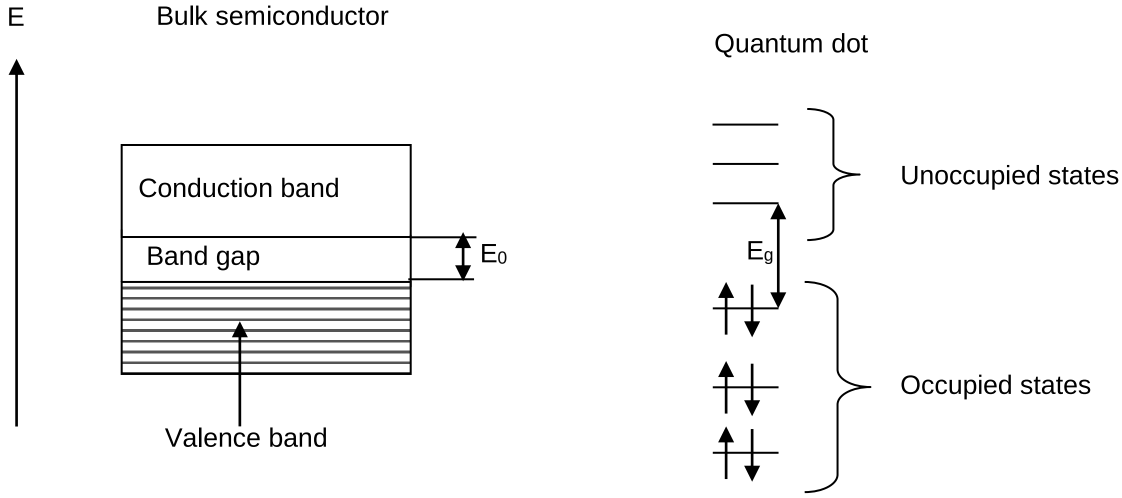
$$N=\sqrt{\frac{m_1}{m_3}}=\sqrt{\frac{10000}{25}}=20$$

Find the energy:

$$E=\frac{\left(\frac{10000+700\cdot 20+25\cdot 20^2}{6.02\cdot 10^{23}}\cdot 10^{-3}kg\right)\left[1-\cos(\pi/20)\right]\cdot 9.8\frac{H}{kg}\cdot 1.4\cdot 10^{-10}m\cdot\sqrt{3}}{2\sin(\pi/20)}=5.2\cdot 10^{-33}J$$

9b4.

1)



2) Hole is an excited quantum state of multi-electron system, characterized by the thing that one of the single-electron states is unoccupied (from physical encyclopedia). Hole is a point from where an electron went and which can be represented as a quasiparticle with a positive charge equal to the charge of an electron.

3) The luminescence is the radiation of atoms, molecules, ions and other more complex particles, resulting from an electronic transition in these particles during their return from excited to normal state.

4) It is obvious that the addition for the crystal with 1cm radius associated with the quantum behavior would be neglible, in this case $E_g = E_0 = 2.88\times10^{-19}$ J. The following is obtained for the crystal with 1nm radius as per the given formula: $E_g^2 = 8.29\times10^{-38} + (6.26\times10^{-68})/(1.09\times10^{-31}) = 8.29\times10^{-38} + 5.74\times10^{-37} = 6.57\times10^{-37}$ J^2 (All calculations are in SI units). Hence $E_g = 8.1\times10^{-19}$ J.

5) Visible light has a range of 400-750 nm. The smaller the wavelength, the greater the energy, the smaller the radius of the nanoparticle. That is, the minimum size of the nanoparticle will be responsible of the luminescence light with a wavelength of 400 nm, which corresponds to the energy $E_g = h\nu = hc/\lambda = (6.62\times10^{-34}$ J×s) × (3 ×10^8 m/s) / (4×10^{-7} m) = 4.97×10^{-19} J. Transforming the expression to find E_g, this is obtained: $r^2 = (E_0\times h^2) / [2 \times (E_g^2 - E_0^2) \times m] = 1.26\times10^{-85} / 3.58\times10^{-68} = 3.52\times10^{-18}$ m^2, hence $r = 1.88\times10^{-9}$ m or 1.88 nm.

6) $Cd(C_{17}H_{33}COO)_2 + SeP(C_8H_{17})_3 = CdSe + PO(C_8H_{17})_3 + (C_{17}H_{33}CO)_2O$

7) The atmosphere of argon is needed to prevent oxidation of raw and end products. The solvent is chosen high-boiling and inert with respect to the quantum dots. Heating during the synthesis is necessary for obtaining well-crystallized one-dimensional quantum dots. The reagents are selected so as to ensure solubility in appropriate solvents and to eliminate chemical interaction with it. Also reagents must be easy to obtain and store, and have as much molecular weight as possible. The proposed method for the second part of the question is completely unacceptable.

a) The boiling temperature of water is 100 ° C lower than the optimum temperature of synthesis.
b) It is known that cadmium salts are considerably hydrolyzed by a cation and have acid reaction medium, and selenides - anion, hence, their solutions have alkaline reactions. When pouring the solutions, mutually reinforcing hydrolysis will occur. And when it is considered that the reaction is supposed to occur in boiling water, and at pouring the solution dilution of each of them will happen, then, remembering that the heating and dilution just significantly accelerate the hydrolysis, one can precisely say that the main products of the reaction in this case would be useless hydroxide cadmium in the bottom of the vessel and the poisonous gas Hydrogen selenide in the laboratory.
8) Quantum dots based on cadmium selenide are already widely used in the following areas:
a) LED lamp with the main characteristics of an order of magnitude superior to traditional incandescent and mercury lamps;
b) As a component of sensitive sensor devices as the intensity of the luminescence of quantum dots is sensitive to the presence of minimal amounts of vapors of certain substances (amines, arenes) and minimum amounts of certain bacteria, including harmful;
a) Quantum dots of cadmium selenide doped with magnetic components (e.g., iron) can shift the luminescence in the near infrared range, where weakly absorb water and hemoglobin. It is used in magnetic resonance imaging of internal organs and tissues.

9b5.

In this task, the apparent contradiction arises from the thing that the arguments of the first friend the concept of phase and group velocity are confused. In their formulas it is written phase velocity $\upsilon_{ф}$ and group velocity υ_{gr}, but he did not distinguish these speeds and marked them with the same letter υ. Because of this, "veiled" error occurred.

The phase velocity is included in the formula of the period of the wavelength: $T = \frac{\lambda}{\upsilon_{ф}}$, that is why the phase velocity is: $\omega = \frac{2\pi}{T} = \frac{2\pi\upsilon_{ф}}{\lambda}$.

At the same time, group velocity appears in the expression for the pulse: $\vec{p} = m\vec{\upsilon}_{гр}$.

Since the phase and group velocities of the electron are not equal to each other in a chain of equalities below there is an error (a violation of equality is indicated by exclamation marks):

$$\omega = \frac{2\pi}{T} = \frac{2\pi\upsilon}{\lambda} = \frac{2\pi\upsilon p}{h} = \frac{p\upsilon}{\hbar} = \frac{pm\upsilon}{\hbar m} =!!!= \frac{\hbar^2 k^2}{\hbar m} = \frac{\hbar k^2}{m},$$

On the left of the numerator is the product of pulse on the mass at the phase velocity, and on the right of the numerator is the square of the pulse, and these expressions are not equal to each other. Therefore, the formula obtained by the first friend is wrong.

The second friend got the correct formula for connection of frequency with wave vector, contained in a number of textbooks. However, he also made an inaccuracy in reasoning. The thing is that in the formula $E = \hbar\omega$ appears as full energy, and the second friend wrote the expression $E = \frac{p^2}{2m}$, representing the kinetic energy in the nonrelativistic approximation. To be more precise, the relativistic expression should be written for the total energy:

$$E = mc^2 = \sqrt{m_0^2 c^4 + p^2 c^2}$$

where m_0 – the rest mass of an electron, and m - its total mass. Expanding the right side of in Taylor series, there is:

$$\hbar\omega = m_0 c^2 + \frac{p^2}{2m_0} + \ldots$$

where ellipsis identifies a number of the terms of a higher order. Considering $p = \hbar k$, there is:

$$\omega = \frac{m_0 c^2}{\hbar} + \frac{\hbar k^2}{2m_0} + \ldots$$

Thus, the frequency and wave vector are related by the above written formula which differs from formula of the second friend. The difference lies in the presence of a large term in the right side of the rest energy, and corrections, which in the nonrelativistic limit can be considered small (indicated by an ellipsis). However, in practice the frequency of the de Broglie wave of the electrons is not measured directly in experiments, and only difference between the frequencies corresponding energy difference is measured. Therefore, as energy, the frequency of de Broglie waves can be measured not from the absolute zero, but from an arbitrary zero level. This allows choosing as the origin of frequency value $\frac{m_0 c^2}{\hbar}$. Then the formula, obtained by the second friend, is true for nonrelativistic approximation:

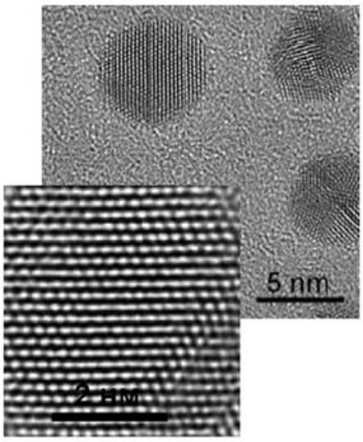
$$\omega = \frac{\hbar k^2}{2m}$$

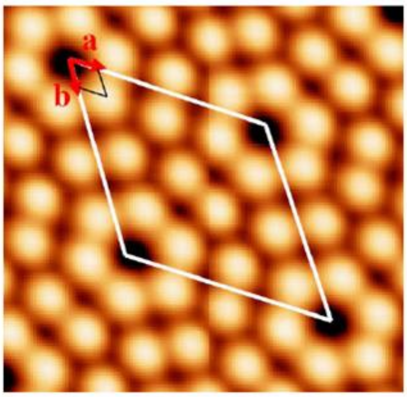
9b6.

First, explain in more detail, what is the proposed "paradox". Recall what the concept of wave-particle duality is:

"All microscopic objects have both wave and corpuscular properties. Their movement in space must be described by the wave theory. The corresponding wave field is distributed in space. However, when measuring the microparticle, space is registered to a certain point as a single entity with all the characteristics of the particle (mass, charge, energy, etc.). The measurement result is probabilistic in nature, to predict where the particle will be detected with certainty unit is impossible. One can only talk about the probability of an event and this probability is ultimately determined by the wave field, which describes the motion of a particle in space.

Simply speaking, "measurement" is an instant photograph on which the electron (or some other particle) is recorded as one point in space, as a point particle with characteristic mass, charge and other characteristics. Therefore, it would seem, not a continuous "electron cloud" is seen on the "photographs" of microworld, but a single point or several points, the position of which is determined randomly with some probability distribution.





Why a continuous cloud is seen? The answer is quite simple: actually it is not dealt with instant photography, but with "photography with great exposure." As known, instant photographs (in the literal sense of the word) do not exist, this is only an idealization, but the real photograph always has the final extract (final imaging time). The real "dimension" in this case is the interaction of atoms with a probe microscope (the scanning probe microscopy), or with an external electron beam (transmission electron microscopy - TEM). Without going into details of the interaction of an atom with a measuring device, one can identify a general property of all the microscopes discussed in such types of tasks: typical time during which images are formed (like the ones in the figure), much larger than the characteristic atomic time, therefore such images are formed statistically as a result of the myriad interactions of atoms with a microscope.

For example, in transmission electron microscopy, image is formed by multiple electron beam, which interact with atoms of the sample and then are registered by the receiver. Each electron separately carries little information and cannot form an image. The same can be said about other types of microscopy. In the AFM, image is formed by processing a large number of cantilever oscillations, but even a period of one oscillation (which already represents a very complex process) is much larger than the characteristic atomic time. Therefore, measuring the interaction potential of the cantilever with an atom is a "shot with great exposure", and this potential is formed statistically from one of the elementary acts of the electromagnetic interaction, which, in terms of quantum field theory, is the exchange of quanta of electromagnetic field - photons.

What is the characteristic atomic time, and how can it be assessed? This is the time during which phase of the wave function (wave field, as discussed above), describing the electron shell of the atom, manages to change to the order of 2π. To put it simply, this is the time during which significant changes occur in atom.

If an electron is found at some point (more precisely, in a sufficiently small neighborhood), then the wave field, describing this electron is localized (concentrated) in this neighborhood. For the wave field to "blur" again and take all the characteristic volume of the atom, it takes time of atomic. The atomic time is estimated by:

$$t_{at} \approx \frac{\hbar}{E_{at}}$$

where $\hbar = 1{,}05 \cdot 10^{-34}$ J·s – Planck's constant with feature, E_{at} – characteristic energy of an electron in an atom (taken modulo). The above written formula can be obtained from Heisenberg's uncertainty relation, written for the energy and time:

$$\Delta E \cdot \Delta t \geq \hbar$$

It can also be obtained from the consideration that the phase of the wave function contains term ωt, where ω – cyclic frequency, and therefore the phase changes by 2π in time

$$T = \frac{2\pi}{\omega} = \frac{2\pi\hbar}{E}.$$

A characteristic electron energy can be estimated as the energy of an electron in the ground state of the simplest atom - hydrogen atom. This value is called the Rydberg (denoted by Ry) and is equal *to* E_{at} = Ry = 13,6 эВ = $2{,}18 \cdot 10^{-18}$J. An estimate for the atomic time is obtained:

$$t_{at} \approx 5 \cdot 10^{-17} \text{ c.}$$

Obviously, this is an extremely short time compared to the time of imaging, given as examples in the problem. For comparison, the maximum oscillation frequency of the cantilever is of the order of several megahertz, which corresponds to the period of oscillation T ~ 10^{-6} s. In scanning electron microscopy, image is formed as a result of multiple interactions of electrons with the sample matrix and the receiver, each of which has a length greater than the atomic time. Also note that the minimum laser pulse duration is of the order of several femtoseconds, which is also much larger than the atomic time.

9b7.

1. Since gold has a high conductivity (~4,3*10^7cm) and rather thin contacts can be obtained from it (plastic deformation at not very high temperatures). For tungsten - high conductivity (~1,2*10^7 Cm), developed method of obtaining thin needles for STM.

2. Physicists have observed the effect of quantum conductance. This is seen from the piecewise linear nature of the CVC. Reducing the size of the conductor leads to a decrease in the levels that determine the conductivity. Thus, not completely filled band appears below the Fermi level, but a set of subbands which are separated by "forbidden" minibands.

The specific conductivity of tungsten G_W = 18200000 Cm/m. Subsequently, specific resistance $\rho_W = 1/G_W$ = 5,4945*10^{-8} Ohm*m.

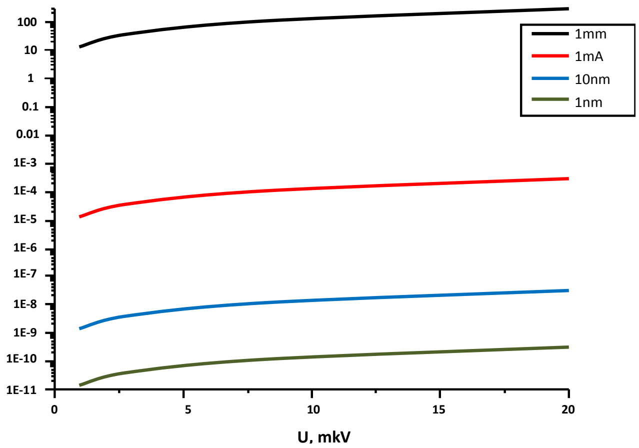
Formulas for calculation:

$S_{sec} = \pi r^2 = (\pi d^2)/4$; $R = \rho l / S_{sec}$.

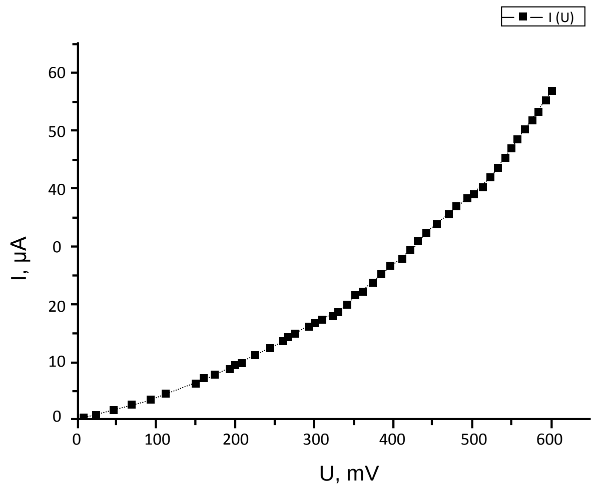
Let l=1m.

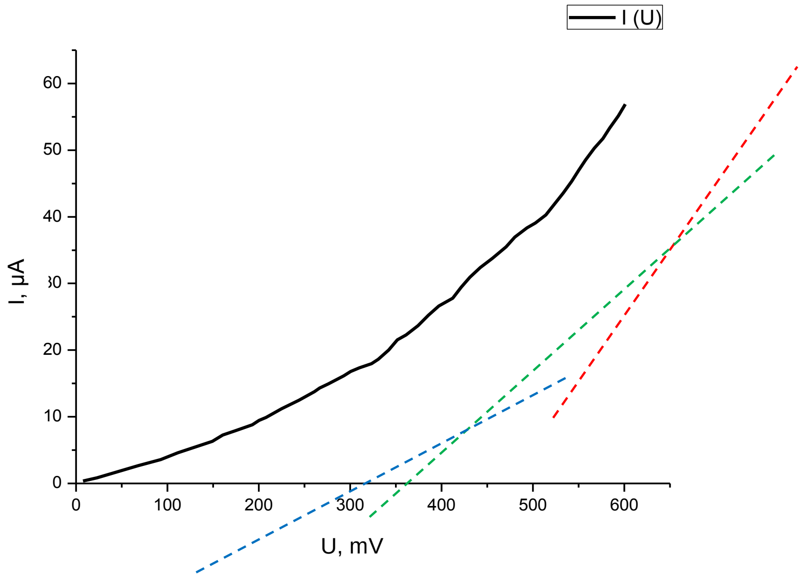
Diameter	Diameter, m	$S_{сеч}$, m^2	R, Ohm
1 mm	1*10^{-3}	7,85*10^{-7}	7*10^{-2}
1 um	1*10^{-6}	7,85*10^{-13}	7*10^{4}
10 nm	1*10^{-8}	7,85*10^{-17}	7*10^{8}
1 nm	1*10^{-9}	7,85*10^{-19}	7*10^{10}

Using formula U = I*R, plot the following graph.



1. Plot the chart of dependence of conduction on the applied voltage as per data given in the table*.*



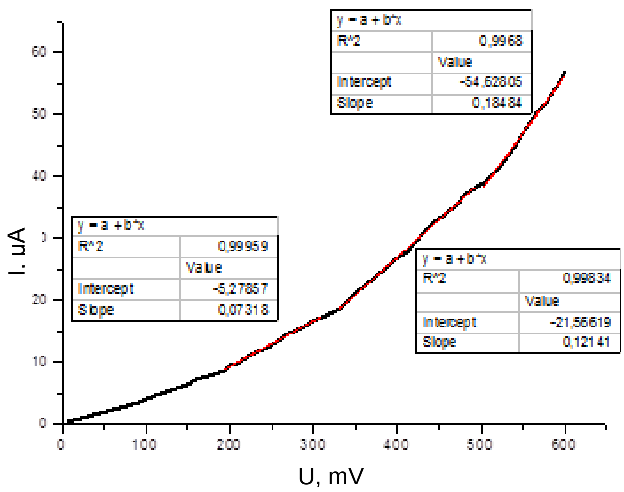


At least 3 regions with different angles of slope of the curve can be clearly distinguished on the presented chart. Calculate the angles for 3 regions:

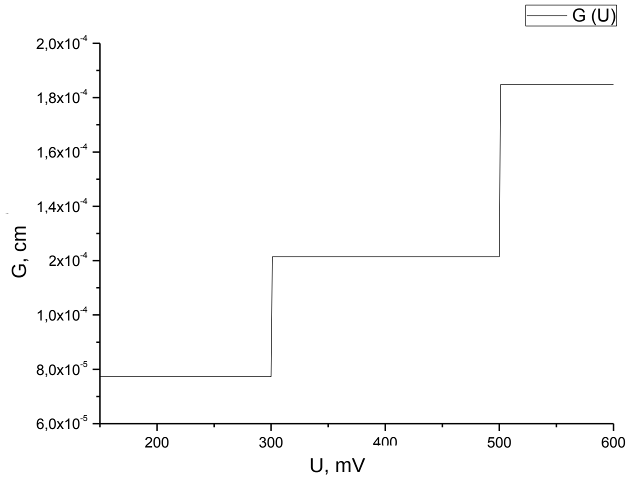
From 150 to 300 mV - 0,07318 uA/mV = 7,7318*10^{-5} cm = G_0;

From 300 to 500 mV - 0,12141 uA/mV = 12,141*10^{-5} cm = 1,5*G_0;

From 500 to 600 mV - 0,18484 uA/mV = 18,484*10^{-5} cm = 2,3*G_0 (for the given case it must be 2*G_0, however, due to errors in the calculation of the tangent, somewhat conservative value is obtained).



Next, construct graph G (U) as per calculated data:



Constant G_0 is usually applied to the above described effect. What is this constant called? What is its dimension and value in the SI system? And for what is this value currently used? (3 points)

$G_0 = 2e^2/h$ - quantum of conductance.

$e = 1{,}6*10^{-19}$ Kl, $h = 6{,}6*10^{-34}$ J*s, consequently $G_0 = 7{,}75*10^{-5}$ cm.

It (or rather its inverse) is used to calibrate the resistance and since 1990 has been the benchmark for measuring the resistance.

9b8.

Answer 1: It is known that films of mesoporous silicon have great specific surface, and its limit reaches the value of about 800 m^2/g. The presence of the developed surface of porous silicon causes the presence of her huge number of defects - dangling silicon bonds, which in turn are trapping centers for FCC. The fact that in the process of electrochemical etching of crystalline silicon, dopant atoms are not "washed" with the silicon atoms must also be taken into account. Therefore, reducing the concentration of FCCs in the meso-PC cannot be attributed to the "removal" of the substance.

Answer 2: Using expression for crystalline silicon it can be written:

$$N_{sthz}(c-Si) = \frac{A\alpha_{c-Si} n_{c-Si}}{\lambda^2 \tau},$$

For porous silicon:

$$N_{FCC}(PC) = \frac{A\alpha_{PC} n_{PC}}{\lambda^2 \tau (1-p)},$$

where $A = 4\pi^2 c^3 \varepsilon_0 m^{*2} / e^2 = const$, $p = 0.6$, α_{c-Si}, $\alpha_{meso-PC}$ – absorption coefficient for crystalline and porous silicon, measured at a wavelength of λ, $n_{c-Si} = 3.4$, $n_{meso-PC} = 1.7$ – refractive index for crystalline and porous silicon, respectively. Using the above written formulas to calculate the concentration of free charge carriers in mesoporous silicon, the following is obtained:

$$N_{FCC}(PC) = \frac{\alpha_{meso-PC} n_{meso-PC} N_{FCC}(c-Si)}{(1-p)\alpha_{c-Si} n_{c-Si}},$$

where N_{c-Si} is equal to 10^{20} cm^{-3}.

Substituting numerical values, the following is obtained:

$$N_{FCC}(PC) \approx \frac{130 cм^{-1} * 1.7 * 10^{20} cm^{-3}}{(1-0.6) * 620 cm^{-1} * 3.4} \approx 2.6 * 10^{19} cm^{-3}$$

Answer 3: During thermal oxidation of silicon nanocrystals, concentration in their FCCs decreases. This is due to the increasing number of defects - dangling silicon bonds that are formed during the oxidation of the samples. It is known that these dangling bonds are trapping centers for FCC.

Answer 4: Microporous silicon films are obtained by electrochemical etching of lightly doped silicon substrates. The concentration of FCCs in these substrates is approximately 10^{16} cm^{-3}. It is also known in case of reducing the size of silicon nanocrystals to a few nanometers (as in the case of microporous silicon), the electronic spectrum of charge carriers undergoes significant changes due to quantum confinement effect. It can therefore be stated that this material is almost completely depleted of charge carriers in equilibrium.

9b9.

The cantilever is represented as a rectangular beam, which bends under the effect of force F, applied along the normal to the free end of the beam. The beam theory of bending was developed by Bernoulli and Euler. It is clear that the upper surface due to deformation is accustomed, and the upper one stretches. For simplicity, beam is replaced by a segment which is bent under load and at each point the curvature is proportional to the moment of external forces. For small deflections of the curvature is almost equal to the second derivative.

So, the interval in the undisturbed position is described by $Z(x) = 0$, and when the load has a certain dependence $Z(x)$, which is to be found.

Thus $EJ\frac{d^2Z}{dx^2} = F(L - X)$.

The coefficient of proportionality EJ is called the flexural rigidity and is equal to the product of the modulus of elasticity of the material of the beam on the moment of inertia.

Modulus of elasticity is given in the problem, and the moment of inertia is given by $J = \frac{wt^3}{12}$. So there is a differential equation with boundary conditions:

$$\begin{cases} EJ\dfrac{d^2Z}{dx^2} = F(L - X) \\ Z(x = 0) = 0 \\ \dfrac{dZ}{dx}(x = 0) = 0 \end{cases}$$

Solution of this system: $Z = \frac{F}{2EJ}\left(Lx^2 - \frac{x^3}{3}\right)$ or $Z' = \frac{F}{EJ}\left(Lx - \frac{x^2}{2}\right)$

For $x = L$ there is the real height of the object: $Z(L) = \frac{4FL^3}{Ewt^3}$.

Generally speaking, the signal of deflection in AFM is proportional to cantilever deflection, that is, Z', but in solving the problem it could also be simplified and assumed that the signal is proportional to height. Both options were considered correct solutions.

Estimate as per the order of the values obtained.

Typical force at work on AFM has the order of F = 1 nN. According to the formula, this corresponds to

$$Z = \frac{4*10^{-9}*8*10^{6}*10^{-18}}{2*10^{10}*40*10^{-6}*\frac{1}{8}*10^{-18}} = \frac{32*10^{-3}}{10^5} = 32*10^{-8} \approx 300 \text{ nm}$$

Let's see what happens if the beam is put in the middle of the cantilever:

$$Z = \frac{12 * 10^{-9}}{2 * 2 * 10^{10} * 40 * 10^{-6} * \frac{1}{8} * 10^{-18}} * \left(200 * 10000 - \frac{1000000}{3}\right) * 10^{-18} = 10^7 * 10^{-14} = 10^{-7} = 100\ nm$$

That is, there was a great mistake in 60%!

When calculating through derivative, the error is 25%.

The difference between the answers is large, but as first of all it is important to do calculations in the first question, they are both counted as correct.

Since Z' is linearly dependent on the force, the same relative error will be obtained at different forces (i.e., heights).

Questions 2 and 3. The data in the topographic images are usually formed as follows. Feedback monitors changes in signal deflection and generates such a signal to move the piezoelectric ceramic to compensate the deviation of all time. Piezoceramic is calibrated and its move (exactly known in nm) gives a high-rise image.

Thus, the incorrect position of the beam on the cantilever does not directly lead to a distortion of the height of objects on topographic images, but also significantly reduces signal/noise ratio. It is more critical for small objects (DNA, thin films, etc.).

Questions 4. To minimize this error, a laser system must be properly set up. But if not sure, one can accurately adjust the laser by choosing a shorter and more rigid cantilever.

9b10.

When hitting a hard surface, the stream breaks up into many drops of different diameters. Due to surface tension, the potential energy of the stream, that crashed on the drops, increases. To estimate, assume that for the formation of drops of a certain diameter at impact it is necessary that the kinetic energy of a selected volume of the drop in the stream be greater than the potential energy of the surface tension of the drop after its discharge from the stream. According to the law of conservation of energy:

$$\frac{m_0V^2}{2} = S\sigma + \frac{m_0V'^2}{2}$$

where S – surface area of drops, m_0 – mass of drop, V' - the speed of drop after impact.
The process of drop formation of a certain diameter has a threshold as per kinetic energy (kinetic energy of a drop after impact is zero). Thus, the condition of the threshold for drop formation:

$$4\pi\sigma R^2 = \frac{2}{3}\pi\rho R^3 V^2$$

$$V = \sqrt{\frac{6\sigma}{\rho R}}$$

For drops with a diameter of 100 nm, the following is obtained:

$$V = \sqrt{\frac{6\sigma}{\rho R}} \approx 92m/s$$

which is less than the speed of sound in air. Consequently, this stream will be heard.
For drops with a diameter of 10 nm:

$$V = \sqrt{\frac{6\sigma}{\rho R}} \approx 290m/s$$

which is also slightly less than the speed of sound.

9b11.
Due to quantization of electron movement, the effective bandgap increases. In conductance region, the energy of basic state (n=1) of electron ($m^* = 0.067m_0$) increases by 55.77 mEV. In valence region ($m^*_{hh} = 0.4m_0$) on the contrary – it decreases by 9.34 mEV. The change of effective bandgap will equal 65.11mEV. Thus, for extensional GaAs, the bandgap is by 65.11mEV smaller than the "effective bandgap" of the GaAs/AlAs quantum well of 100Å width (the energy is equal to $E_n = \frac{\pi^2\hbar^2 n^2}{2m^* d^2}$).

9b12.

The potential outside cubic quantum dot is equal to zero, and inside $-V_0$. The wave vector of the electron takes values from 0 to $k_{\max}$, the value of which will be defined from $k_{\max}(r) = \frac{1}{\hbar}\sqrt{2m^*|V(r)|}$ expression. Thus, in $\Delta x\Delta y\Delta z$ volume, the number of energy levels will be defined by the following expression:

$$\Delta N = 2\Delta x\Delta y\Delta z \frac{4\pi}{(2\pi)^3}\int_0^{k_{\max}} k^2 dk = 2\frac{4\pi}{(2\pi)^3}\frac{k_{\max}^3}{3} = \frac{k_{\max}^3}{3\pi^2}\Delta x\Delta y\Delta z$$

Summing by all coordinates of classically permissible energy regions, the number of states in quantum well will be:

$$N = \frac{(2m^*)^{3/2}}{3\pi^2\hbar^2}\int dxdydz|V(r)|^{3/2} = \frac{(2m^*)^{3/2}}{3\pi^2\hbar^2}V_0^{3/2}L_xL_yL_z$$

For example, if $L_x = L_y = L_z = 100$ Å, V_0=0.2 ev, the number of energy levels in cubic quantum dot $N = 75$.

9b13.
By first approximation quantum well can be considered infinitely deep, the energy levels of which are defined by the following expression $E_n = \frac{\pi^2\hbar^2 n^2}{2m^* d^2}$. Here m^* is the effective mass of the electron

$m^* = 0.067m_0$, n is the quantum number, and d is the well width. For the basic state $n=1$, $E_1 \approx 35$ mEV will be obtained, and for the second level $E_2 \approx 140$ mEV.

9b14.

The energy levels of infinitely deep quantum well are defined by $E_n = \frac{\pi^2\hbar^2 n^2}{2m^* d^2}$. Here m^* is the effective mass of the electron $m^* = 0.067m_0$, n is the quantum number, and d is the well width. In a room temperature the average thermal energy of an electron is $k_B T \approx 26$ mEV. The difference of lower level energies will be:

$$\Delta E_n = E_{n+1} - E_n = \frac{\pi^2\hbar^2}{2m^* d^2}\left((n+1)^2 - n^2\right) = \frac{\pi^2\hbar^2}{2m^* d^2}(2n+1).$$

$$\Delta E_n = \frac{3\pi^2\hbar^2}{2m^* d^2}$$

Equaling the latter to the average thermal energy value, d=14.5nm will be obtained.

9b15.

For the basic state, wave function of the basic state of the electron, located in bulk crystal in mixture center coulomb field is represented by $F(\vec{r}) = \frac{1}{(\pi a_B^3)^{1/2}} \exp\left(-\frac{r}{a_B}\right)$ hydrogen wave function, where a_B is the effective Boron radius and is defined by $a_B = \frac{\varepsilon\hbar^2}{m^* e^2} = 0.53\varepsilon\frac{m_0}{m^*}$ Å. Particularly, for $GaAs$ crystal $\varepsilon = 12.85$, $m^* = 0.067m_0$ and therefore $a_B \approx 100$ Å. Binding energy of basic state is given by $R_y^{3D} = \frac{m^* e^4}{2\hbar^2} = 13600\frac{m^*}{m_0}$ mEV expression. For $GaAs$, $R_y^{3D} \approx 5.5$ mEV.

In 3D coulomb task, making $l + \frac{1}{2} = |m|$ substitution in $E_{n_r,l} = -\frac{m^* e^4}{2\hbar^2 (n_r + l + 1)^2}$ which defines the energy levels of binding states, $E_{n_r,l} = -\frac{m^* e^4}{2\hbar^2\left(n_\rho + |m| + \frac{1}{2}\right)^2}$ energy expression of 2D coulomb task will be easily defined. Denoting $N = n_\rho + |m| + 1$ for 2D for energy levels, $E_N = -\frac{m^* e^4}{2\hbar^2\left(N - \frac{1}{2}\right)^2}$ will finally be obtained, where $N = 1, 2, 3, \ldots$. As seen from energy expressions, for the basic binding state ($n_r = 0, l = 0, N = 1$), the state energy surpasses the energy value of the basic state four times in 3D.

9b16.

The effective mass of electron for GaAs is $m^* = 0.067m_0$. In a quantum well, the state density function is defined by $\rho(E) = \frac{m^* S}{\pi\hbar^2}\sum_n \theta(E - E_n)$, where $\theta(E)$ is the unit jump function. State density function for unit area will be:

$$\frac{\rho(E)}{S} = 1.6*10^{-19}\frac{0.067*0.9*10^{-30}kg}{3.14*(1.05*10^{-34})} = 2.78*10^{13} eV^{-1}cm^{-2}$$

For critical density:

$$n_c = \frac{\rho(E)}{S} k_B T = 2.78*10^{13} eV^{-1}cm^{-2} * 25.9meV = 72*10^{10} cm^{-2}$$

9b17.

The motion of electron is limited in eFz triangle potential well. As $\left[\hbar^2/2m^*\right]$=energy*length² and $\left[eF\right]$ =energy/length, then $z_0=\left(\frac{\hbar^2}{2m^*eF}\right)^{1/3}$ value has length unit: In this case $E_0=eFz_0=z_0=\left(\frac{\hbar\left(eF\right)^2}{2m^*}\right)^{1/3}$ expression has energy unit: To accurately solve the Schrödinger equation, the following will be obtained for the energy:

$$E_n=\left(\frac{\hbar\left(eF\right)^2}{2m^*}\right)^{1/3}\alpha_n,\ n=1,2,3$$

where α_n are the zeros of Eyring function. For the basic state when $n=1,\ \alpha_n=2.34$ and field tenseness is 10^4V/cm, $E_1\approx 2.34\left(\frac{\hbar\left(eF\right)^2}{2m^*}\right)^{1/3}=7.5$ mEV.

9b18.

The exciton absorption coefficient is defined by:

$$\alpha\left(\hbar\omega\right)=\frac{\pi e^2\hbar}{2n_r\varepsilon_0 cm_0\hbar\omega}\left(\frac{2\left|p_{cv}\right|^2}{m_0}\right)a_p\left(\frac{1}{\sqrt{1.44\pi}}\frac{1}{\sigma}\frac{1}{W\pi a_{ex}^3}\exp\left(\frac{-\left(\hbar\omega-E_{ex}\right)^2}{1.44\sigma^2}\right)\right)$$

Due to quantization, the following modification has been implemented $\frac{1}{\pi a\left(3D\right)_{ex}^3}\to\frac{1}{W\pi a\left(QW\right)_{ex}^3}$.

Considering $a_{ex}\left(QW\right)\cong\frac{2}{3}a_{ex}\left(3D\right)$ connection between exciton radiuses in quantum well and in bulk sample, and $a_p=\frac{1}{2}$ for x polarization of light, the following will be obtained:

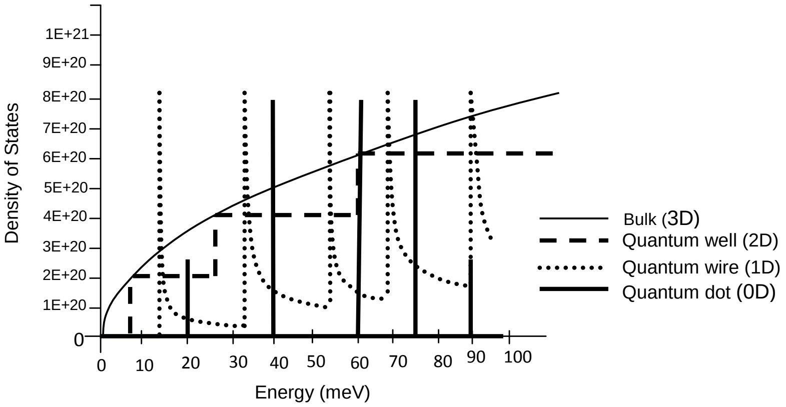
$$\alpha\left(\hbar\omega\right)=\frac{3.14*\left(1.6*10^{-19}C\right)^2\left(1.05*10^{-34}Js\right)}{2*3.4\left(8.85*10^{-12}F/m\right)\left(3*10^8m/s\right)\left(0.91*10^{-30}kg\right)}\left(\frac{25}{1.5}\right)\left(\frac{1}{3}\right)*$$

$$*\frac{1}{\sqrt{1.44*3.14}}\frac{1}{\sigma\left(meV\right)\left(1.6*10^{-19}J\right)}\frac{1}{\left(3.14*120*10^{-10}m\right)^3}\exp\left(\frac{-\left(\hbar\omega-E_{ex}\right)^2}{1.44\sigma^2}\right)=$$

$$=\frac{2.9*10^6}{\sigma\left(meV\right)}\exp\left(\frac{-\left(\hbar\omega-E_{ex}\right)^2}{1.44\sigma^2}\right)$$

When $\sigma=1meV$, then $\alpha\left(\hbar\omega\right)=2.9*10^6m^{-1}$.

9b19.



9b20.

Intensity of radiated light is equal to:

$$I=I_0\exp\left(-\alpha d\right)$$

If there is no field:

$$\alpha(0)=\frac{2.9*10^4}{2.5}\exp\left(\frac{-(1.49-1.51)^2}{1.44(2.5*10^{-3})^2}\right)\approx 0$$

When 80kV/cm voltage is applied, the exciton peak deviates by 20mEV. Then the absorption coefficient will be equal to:

$$\alpha(80kV/cm)=\frac{2.9*10^4}{2.5}\exp\left(\frac{-(1.49-1.49)^2}{1.44(2.5*10^{-3})^2}\right)\approx 1.2*10^4 cm^{-1}$$

Finally, for intensity ratio, the following will be obtained:

$$\frac{I(80kV/cm)}{I(0)}=0.3$$

9b21.

Height of p-n junction's potential barrier at the thermodynamic equilibrium is defined as follows:

$$e\varphi_c = kT\ln\frac{n_n p_p}{n_i^2}, \tag{1}$$

where

$$n_i^2 = N_c N_\upsilon \exp\left(-\frac{E_g}{kT}\right),\quad N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2},\ N_\upsilon = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2}.$$

Solve n_i^2 and substitute it in Equation (1):

$$n_i^2 = N_c N_\upsilon \exp\left(-\frac{E_g}{kT}\right) = 4\cdot\left(m_n^* m_p^*\right)^{3/2}\cdot\left(\frac{2\pi kT}{h^2}\right)^3\exp\left(-\frac{E_g}{kT}\right),$$

$$n_i^2 = 4\cdot[0{,}4\cdot 0{,}073\cdot(9{,}1\cdot 10^{-31}\text{kg})^2]^{3/2}\cdot\left(\frac{2\cdot 3{,}14\cdot 0{,}026\cdot 1{,}6\cdot 10^{-19}\text{J}}{(6{,}626\cdot 10^{-34}\text{ Js})^2}\right)^3\exp\left(-\frac{1{,}34}{0{,}026}\right) = 15{,}04\cdot 10^{-93}\text{kg}^3\cdot 2{,}11\cdot$$

$$10^{140}\ \text{J}^{-3}\text{s}^{-6}\cdot 4{,}14\cdot 10^{-23} = 1{,}31\cdot 10^{24}\left(\frac{\text{kg}}{\text{Js}^2}\right)^3 = 1{,}31\cdot 10^{24}\text{m}^{-6} = 1{,}31\cdot 10^{12}\text{cm}^{-6}.$$

Then using Equation (1), this is obtained:

$$e\varphi_c = 0{,}026\cdot\ln\frac{5\cdot 10^{16}\cdot 2\cdot 10^{16}}{1{,}31\cdot 10^{12}} = 0{,}026\cdot(2{,}03+46{,}05) = 1{,}25\text{ eV}.$$

The total thickness of the space charge layer is defined as follows:

$$L = \sqrt{\frac{2\varepsilon\varepsilon_0\varphi_c}{e}\frac{n_n+p_p}{n_n p_p}}\,. \tag{2}$$

Substituting constants in Equation (2) and taking into account that vacuum permittivity $\varepsilon_0 = 8{,}85\cdot 10^{-14}$ F/cm, there is:

$$L = \sqrt{\frac{2\cdot 12{,}35\cdot 8{,}85\cdot 10^{-14}\cdot 1{,}25}{1{,}6\cdot 10^{-19}}\frac{5\cdot 10^{16}+2\cdot 10^{16}}{5\cdot 10^{16}\cdot 2\cdot 10^{16}}\frac{\text{F}\cdot\text{V}\cdot\text{cm}^2}{\text{C}}} =$$

$$= \sqrt{11{,}952\cdot 10^{-10}}\text{cm} = 3{,}46\cdot 10^{-5}\text{ cm}\approx 0{,}35\ \mu\text{m}.$$

The barrier capacity of the p-n junction is defined as:

$$C = \frac{\varepsilon\varepsilon_0}{L}: \tag{3}$$

Then substituting constants value, there is:

$$C = \frac{12{,}35\cdot 8{,}85\cdot 10^{-14}}{3{,}46\cdot 10^{-5}}\text{F/cm}^2 = 3{,}16\cdot 10^{-8}\text{ F/cm}^2 = 31{,}6\ \text{pF/cm}^2.$$

Solution: $1{,}25$ eV, $0{,}35\ \mu$m, $31{,}6\ \text{pF/cm}^2$

9b22.

The electron concentration can be found from the following equation:

$$n_i = \sqrt{n_0 p_0} = \sqrt{N_c N_\upsilon}\exp\left(-\frac{E_g}{2kT}\right).$$

Here n_0 and p_0 are the equilibrium concentration of the carriers, and

$$N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2},\qquad N_\upsilon = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2}.$$

Substituting constants ($\pi = 3{,}14$, $k = 1{,}38 \cdot 10^{-23}\mathrm{J/K}$, $h = 6{,}626 \cdot 10^{-34}\mathrm{Js} = 4{,}136 \cdot 10^{-15}$eVs) and problem data, this is found:

$$n_i = 4{,}9 \cdot 10^{15} \cdot (0{,}56 \cdot 0{,}37)^{3/4} \cdot (300)^{3/2} \cdot \exp\left(-\frac{0{,}66}{0{,}052}\right) = 2{,}4 \cdot 10^{13}\mathrm{cm}^{-3}.$$

Solution: $2{,}4 \cdot 10^{13}\mathrm{cm}^{-3}$

9b23.

The electron concentration can be found from the following equation:

$$n_0 = N_c \exp\left(-\frac{E_g}{kT}\right).$$

For temperatures T_1 and T_2 there are, correspondingly:

$$n_0(T_1) = N_c(T_1) \cdot \exp\left(-\frac{3{,}23 - 4 \cdot 10^{-4} T_1}{kT_1}\right), \qquad n_0(T_2) = N_c(T_2) \cdot \exp\left(-\frac{3{,}23 - 4 \cdot 10^{-4} T_2}{kT_2}\right).$$

Finally

$$\frac{n_0(T_1)}{n_0(T_2)} = \left(\frac{T_1}{T_2}\right)^{3/2} \cdot \frac{\exp\left(-\frac{3{,}23-4\cdot 10^{-4}T_1}{kT_1}\right)}{\exp\left(-\frac{3{,}23-4\cdot 10^{-4}T_2}{kT_2}\right)}.$$

After substituting the values of the constants, it is found that:

$$\frac{n_0(T_1)}{n_0(T_2)} = \left(\frac{300}{200}\right)^{3/2} \cdot \frac{\exp\left(-\dfrac{3{,}23 - 4 \cdot 10^{-4} \cdot 300}{0{,}026}\right)}{\mathrm{exph}\left(-\dfrac{3{,}23 - 4 \cdot 10^{-4} \cdot 280}{0{,}024}\right)} =$$

$$1{,}837 \cdot \frac{\exp(-119{,}615)}{\exp(-129{,}917)} = 1{,}837 \cdot \exp(-119{,}615 + 129{,}917) \approx 5{,}5 \cdot 10^4.$$

Solution: $5{,}5 \cdot 10^4$ times

9b24.

For the resistivity, there is:

$$\rho = \frac{1}{e\mu_n n_0 + e\mu_p p_0}. \tag{1}$$

On the other hand, there is the following equation:

$$n_0 p_0 = n_i^2. \tag{2}$$

Joint resolution of Equations (1) and (2) gives the following quadratic equation for the concentration n_0:

$$n_0^2 - \frac{n_0}{e\mu_n \rho} + \frac{\mu_p}{\mu_n} n_i^2 = 0. \tag{3}$$

Solutions of Equation (3) are the following:

$$n_0 = \frac{1}{2e\mu_n\rho}\left[1 \mp \sqrt{1 - 4\mu_n\mu_p(e\rho n_i)^2}\right].$$

Substituting constants, there is:

$$n_0 = \frac{1}{2 \cdot 1{,}6 \cdot 10^{-19} \cdot 1000 \cdot 10^5}\left[1 - \sqrt{1 \mp 4 \cdot 1000 \cdot 200 \cdot (1{,}6 \cdot 10^{-19} \cdot 10^5 \cdot 10^{10})^2}\right]$$

$$= 3{,}13 \cdot 10^{10}\left[1 - \sqrt{1 \mp 0{,}02}\right] \mathrm{cm}^{-3}$$

Taking into account that $n_0 \geq 0$, the following solution is ofund:

$$n_0 \approx 3{,}1 \cdot 10^8 \mathrm{cm}^{-3}.$$

Solution: $3{,}1 \cdot 10^8 \mathrm{cm}^{-3}$

I-XI ANNUAL INTERNATIONAL MICROELECTRONICS OLYMPIADS OF ARMENIA

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