
2016

iGP: Autonomous Car

iGP Module: SATA Host IP Implementation

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Introduction:

SATA Host IP Core is an essential component ideal for the storage system which does not have internal CPU to control SATA Device access. In this project, students will design a SATA Host IP core using SystemC and CatapultC in the implementation. The RTL generated from CatapultC will be synthesized on Altera FPGA and benchmarked against already existing SATA Host IPs we have. We will implement also UVM test environment for verifying the SATA Host IP operation. If stuff worked fine, we can interface this SATA Host IP design with Altera Serdes and make hardware validation versus commercial SATA HDD.

The scope of the project will be the design, verification and realization of SATA Host Transport and Link layers using HLS, CatapultC ,UVM verification methodology and Altera FPGA flow.